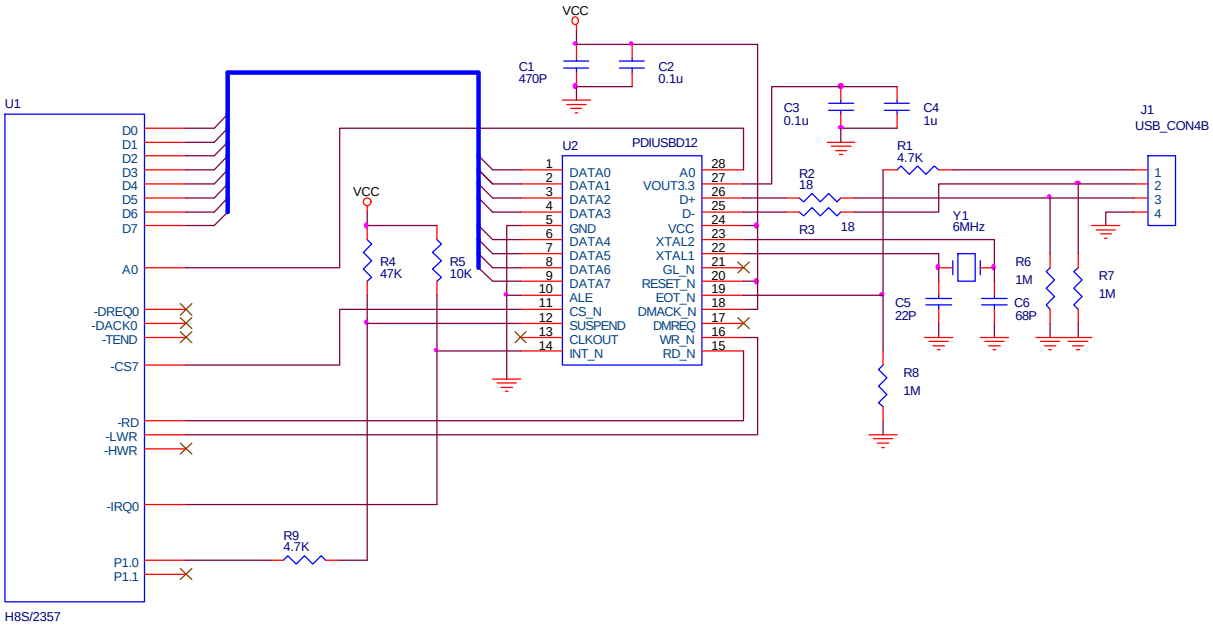
8 June 1998

Application Notes

Interfacing PDIUSBD12 to Hitachi H8S/2357

Application Notes: Interfacing PDIUSBD12 to Hitachi H8S/2357

Example Interfacing Circuit in Non-DMA Mode



Above schematic shows interfacing PDIUSBD12 to H8S/2357 with minimum glue logic components. The PDIUSBD12 works in non-DMA mode.

1. Interrupt Handling

Program the *IRQ Sense Control Register (ISCRH and ISCRL)* to specify low-level sense IRQ input.

2. Address Mapping

The bus controller partitions the total 16Mbytes address space into eight areas, 0 to 7, in 2Mbytes units. The bus controller will output CS0 to CS7 when external address space for each area is accessed.

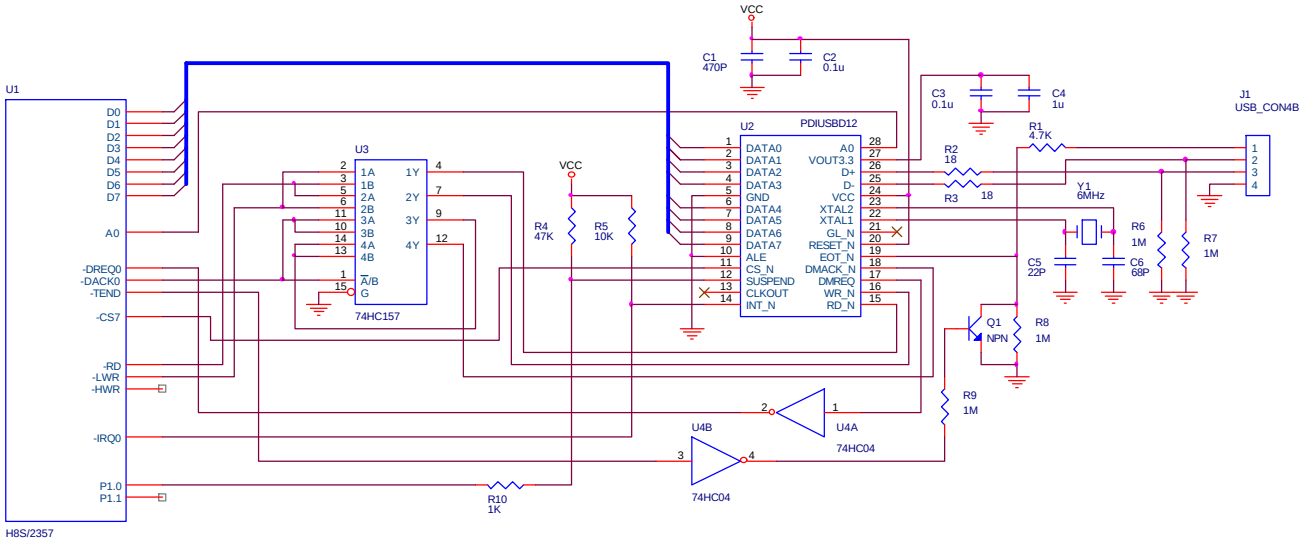
PDIUSBD12 can be mapped to any address area, where is simple for interfacing requirements. In above example circuit, PDISUBD12's base address is mapped to H'FFFF08 in CS7 area. Assuming that it is the only external device within this area, CS7 can be directly connected to CS_N.

The external bus specifications, bus width, number of access states and number of program wait states, can be programmed for each area. Recommend setting for PDIUSBD12 are 8-bit bus in *Bus Width Control Register (ABWCR)*, enable wait states in *Access State Control Register (ASTCR)* and 1 program wait states in *Wait Control Register (WCRH and WCRL)*.

3. Using DMA

H8S/2357 can be programmed to single-address DMA to work with PDIUSBD12. In single address DMA mode, the source and destination are accessed within the same read/write cycle. But this doesn't mean DMA transfer will be significantly faster than non-DMA, because the transfer rate is also limited by USB bus maximum bulk transfer rate (1.152MBytes/S) and PDIUSBD12 parallel bus interface speed (2MBytes/s).

Application Notes: Interfacing PDIUSBD12 to Hitachi H8S/2357



Above circuit shows single address mode DMA interface. A quad 2-input multiplexer, 74HC157, is used to generate RD_N, WR_N and proper delay on DMACK_N to PDIUSBD12. DMREQ needs to be inverted and TEND from H8S/2357 needs to be converted to an open collector output.

4. I/O Ports

In example interfacing schematic, PDIUSBD12's SUSPEND pin is connected to P1.0 which is configured as a general input port by default. P1.0 may be configured to a general output port when it is required to drive SUSPEND pin low during remote wake up.

The 4.7K resistor (R9) is added as protection against the faulty situation when P1.0 output high and PDIUSBD12 pulls SUSPEND pin low.

There are 3 registers to configure port 1: *Port 1 Data Direction Register (P1DDR)*, *Port 1 Data Register (P1DR)* and *Port 1 Register (PORT1).*