BURR - BROWN®

PCM1737

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SoundPLUS™ 24-Bit, 192kHz Sampling Enhanced Multi-Level, Delta-Sigma, Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 24-BIT RESOLUTION
- ANALOG PERFORMANCE (V_{CC} = +5V):
  Dynamic Range: 106dB typ
  SNR: 106dB typ
  THD+N: 0.0015% typ
  Full-Scale Output: 3.1Vp-p typ
- 4x/8x OVERSAMPLING DIGITAL FILTER:
  Passband: 0.454f_S
  Stopband: 0.546f_S
  Stopband Attenuation: –82dB
  Passband Ripple: ±0.002dB
- SAMPLING FREQUENCY: 10kHz to 192kHz
- SYSTEM CLOCK: 128, 192, 256, 384, 512, or 768f_S with Auto Detect
- ACCEPTS 16-, 18-, 20-, AND 24-BIT AUDIO DATA
- DATA FORMATS: Standard, I^2S, and Left-Justified
- USER-PROGRAMMABLE MODE CONTROLS:
  Digital Attenuation: 0dB to –63dB, 0.5dB/Step
  Digital De-Emphasis
  Digital Filter Roll-Off: Sharp or Slow
  Soft Mute
  Variable Oversampling for ΔΣ DACs
  Zero Detect Mute
  Zero Flags for Each Output
- DUAL SUPPLY OPERATION:
  +5V Analog, +3.3V Digital
- 5V TOLERANT DIGITAL INPUTS
- SMALL 28-LEAD SSOP PACKAGE

APPLICATIONS

- A/V RECEIVERS
- DVD MOVIE AND AUDIO PLAYERS
- DVD ADD-ON CARDS FOR HIGH-END PCs
- HDTV RECEIVERS
- CAR AUDIO SYSTEMS
- OTHER APPLICATIONS REQUIRING 24-BIT AUDIO

DESCRIPTION

The PCM1737 is a CMOS, monolithic, integrated circuit which includes stereo Digital-to-Analog converters and support circuitry in a small 28-lead SSOP package. The data converters utilize Burr-Brown's enhanced multi-level delta-sigma architecture, which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1737 accepts industry standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 192kHz are supported. A full set of user-programmable functions are accessible through a 4-wire serial control port which supports register write and read back functions.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1552A
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SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = +5V, $+V_{DD}$ = +3.3V, system clock = $384f_S$ (f_S = 44.1kHz) and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1737E MIN	PCM1737E TYP	PCM1737E MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Formats	User Selectable		Standard, I²S, Left-Justified		
Audio Data Bit Length	User Selectable		16-, 18-, 20-, 24-Bit		
Audio Data Format			MSB-First, Binary Two's Complement		
System Clock Frequency			128, 192, 256, 384, 512, $768f_S$		
Sampling Frequency (f_S)		10		200	kHz
DIGITAL INPUT/OUTPUT					
Logic Family			TTL-Compatible		
Input Logic Level					
V_{IH}		2.0			V
V_{IL}				0.8	V
Input Logic Current					
I_{IH}	$V_{IN} = V_{DD}$			0.1	µA
I_{IL}	V_{IN} = 0V			–0.1	µA
I_{IH}(1)	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}(1)	V_{IN} = 0V			–0.1	µA
Output Logic Current, Pin 25 (MDO)					
I_{IZH}	At Output Disable, $V_{IN} = V_{DD}$			2.0	µA
I_{IZL}	At Output Disable, V_{IN} = 0V			–0.1	µA
Output Logic Level					
V_{OH}(2)	I_{OH} = –2mA	2.4			V
V_{OL}(2)	I_{OL} = +2mA			1.0	V
V_{OH}(3)	I_{OH} = –4mA	2.4			V
V_{OL}(3)	I_{OL} = +4mA			1.0	V
DYNAMIC PERFORMANCE(4)					
THD+N, V_{OUT} = 0dB	f_S = 44.1kHz, SCLK = $384f_S$		0.0015	0.0035	%
	f_S = 96kHz, SCLK = $256f_S$		0.0020	0.0050	%
	f_S = 192kHz, SCLK = $128f_S$		0.0025	0.0060	%
V_{OUT} = –60dB	f_S = 44.1kHz		0.6	0.8	%
	f_S = 96kHz		0.7	1.0	%
	f_S = 192kHz		0.8	1.2	%
Dynamic Range	EIAJ, A-Weighted, f_S =44.1kHz	102	106		dB
	A-Weighted, f_S = 96kHz	100	105		dB
	A-Weighted, f_S =192kHz	98	104		dB
Signal-to-Noise Ratio(5)	EIAJ, A-Weighted, f_S =44.1kHz	100	105		dB
	A-Weighted, f_S = 96kHz	100	104		dB
	A-Weighted, f_S = 192kHz	100	104		dB
Channel Separation	f_S = 44.1kHz	96	102		dB
	f_S = 96kHz		101		dB
	f_S = 192kHz	96	102		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error	$V_O = 0.5V_{CC}$ at Bipolar Zero		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		62% of V_{CC}		Vp-p
Center Voltage			50% V_{CC}		V
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristic, Sharp Roll-Off					
Passband	±0.002dB			$0.454f_S$	Hz
	–3dB			$0.490f_S$	Hz
Stopband		$0.546f_S$			Hz
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = $0.546f_S$	–75			dB
	Stopband = $0.567f_S$	–82			dB
Filter Characteristics, Slow Roll-Off 1					
Passband	±0.002dB			$0.274f_S$	Hz
	–3dB			$0.454f_S$	Hz
Stopband		$0.732f_S$			Hz
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = $0.732f_S$	–82			dB

SPECIFICATIONS (Cont.)

All specifications at +25°C, $+V_{CC}$ = +5V, $+V_{DD}$ = +3.3V, system clock = $384f_S$ (f_S = 44.1kHz) and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1737E MIN	PCM1737E TYP	PCM1737E MAX	UNITS
DIGITAL FILTER PERFORMANCE (cont.)					
Filter Characteristics, Slow Roll-Off 2					
Passband	±0.01dB			$0.072f_S$	Hz
	–3dB			$0.363f_S$	Hz
Stopband		$0.952f_S$			Hz
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = $0.732f_S$	–49			dB
Delay Time			$34/f_S$		sec
De-Emphasis Error			±0.1		dB
ANALOG FILTER PERFORMANCE					
Frequency Response	f = 20kHz		–0.03		dB
	f = 44kHz		–0.20		dB
Cut-Off Frequency	–3dB		190		kHz
POWER SUPPLY REQUIREMENTS					
Voltage Range					
V_{DD}		+3.0	+3.3	+3.6	V
V_{CC}		+4.5	+5.0	+5.5	V
Supply Current					
I_{DD}[6]	V_{DD} = +3.3V				
	f_S = 44.1kHz		8.5	12.0	mA
	f_S = 96kHz, $256f_S$		16.5		mA
	f_S = 192kHz, $128f_S$		19.5		mA
I_{CC}	V_{CC} = 5.0V				
	f_S = 44.1kHz		13.0	18.0	mA
	f_S = 96kHz, $256f_S$		14.0		mA
	f_S = 192kHz, $128f_S$		14.5		mA
Power Dissipation	V_{DD} = 3.3V, V_{CC} = 5.0V				
	f_S = 44.1kHz		93	130	mW
	f_S = 96kHz, $256f_S$		124		mW
	f_S = 192kHz, $128f_S$		137		mW
TEMPERATURE RANGE					
Operation		0		+70	°C
Storage		–55		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Pins 8, 9, 26, 27, 28 (TEST1, TEST2, MDI, MC, ML). (2) Pins 23, 24 (ZEROL, ZERO). (3) Pin 4 (CLKO). (4) Analog performance specifications are tested with Shibasoku #725 THD Meter 400Hz, HPF on, 30kHz LPF on, average mode with 20kHz bandwidth limiting. The load connected to the analog output is 5kΩ or larger, AC-coupled. (5) SNR is tested with Infinite Zero Detection off. (6) CLKO is disabled.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, $+V_{DD}$	+4.0V
$+V_{CC}$	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Digital Input Voltage	–0.2V to +5.5V
Digital Output Voltage[1]	–0.2V to (V_{DD} + 0.2V)
Input Current (except power supply)	±10mA
Power Dissipation	650mW
Operating Temperature Range	0°C to +70°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, 10s)	+235°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

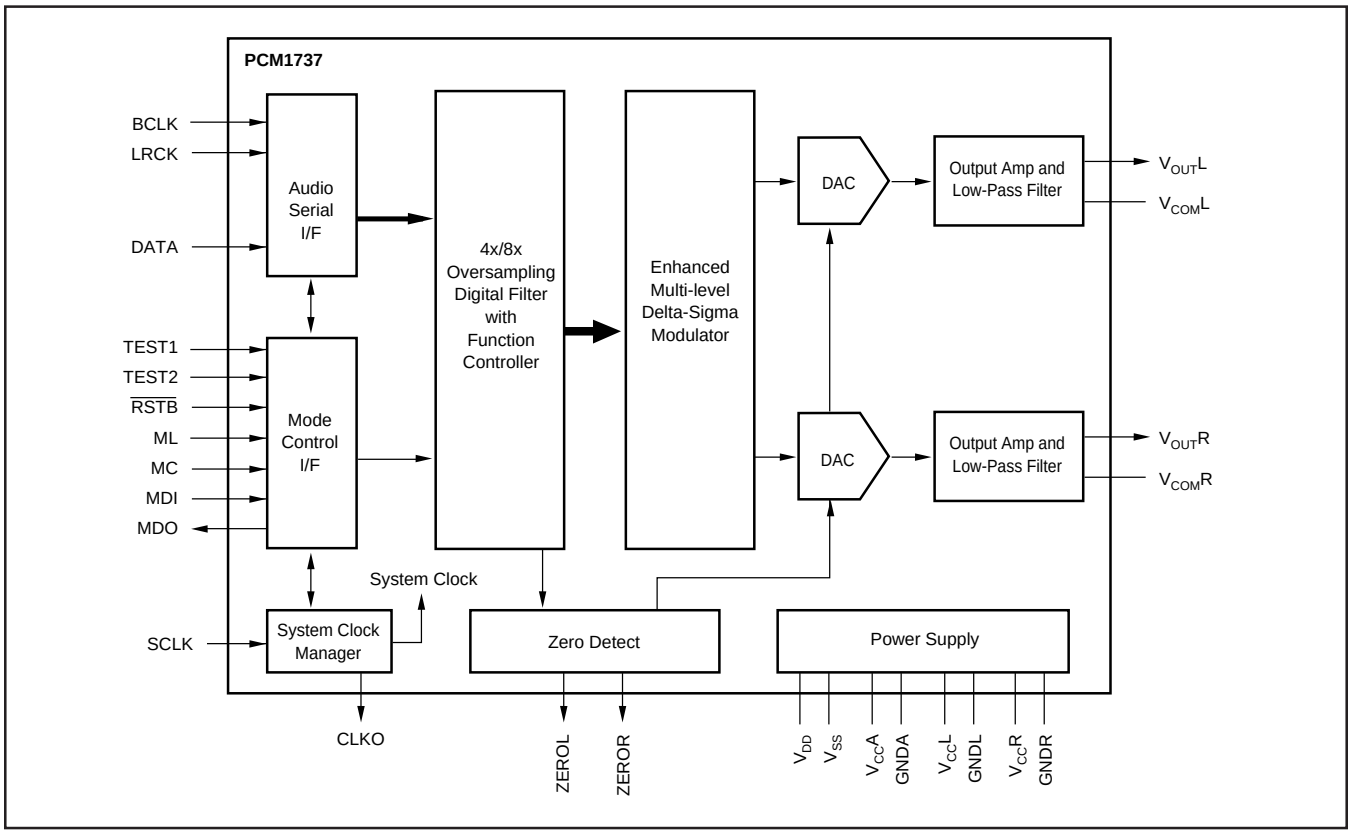
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
PCM1737E	28-Lead SSOP	324	0°C to +70°C	PCM1737E	PCM1737E	Rails
"	"	"	"	"	PCM1737E/2K	Tape and Reel

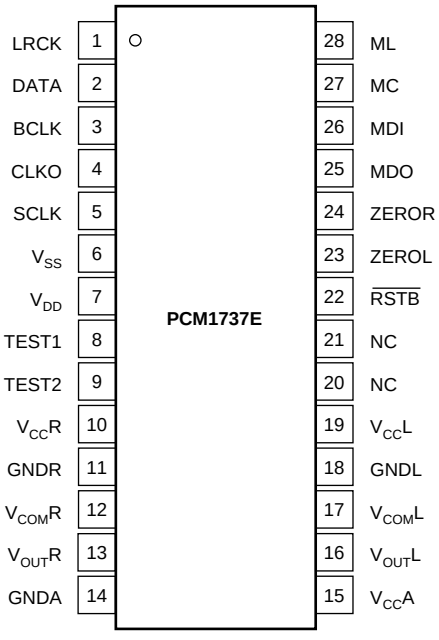
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1737E/2K" will get a single 2000-piece Tape and Reel.

BLOCK DIAGRAM



PIN CONFIGURATION

Top View **SSOP**



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	LRCK	I	Left/Right Word Clock(1)
2	DATA	I	Data In for Left/Right Channels(1)
3	BCLK	I	Bit Clock(1)
4	CLKO	O	System Clock Output
5	SCLK	I	System Clock Input(1)
6	V_{SS}	—	Digital Ground
7	V_{DD}	—	Digital Supply, +3.3V.
8	TEST1	I	Test Pin(2). Must be connected to ground (V_{SS}).
9	TEST2	I	Test Pin(2). Must be connected to ground (V_{SS}).
10	$V_{CC}R$	—	Analog Supply for Right Channel, +5V
11	GNDR	—	Analog Ground for Right Channel
12	$V_{COM}R$	—	Common for Right Channel
13	$V_{OUT}R$	O	Analog Output for Right Channel
14	GNDA	—	Analog Ground
15	$V_{CC}A$	—	Analog Supply, +5V
16	$V_{OUT}L$	O	Analog Output for Left Channel
17	$V_{COM}L$	—	Common for Left Channel
18	GNDL	—	Analog Ground for Left Channel
19	$V_{CC}L$	—	Analog Supply for Left Channel, +5V
20	NC	—	Not Connected
21	NC	—	Not Connected
22	$\overline{RSTB}$	I	Reset, Active Low(2).
23	ZEROL	O	Zero Flag for Left Channel
24	ZEROR	O	Zero Flag for Right Channel
25	MDO	O	Mode Data Out(3)
26	MDI	I	Mode Data In(2)
27	MC	I	Mode Clock(2)
28	ML	I	Mode Latch(2)

NOTES: (1) Schmitt-Trigger input, 5V tolerant. (2) Schmitt-Trigger input with internal pull-down, 5V tolerant. (3) Tri-state output.

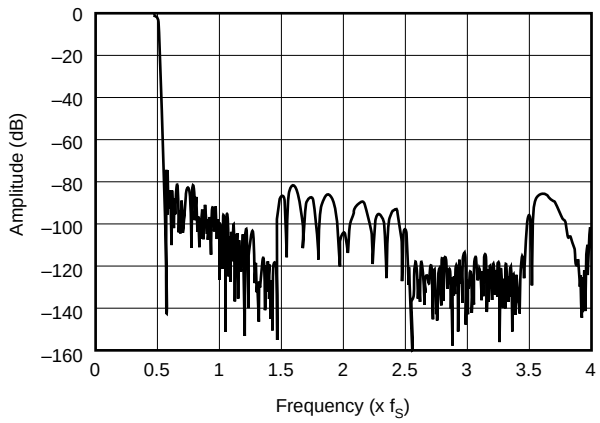
TYPICAL PERFORMANCE CURVES

All specifications at T_A = +25°C, V_{DD} = V_{CC} = 5V, SYSCLK = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

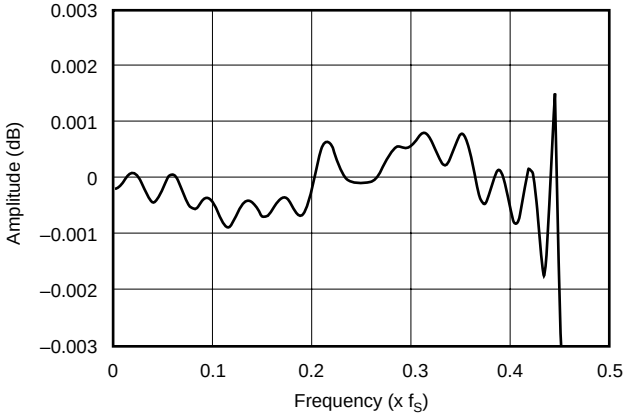
DIGITAL FILTER

Digital Filter (De-Emphasis Off, f_S = 44.1kHz)

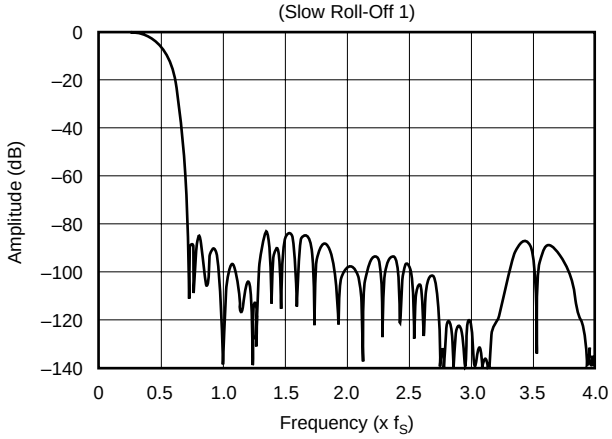
FREQUENCY RESPONSE
(Sharp Roll-Off)



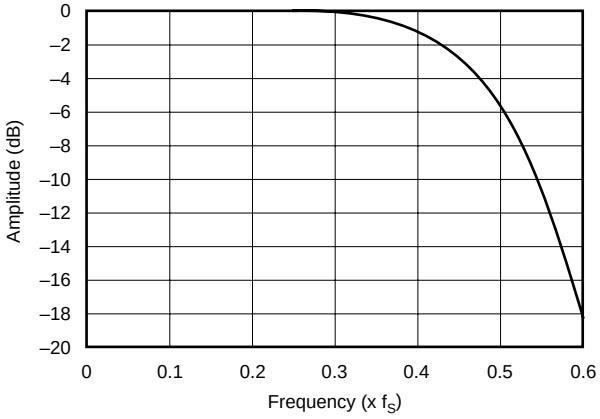
PASSBAND RIPPLE
(Sharp Roll-Off)



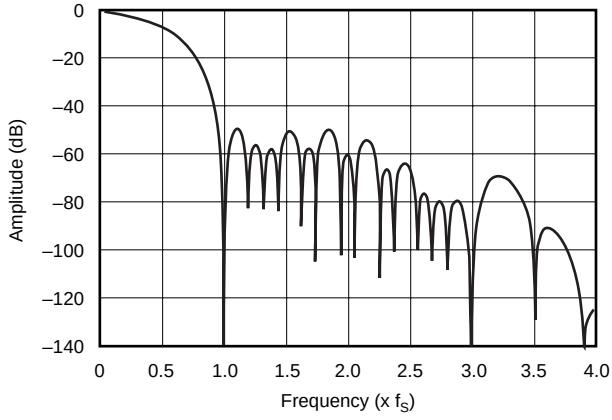
FREQUENCY RESPONSE
(Slow Roll-Off 1)



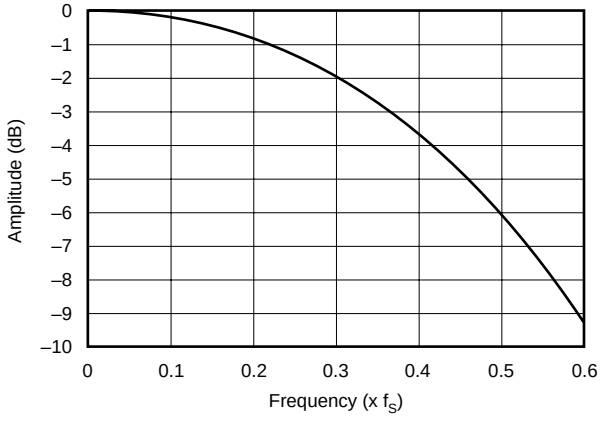
TRANSITION CHARACTERISTICS
(Slow Roll-Off 1)



FREQUENCY RESPONSE
(Slow Roll-Off 2)



TRANSITION CHARACTERISTICS
(Slow Roll-Off 2)



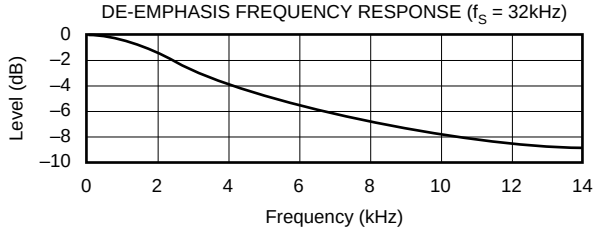
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at T_A = +25°C, V_{DD} = V_{CC} = 5V, SYSCLK = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

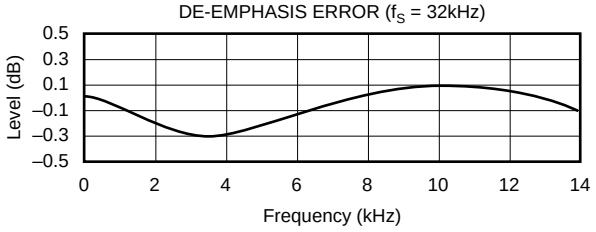
DIGITAL FILTER

De-Emphasis Error

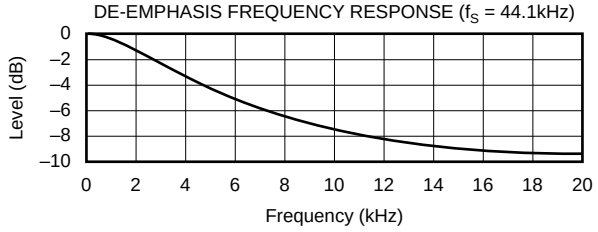
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 32kHz)



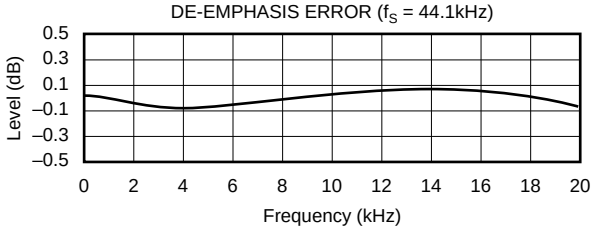
DE-EMPHASIS ERROR (f_S = 32kHz)



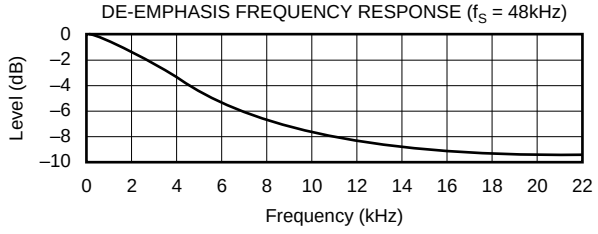
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 44.1kHz)



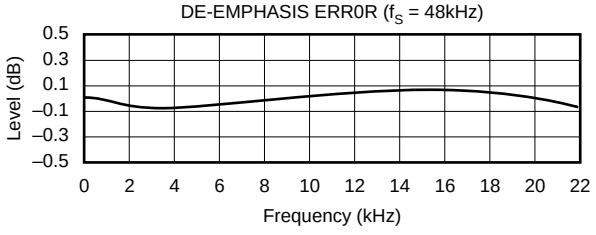
DE-EMPHASIS ERROR (f_S = 44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (f_S = 48kHz)



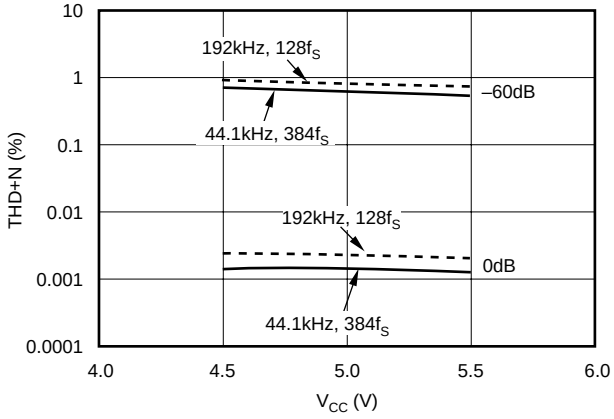
DE-EMPHASIS ERR0R (f_S = 48kHz)



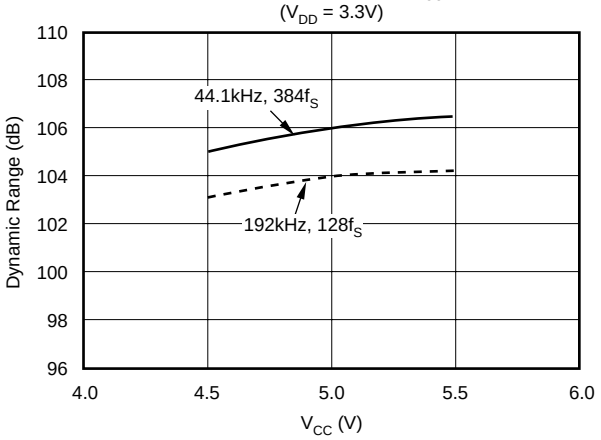
ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

TOTAL HARMONIC DISTORTION + NOISE vs V_{CC} (V_{DD} = 3.3V)



DYNAMIC RANGE vs V_{CC} (V_{DD} = 3.3V)



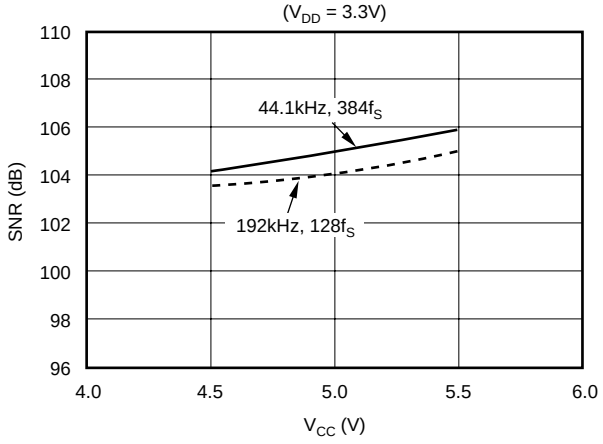
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at T_A = +25°C, V_{DD} = V_{CC} = 5V, SYSCLK = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

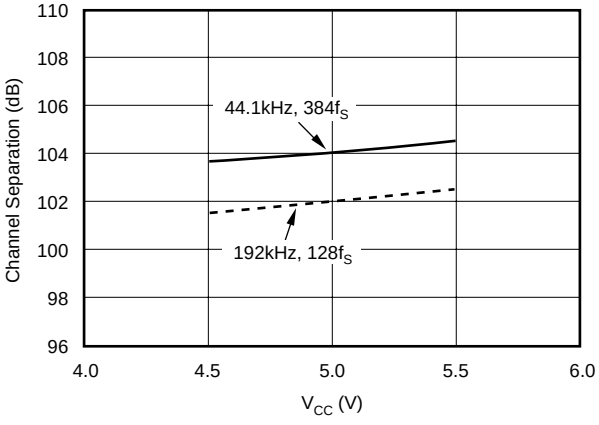
ANALOG DYNAMIC PERFORMANCE (con.t)

Supply Voltage Characteristics

SIGNAL-TO-NOISE RATIO vs V_{CC}
(V_{DD} = 3.3V)

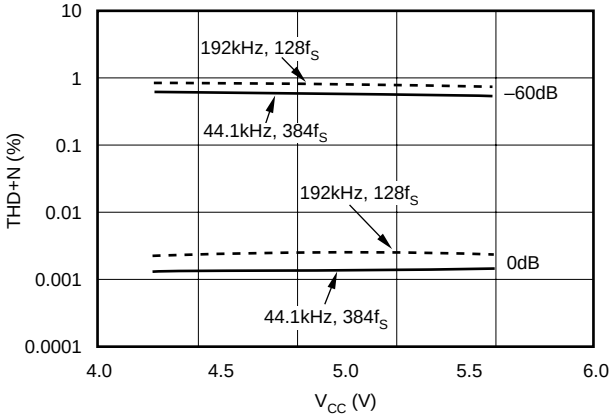


CHANNEL SEPARATION vs V_{CC}

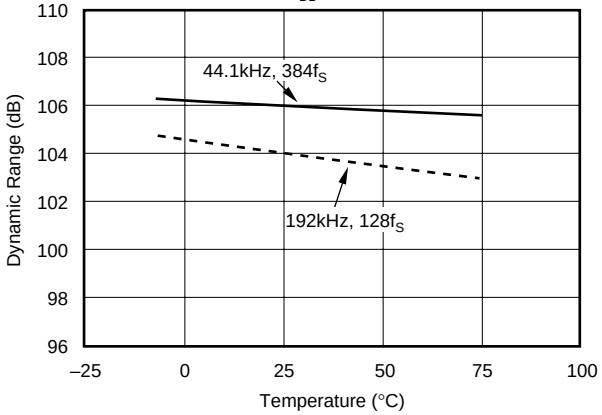


Temperature Characteristics

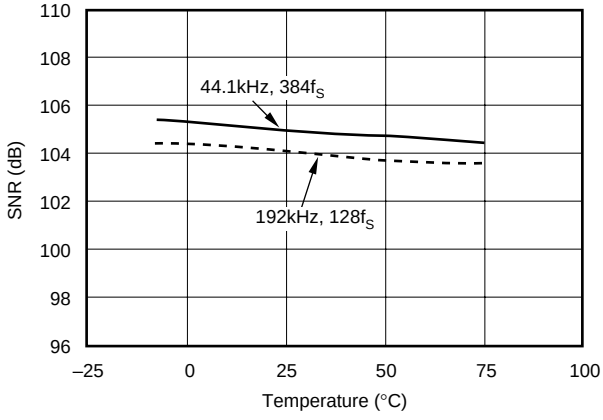
TOTAL HARMONIC DISTORTION + NOISE
vs TEMPERATURE



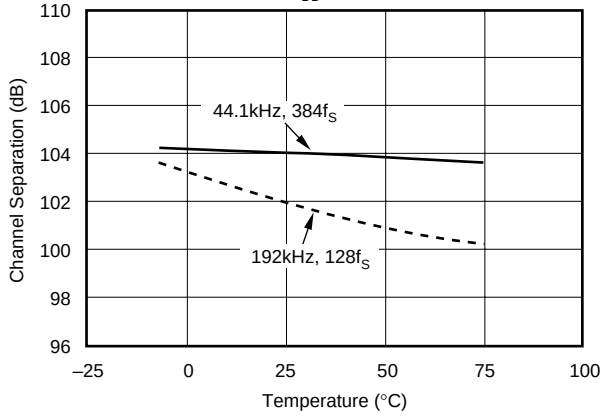
DYNAMIC RANGE vs TEMPERATURE
(V_{DD} = 3.3V)



SIGNAL-TO-NOISE RATIO vs TEMPERATURE
(V_{DD} = 3.3V)



CHANNEL SEPARATION vs TEMPERATURE
(V_{DD} = 3.3V)



SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

The PCM1737 requires a system clock for operating the digital interpolation filters and multi-level delta-sigma modulators. The system clock is applied at the SCLK input (pin 5). Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Burr-Brown's PLL1700 multi-clock generator is an excellent choice for providing the PCM1737 system clock.

SYSTEM CLOCK OUTPUT

A buffered version of system clock input is available at the CLKO output (pin 4). CLKO can operate at either full (f_{SCLK}) or half ($f_{SCLK}/2$) rate. The CLKO output frequency may be programmed using the CLKD bit of Control Register 20. The CLKO output pin can also be enabled or disabled using the CLKE bit of Control Register 20. The default is CLKO enabled.

POWER-ON AND EXTERNAL RESET FUNCTIONS

The PCM1737 includes a power-on reset function. Figure 2 shows the operation of this function. The system clock input at SCLK should be active for at least one clock period prior to V_{DD} = 2.0V. With the system clock active and V_{DD} > 2.0V, the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2.0V. After the initialization period, the PCM1737 will be set to its reset default state, as described in the Mode Control Register section of this data sheet.

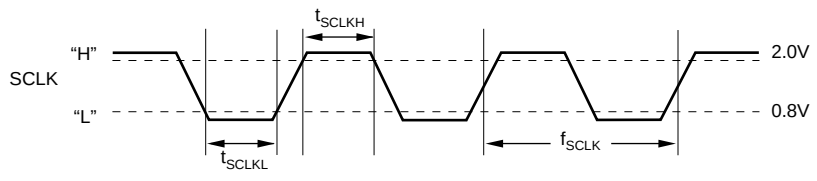
The PCM1737 also includes an external reset capability using the $\overline{RSTB}$ input (pin 22). This allows an external controller or master reset circuit to force the PCM1737 to initialize to its reset default state.

Figure 3 shows the external reset operation and timing. The $\overline{RSTB}$ pin is set to logic '0' for a minimum of 20ns. The $\overline{RSTB}$ pin is then set to a logic "1" state, which starts the initialization sequence which lasts for 1024 system clock periods. After the initialization sequence is complete, the PCM1737 will be set to its reset default state, as described in the Mode Control Register section of this data sheet.

SAMPLING FREQUENCY (f_S)	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)					
	$128f_S$	$192f_S$	$256f_S$	$384f_S$	$512f_S$	$768f_S$
16kHz	—	—	4.0960	6.1440	8.1920	12.2880
32kHz	—	—	8.1920	12.2880	16.3840	24.5760
44.1kHz	—	—	11.2896	16.9344	22.5792	33.8688
48kHz	—	—	12.2880	18.4320	24.5760	36.8640
88.2kHz	—	—	22.5792	33.8688	45.1584	See Note 1
96kHz	12.2880	18.4320	24.5760	36.8640	49.1520	See Note 1
176.4kHz	22.5792	33.8688	See Note 2	See Note 2	See Note 2	See Note 2
192	24.5760	36.8640	See Note 2	See Note 2	See Note 2	See Note 2

NOTE: (1) The $768f_S$ system clock rate is not supported for f_S > 64kHz. (2) This system clock rate is not supported for the given sampling frequency.

TABLE I. System Clock Rates for Common Audio Sampling Frequencies.



System Clock Pulse Width High t_{SCLKH} : 7ns min
System Clock Pulse Width Low t_{SCLKL} : 7ns min

FIGURE 1. System Clock Input Timing.

The external reset is especially useful in applications where there is a delay between PCM1737 power up and system clock activation. In this case, the $\overline{\text{RSTB}}$ pin should be held at a logic '0' level until the system clock has been activated. The $\overline{\text{RSTB}}$ pin may then be set to a logic '1" state to start the initialization sequence.

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1737 is comprised of a 3-wire synchronous serial port. It includes LRCK (pin 1), BCLK (pin 3), and DATA (pin 2). BCLK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the audio interface's serial shift register. Serial data is clocked into the PCM1737 on the rising edge of BCLK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface's internal registers.

Both LRCK and BCLK must be synchronous to the system clock. Ideally, it is recommended that LRCK and BCLK be derived from the system clock input or output, SCLK or CLKO. The left/right clock, LRCK, is operated at the sampling frequency, f_S. The bit clock, BCLK, may be operated at 48 or 64 times the sampling frequency.

Audio Data Formats and Timing

The PCM1737 supports industry-standard audio data formats, including standard, I^2S, and left-justified. The data formats are shown in Figure 4. Data formats are selected using the format bits, FMT[2:0], in Control Register 20. The default data format is 24-bit standard. All formats require Binary Two's Complement, MSB-first audio data. Figure 5 shows a detailed timing diagram for the serial audio interface.

SERIAL CONTROL INTERFACE

The serial control interface is a 4-wire serial port which operates asynchronously to the serial audio interface. The serial control interface is utilized to program and read the on-chip mode registers. The control interface includes MDO (pin 25), MDI (pin 26), MC (pin 27), and ML (pin 28). MDO is the serial data output, used to read back the values of the mode registers. MDI is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data in and out of the control port. ML is the control port latch clock.

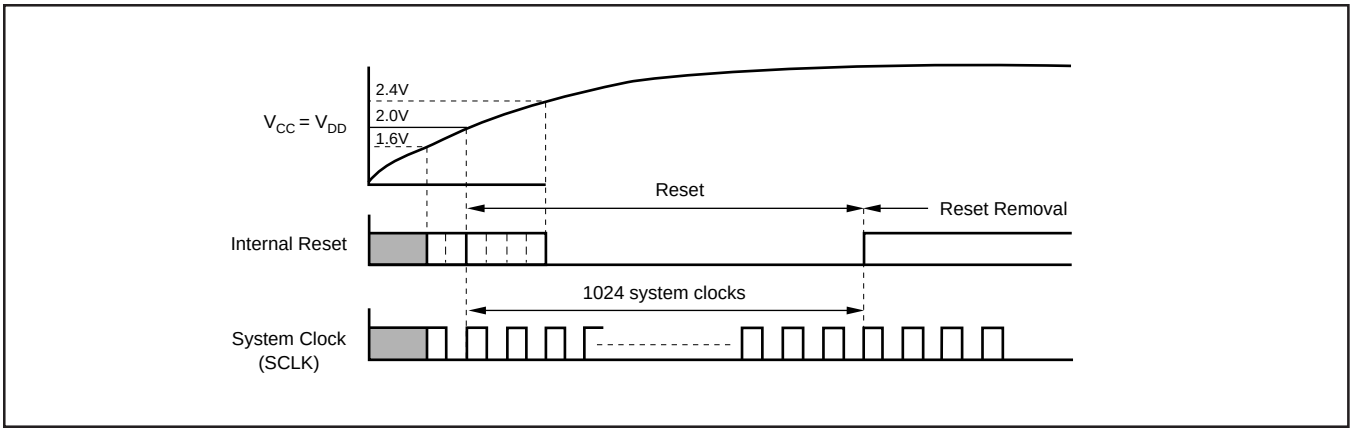


FIGURE 2. Power-On Reset Timing.

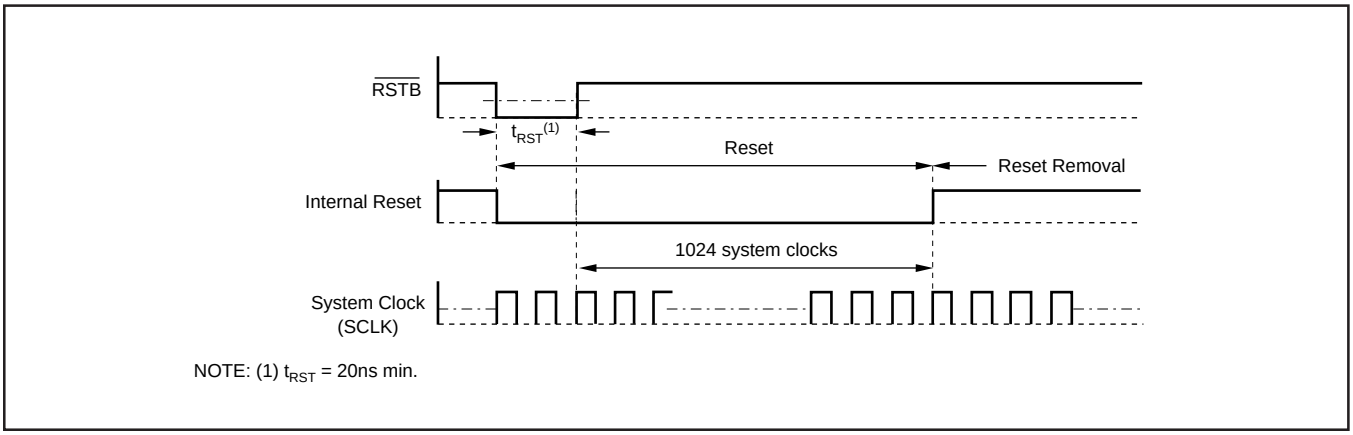


FIGURE 3. External Reset Timing.

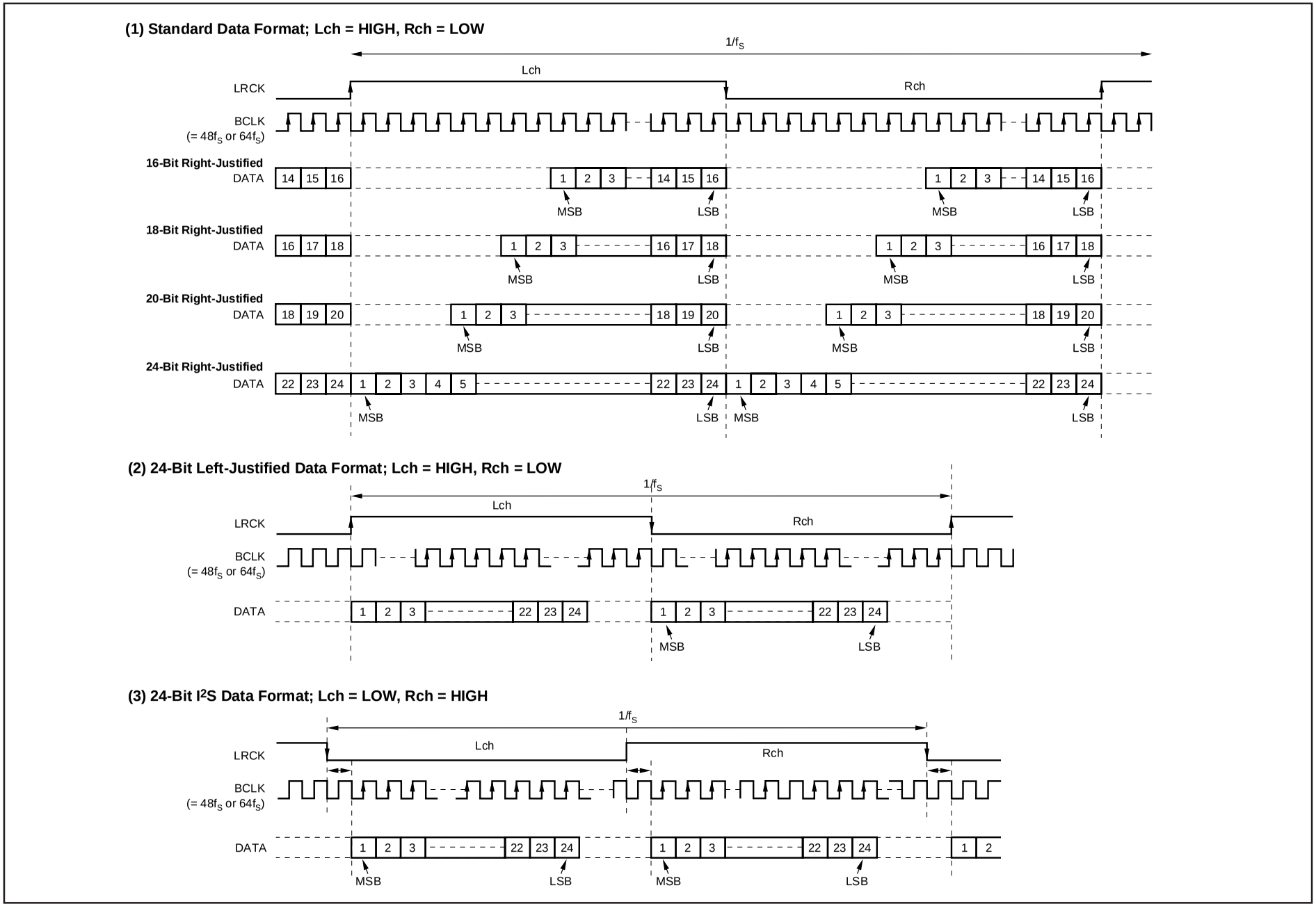


FIGURE 4. Audio Data Input Formats.

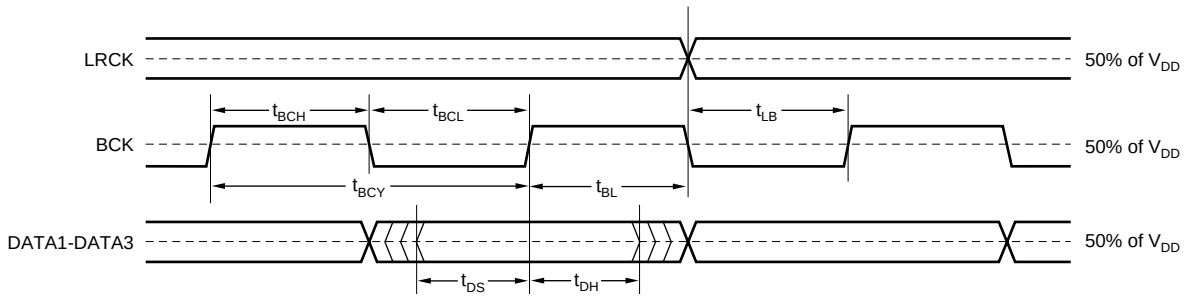
REGISTER WRITE OPERATION

All Write operations for the serial control port use 16-bit data words. Figure 6 shows the control data word format. The most significant bit is the Read/Write (R/W) bit. When set to '0', this bit indicates a Write operation. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the Write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 7 shows the functional timing diagram for writing the serial control port. ML is held at a logic '1' state until a register needs to be written. To start the register write cycle, ML is set to logic '0'. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI. After the sixteenth clock cycle has completed, ML is set to logic '1' to latch the data into the indexed mode control register.

SINGLE REGISTER READ OPERATION

Read operations utilize the 16-bit control word format shown in Figure 6. For Read operations, the Read/Write (R/W) bit is set to '1'. Read operations ignore the index bits, IDX[6:0], of the control data word. Instead, the REG[6:0] bits in Control Register 21 are used to set the index of the register that is to be read during the Read operation. Bits IDX[6:0] should be set to 00_H for Read operations.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{BCY}	BCK Pulse Cycle Time		48 or 64f_S[(1)]	
t_{BCH}	BCK High Level Time	50		ns
t_{BCL}	BCK Low Level Time	50		ns
t_{BL}	BCK Rising Edge to LRCK Edge	30		ns
t_{LB}	LRCK Falling Edge to BCK Rising Edge	30		ns
t_{DS}	DIN Set Up Time	30		ns
t_{DH}	DIN Hold Time	20		ns

NOTE: (1) f_S is the sampling frequency (e.g., 44.1kHz, 48kHz, 96kHz, etc.)

FIGURE 5. Audio Interface Timing.

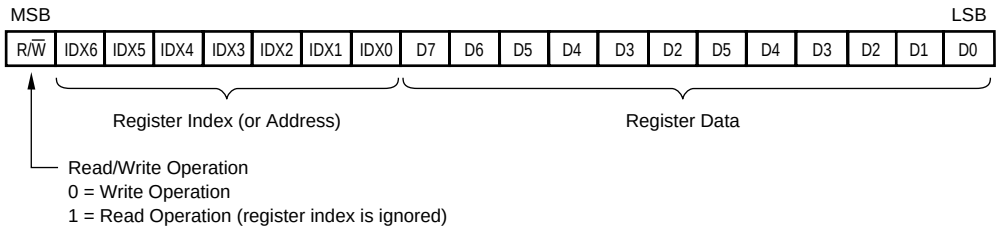


FIGURE 6. Control Data Word Format for MDI.

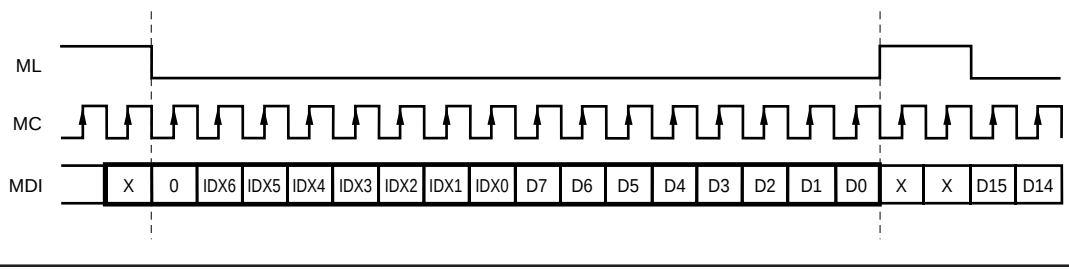


FIGURE 7. Write Operation Timing.

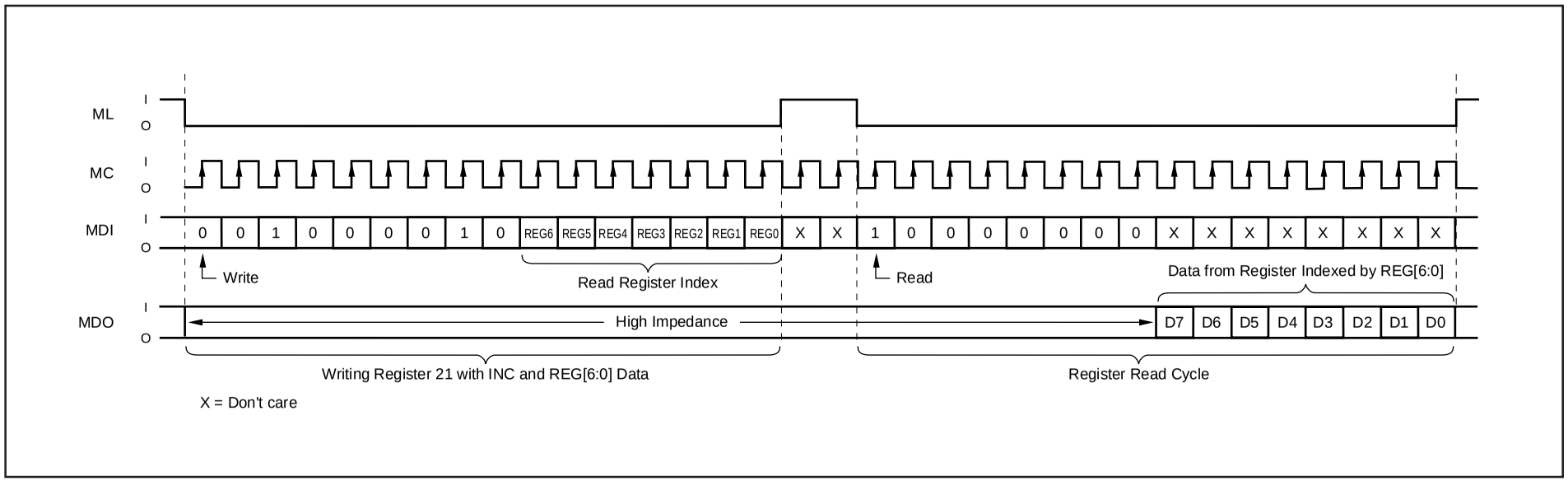


FIGURE 8. Read Operation Timing with INC = 0 (Single Register Read).

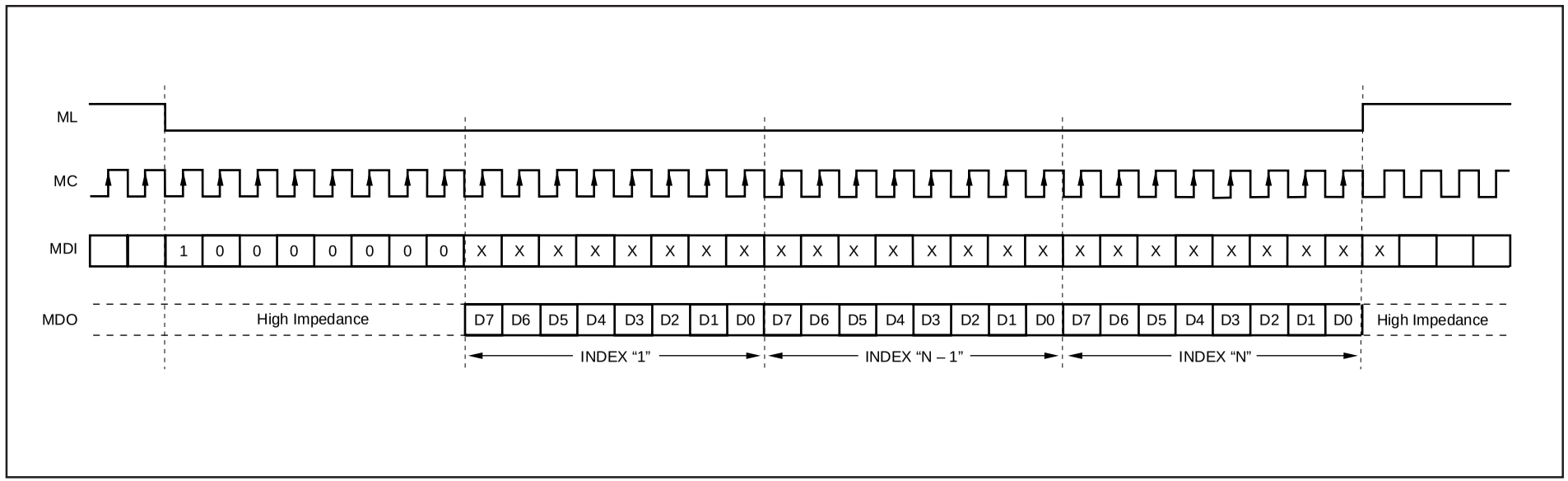


FIGURE 9. Read Operation Timing with INC = 1 (Auto-Increment Read).

Figure 8 details the Read operation. First, Control Register 21 must be written with the index of the register to be read back. In addition, the INC bit must be set to logic '0' in order to disable the auto-increment read function. The Read cycle is then initiated by setting ML to logic '0' and setting the R/W bit of the control data word to logic '1', indicating a Read operation. MDO remains at a high impedance state until the last 8 bits of the 16-bit read cycle, which corresponds to the 8 data bits of the register indexed by the REG[6:0] bits of Control Register 21. The Read cycle is complete when ML is set to '1', immediately after the MC clock cycle for the least significant bit of indexed control register has completed.

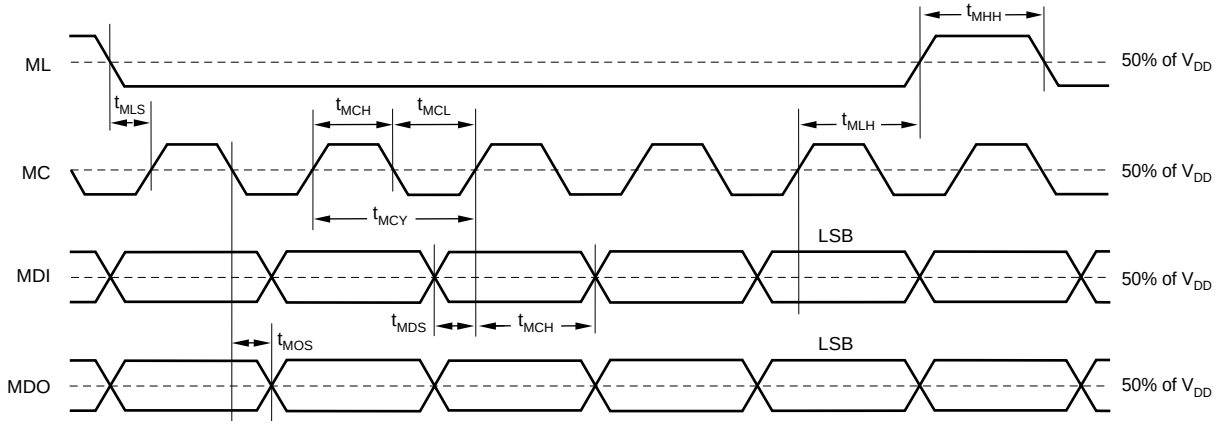
AUTO-INCREMENT READ OPERATION

The Auto-Increment Read function allows for multiple registers to be read sequentially. The Auto-Increment function is enabled by setting the INC bit of Control Register 21 to '1'. The sequence always starts with Register 1, and ends with the register indexed by the REG[6:0] bits in Control Register 21.

Figure 9 shows the timing for the Auto-Increment Read operation. The operation begins by writing Control Register 21, setting INC to '1' and setting REG[6:0] to the last register to be read in the sequence. The actual Read operation starts on the next High to Low transition of the ML pin. The Read cycle starts by setting the R/W bit of the control word to '1', and setting all of the IDX[6:0] bits to '0'. All subsequent bits input on the MDI are ignored while ML is set to '0'. For the first 8 clocks of the Read cycle, MDO is set to a high impedance state. This is followed by a sequence of 8-bit words, each corresponding the data contained in Control Registers 1 through N, where N is defined by the REG[6:0] bits in Control Register 21. The Read cycle is complete when ML is set to '1', immediately after the MC clock cycle for the least significant bit of Control Register N has completed.

CONTROL INTERFACE TIMING REQUIREMENTS

Figure 10 shows a detailed timing diagram for the serial control interface. Pay special attention to the setup and hold times, as well as t_{MLS} and t_{MLH}, which define minimum delays between edges of the ML and MC clocks. These timing parameters are critical for proper control port operation.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{MCY}	MC Pulse Cycle Time	100		ns
t_{MCL}	MC Low Level Time	50		ns
t_{MCH}	MC High Level Time	50		ns
t_{MHH}	ML High Level Time	300		ns
t_{MLS}	ML Falling Edge to MC Rising Edge	20		ns
t_{MLH}	ML Hold Time(1)	20		ns
t_{MDI}	Hold Time	15		ns
t_{MDS}	MDL Set Up Time	20		ns
t_{MOS}	MC Falling Edge to MDSO Stable		30	ns

NOTE: (1) MC rising edge for LSB to ML rising edge.

FIGURE 10. Control Interface Timing.

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1737 includes a number of user programmable functions which are accessed via control registers. The registers are programmed using the Serial Control Interface which was previously discussed in this data sheet. Table II lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table IV. Each register includes a R/W bit, which determines whether a register read (R/W =1) or write (R/W = 0) operation is performed. Each register also includes an index (or address) indicated by the IDX[6:0] bits.

FUNCTION	RESET DEFAULT	REGISTER	BIT(S)
Digital Attenuation Control, 0dB to –63dB in 0.5dB Steps	0dB, No Attenuation	16 and 17	AT1[7:0]
Soft Mute Control	Mute Disabled	18	MUT[2:0]
Digital Attenuation Speed Select	$2/f_S$	18	ATTS
Digital Attenuation Control	Attenuator Disabled	18	ATLD
Infinite Zero Detect Mute	Disabled	18	INZD
Oversampling Rate Control ($64f_S$ or $128f_S$)	$64f_S$ Oversampling	18	OVER
DAC Operation Control	DAC1 and DAC2 Enabled	19	DAC[2:1]
De-Emphasis Function Control	De-Emphasis Disabled	19	DM12
De-Emphasis Sample Rate Selection	44.1kHz	19	DMF[2:1]
Audio Data Format Control	24-Bit Standard Format	20	FMT[2:0]
CLKO Output Enable	CLKO Enabled	20	CLKE
CLKO Frequency Selection	Full Rate (= f_{SCLK})	20	CLKD
Digital Filter Roll-Off Control	Sharp Roll-Off	20	FLT[1:0]
4x/8x Digital Interpolation Control	8x Interpolation	20	X4DS
Read Register Index Control	REG[6:0] = 01_H	21	REG[6:0]
Read Auto-Increment Control	Auto-Increment Disabled	21	INC

TABLE II. User-Programmable Mode Controls.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 17	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
Register 18	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	OVER	res	INZD	ATLD	ATTS	MUT2	MUT1
Register 19	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	DMF1	DMF0	DM12	res	res	DAC2	DAC1
Register 20	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	X4DS	FLT1	FLT0	CLKD	CLKE	FMT2	FMT1	FMT0
Register 21	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0

TABLE III. Mode Control Register Map.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 17	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

ATx[7:0] **Digtial Attenuation Level Setting**

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

These bits are Read/Write.

Default Value: $1111\ 1111_B$

Each DAC output ($V_{OUT}L$ and $V_{OUT}R$) has a digital attenuator associated with it. The attenuator may be set from 0dB to –63dB, in 0.5dB steps. Alternately, the attenuator may be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. However, the data load control (ATLD bit of Control Register 18) is common to both attenuators. ATLD must be set to '1' in order to change an attenuator's setting. The attenuation level may be set using the following formula:

$$\text{Attenuation Level (dB)} = 0.5\text{dB} \bullet (\text{ATx}[7:0]_{DEC} - 255)$$

Where: $\text{ATx}[7:0]_{DEC} = 0$ through 255

For: $\text{ATx}[7:0]_{DEC} = 0$ through 128, the attenuator is set to infinite attenuation.

The following table shows attenuator levels for various settings:

ATx[7:0]	Decimal Value	Attenuator Level Setting
$1111\ 1111_B$	255	0dB, No Attenuation (default)
$1111\ 1110_B$	254	–0.5dB
$1111\ 1101_B$	253	–1.0dB
•	•	•
•	•	•
•	•	•
$1000\ 0010_B$	130	–62.5dB
$1000\ 0001_B$	129	–63.0dB
$1000\ 0000_B$	128	Mute
•	•	•
•	•	•
•	•	•
$0000\ 0000_B$	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	OVER	res	INZD	ATLD	ATTS	MUT2	MUT1

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

MUTx **Soft Mute Control**

Where, x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

These bits are Read/Write.

Default Value: 0

MUTx = 0	Mute Disabled (default)
MUTx = 1	Mute Enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the Soft Mute function for the corresponding DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. The Soft Mute function is incorporated into the digital attenuators. When Mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When Mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output will be decremented from the current setting to the infinite attenuation, one attenuator step (0.5dB) at a time, with the rate of change programmed by the ATTS bit. This provides ‘pop-free’ muting of the DAC output.

By setting MUTx = 0, upon returning from Soft Mute, the attenuator will be incremented one step at a time to the previously-programeed attenuator level.

ATTS **Attenuation Rate Select**

This bit is Read/Write.

Default Value: 0

ATTS = 0	Attenuation rate is $2/f_S$ (default)
ATTS = 1	Attenuation rate is $4/f_S$

Changes in attenuator levels are made by incrementing or decrementing the attenuator by one step (0.5dB) for every $2/f_S$ or $4/f_S$ time interval until the programmed attenuator setting is reached. This helps to minimize audible ‘clicking’, or zipper noise while the attenuator is changing levels. The ATTS bit allows the user to select the rate at which the attenuator is decremented/incremented during level transitions.

ATLD **Attenuation Control**

This bit is Read/Write.

Default Value: 0

ATLD = 0	Attenuator Disabled (default)
ATLD = 1	Attenuator Enabled

The ATLD bit must be set to logic ‘1’ in order for the attenuators to function. Setting ATLD to logic ‘0’ will disable the attenuator function and cause the current attenuator data to be lost.

Set ATLD = 1 immediately after reset.

Register 18 (cont.)

INZD **Infinite Zero Detect Mute Control**

This bit is Read/Write.

Default Value: 0

INZD = 0	Infinite Zero Detect Mute Disabled (default)
INZD = 1	Infinite Zero Detect Mute Enabled

The INZD bit is used to enable or disable the Zero Detect Mute function described in the Zero Flag and Infinite Zero Detect Mute section in this data sheet. The Zero Detect Mute function is independent of the Zero Flag output operation, so enabling or disabling the INZD bit has no effect on the Zero Flag outputs (ZEROL and ZEROR).

OVER **Oversampling Rate Control**

This bit is Read/Write.

Default Value: 0

OVER = 0	64x Oversampling (default)
OVER = 1	128x Oversampling

Sets the oversampling rate of the delta-sigma modulator. The 128x setting can only be used for sampling frequencies up to 96kHz. The 64x setting must be used for sampling frequencies greater than 96kHz.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 19	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	DMF1	DMF0	DM12	res	res	DAC2	DAC1

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

DACx **DAC Operation Control**

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) or $V_{OUT}R$ (x = 2).

These bits are Read/Write.

Default Value: 0

DACx = 0	DAC Operation Enabled (default)
DACx = 1	DAC Operation Disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. When DACx = 0, the corresponding output will generate the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output will be set to the bipolar zero level, or $V_{CC}/2$.

DM12 **Digital De-Emphasis Function Control**

This bit is Read/Write.

Default Value: 0

DM12 = 0	De-Emphasis Disabled (default)
DM12 = 1	De-Emphasis Enabled

The DM12 bit is used to enable or disable the digital de-emphasis function. Refer to the plots shown in the Typical Performance Curves section of this data sheet.

DMF[1:0] **Sampling Frequency Selection for the De-Emphasis Function**

These bits are Read/Write.

Default Value: 00_B

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled.

DMF[1:0]	De-Emphasis Same Rate Selection
00	44.1kHz (default)
01	48kHz
10	32kHz
11	Reserved

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 20	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	X4DS	FLT1	FLT0	CLKD	CLKE	FMT2	FMT1	FMT0

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.
When R/W = 1, a Read operation is performed.
Default Value: 0

FMT[2:0] **Audio Interface Data Format**

These bits are Read/Write.
Default Value: 000_B

The FMT[2:0] bits are used to select the data format for the serial audio interface. The table below shows the available format options.

FMT[2:0]	Audio Data Format Selection
000	24-Bit Standard Format, Right-Justified Data (default)
001	20-Bit Standard Format, Right -Justified Data
010	18-Bit Standard Format, Right-Justified Data
011	16-Bit Standard Format, Right-Justified Data
100	I2S Format, 16 to 24 Bits
101	Right-Justified Format, 16 to 24 Bits
110	Reserved
111	Reserved

CLKE **CLKO Output Enable**

This bit is Read/Write.
Default Value: 0

CLKE = 0	CLKO Enabled (default)
CLKE = 1	CLKO Disabled

The CLKE bit is used to enable or disable the system clock output pin, CLKO. When CLKO is enabled, it will output either a full or half rate clock, based upon the setting of the CLKD bit. When CLKO is disabled, it is set to a high impedance state.

CLKD **CLKO Frequency Selection**

This bit is Read/Write.
Default Value: 0

CKLD = 0	Full Rate, $f_{CLKO} = f_{SCLK}$ (default)
CKLD = 1	Half Rate, $f_{CLKO} = f_{SCLK}/2$

The CLKD bit is used to select the clock frequency for the CLKO pin.

FLT[1:0] Digital Filter Roll-Off Control

These bits are Read/Write.

Default Value: 00_B

FLT[1:0] = 00_B	Sharp Roll-Off (default)
FLT[1:0] = 01_B	Slow Roll-Off 1
FLT[1:0] = 10_B	Slow Roll-Off 2

Bits FLT[1:0] allow the user to select the digital filter roll-off that is best suited to their application. Three filter roll-off selections are available: Sharp, Slow 1, and Slow 2

The filter responses for these selections are shown in the Typical Performance Curves section of this data sheet. Slow roll-off performance is specified for 8x interpolation (X4DS = 0) only.

X4DS 4x/8x Digital Interpolation Control

This bit is Read/Write.

Default Value: 0

X4DS = 0	8x Interpolation (default)
X4DS = 1	4x Interpolation, used for f_S = 192kHz or 176.4kHz

Bit X4DS allows the user to select the oversampling rate of the digital interpolation filter. For sampling frequencies up to 96kHz, 8x interpolation is used, while 4x interpolation is used for 192kHz and 176.4kHz sampling frequencies.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 21	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

INC **Auto-Increment Read Control**

This bit is Read/Write.

Default Value: 0

INC = 0	Auto-Increment Read Disabled (default)
INC = 1	Auto-Increment Read Enabled

The INC bit is used to enable or disable the Auto-Increment Read feature of the Serial Control Interface. Refer to the Serial Control Interface section of this data sheet for details regarding Auto-Increment Read operation.

REG[6:0] **Read Register Index**

These bits are Read/Write.

Default Value: 01_H

Bits REG[6:0] are used to set the index of the register to be read when performing a Single Register Read operation. In the case of an Auto-Increment Read operation, bits REG[6:0] indicate the index of the last register to be read in the in the Auto-Increment Read sequence. For example, if Registers 1 through 6 are to be read during an Auto-Increment Read operation, bits REG[6:0] would be set to 06_H.

Refer to the Serial Control Interface section of this data sheet for details regarding the Single Register and Auto-Increment Read operations.

ANALOG OUTPUTS

The PCM1737 includes two independent output channels: $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 3.1Vp-p typical into a 5kΩ AC-coupled load (V_{CC} = +5V). The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are DC biased to a DC common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1737's delta-sigma D/A converters. The frequency response of this filter is shown in Figure 11. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

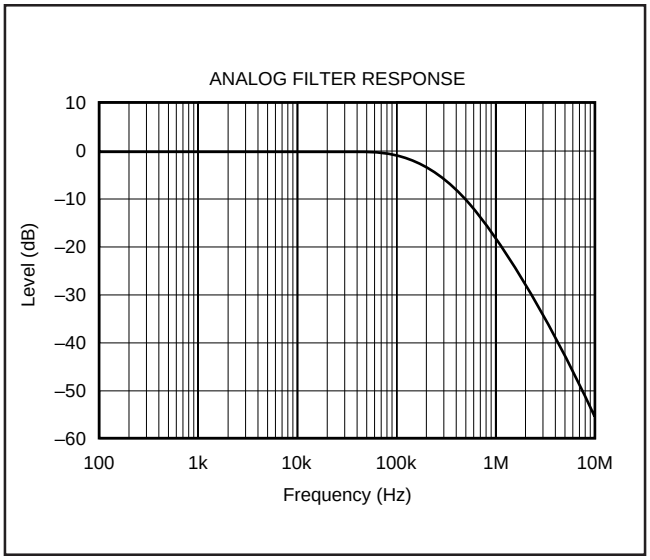


FIGURE 11. Output Filter Frequency Response.

$V_{COM}L$ AND $V_{COM}R$ OUTPUTS

Two unbuffered common-mode voltage output pins, $V_{COM}L$ (pin 17) and $V_{COM}R$ (pin 12), are brought out for decoupling purposes. These pins are nominally biased to a DC voltage level equal to $V_{CC}/2$. These pins may be used to bias external circuits, a voltage follower is required for buffering purposes. Figure 12 shows an example of using the $V_{COM}L$ and $V_{COM}R$ pins for external biasing applications.

ZERO FLAG AND INFINITE ZERO DETECT MUTE FUNCTIONS

The PCM1737 includes circuitry for detecting an all '0' data condition for the data input pin, DATA. This includes two independent functions: Zero Output Flags and Zero Detect Mute. Although the flag and mute functions are independent of one another, the zero detection mechanism is common to both functions.

Zero Detect Condition

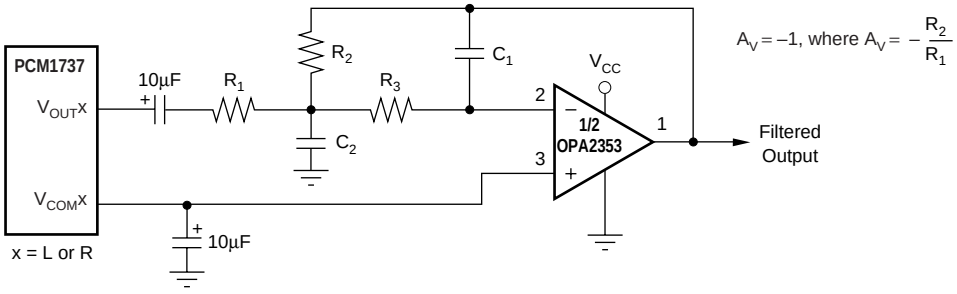
Zero Detection for each output channel is independent from the other. If the data for a given channel remains at a '0' level for 1024 sample periods (or LRCK clock periods), a Zero Detect condition exists for that channel.

Zero Output Flags

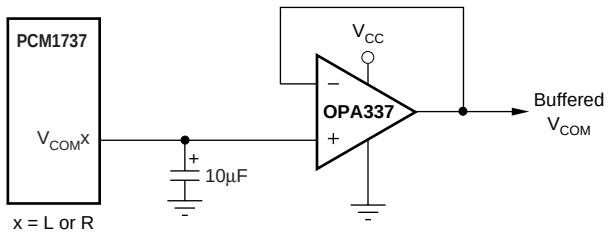
Given that a Zero Detect condition exists for one or more channels, the Zero flag pins for those channels will be set to a logic '1'state. There are Zero Flag pins for each channel, ZEROL (pin 23) and ZEROR (pin 24). These pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally-controlled functions.

Infinite Zero Detect Mute

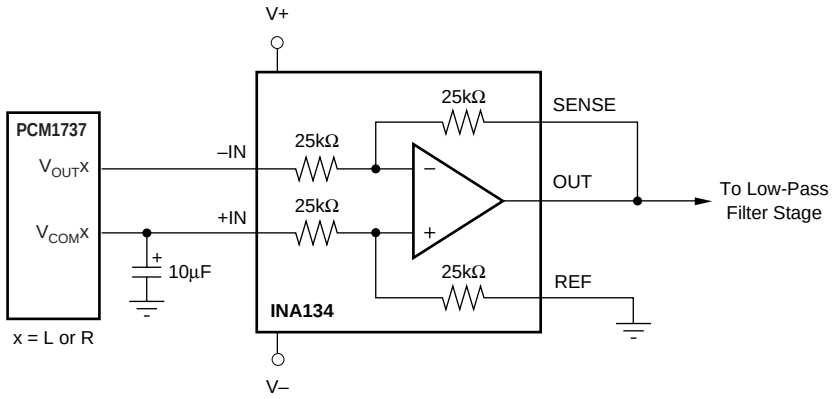
Infinite Zero Detect Mute is an internal logic function. The Zero Detect Mute can be enabled or disabled using the INZD bit of Control Register 18. The reset default is Zero Detect Mute disabled, INZD = 0. Given that a Zero Detect Condition exists for one or more channels, the zero mute circuitry will immediately force the corresponding DAC output(s) to the bipolar zero level, or $V_{CC}/2$.



(a) Using V_{COM} to Bias a Single-Supply Filter Stage



(b) Using a Voltage Follower to Buffer V_{COM} when Biasing Multiple Nodes



(c) Using an INA134 for DC-Coupled Output

FIGURE 12. Biasing External Circuits Using the $V_{COM}1$ and $V_{COM}2$ Pins.

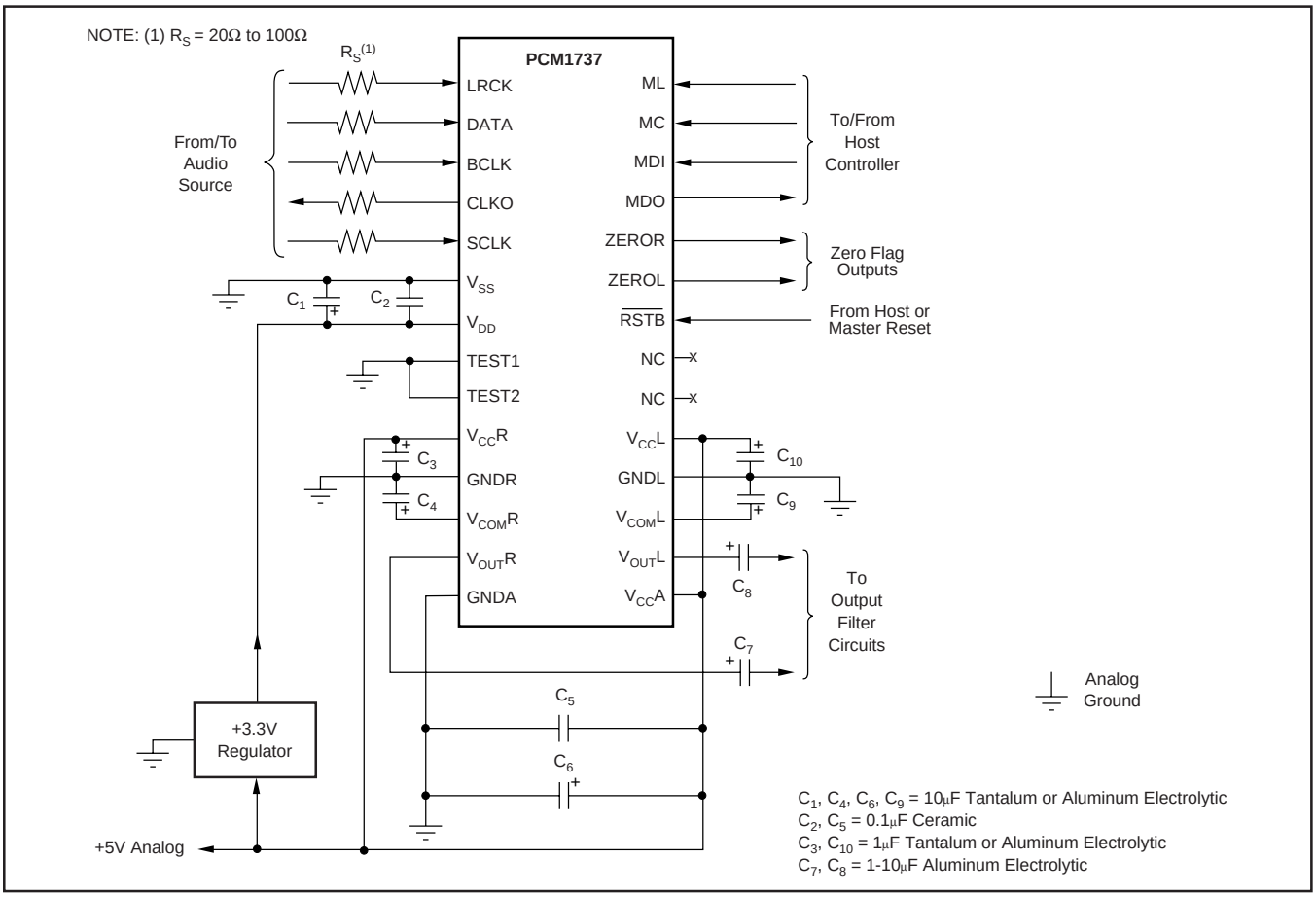


FIGURE 13. Basic Connection Diagram.

APPLICATIONS INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 13, with the necessary power supply bypassing and decoupling components. Burr-Brown recommends using the component values shown in Figure 13 for all designs.

The use of series resistors (22Ω to 100Ω) are recommended for SCLK, LRCK, BCLK, DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter which reduces high frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

POWER SUPPLIES AND GROUNDING

The PCM1737 requires a +5V analog supply and a +3.3V digital supply. The +5V supply is used to power the DAC analog and output filter circuitry, while the +3.3V supply is used to power the digital filter and serial interface circuitry. For best performance, the +3.3V supply should be derived from the +5V supply using a linear regulator, as shown in Figure 13. Burr-Brown's REG1117-3.3 is an ideal choice for this application.

Proper power supply bypassing is shown in Figure 13. The bypass capacitors should be tantalum or aluminum electrolytic, while the 0.1μF capacitors are ceramic (X7R type is recommended for surface-mount applications).

D/A OUTPUT FILTER CIRCUITS

Delta-sigma D/A converters utilize noise-shaping techniques to improve in-band Signal-to-Noise Ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist Frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figures 12a and 14 show the recommended external low-pass active filter circuits for dual and single-supply applications. These circuits are 2nd-order Butterworth filters using the Multiple Feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please refer to Burr-Brown Applications Bulletin AB-034.

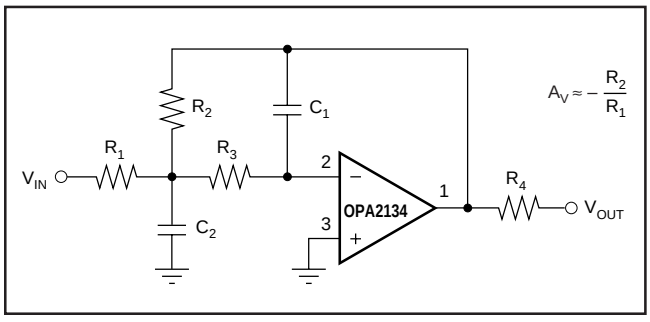


FIGURE 14. Dual-Supply Filter Circuit.

Since the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high quality audio op amps are recommended for the active filters. Burr-Brown's OPA2134 and OPA2353 dual op amps are shown in Figures 12a and 14, and are recommended for use with the PCM1737.

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1600 and PCM1601 is shown in Figure 15. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1737 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1737. In cases where a common +5V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital +5V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 16 shows the recommended approach for single-supply applications.

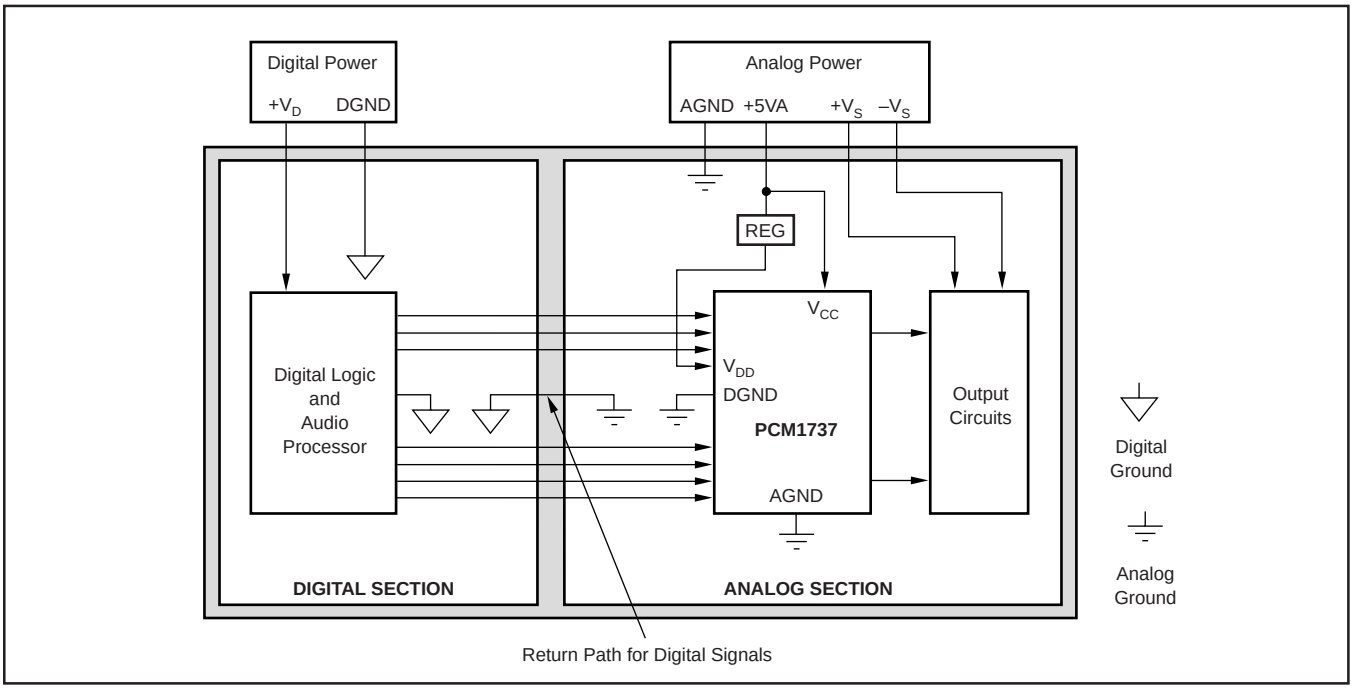


FIGURE 15. Recommended PCB Layout.

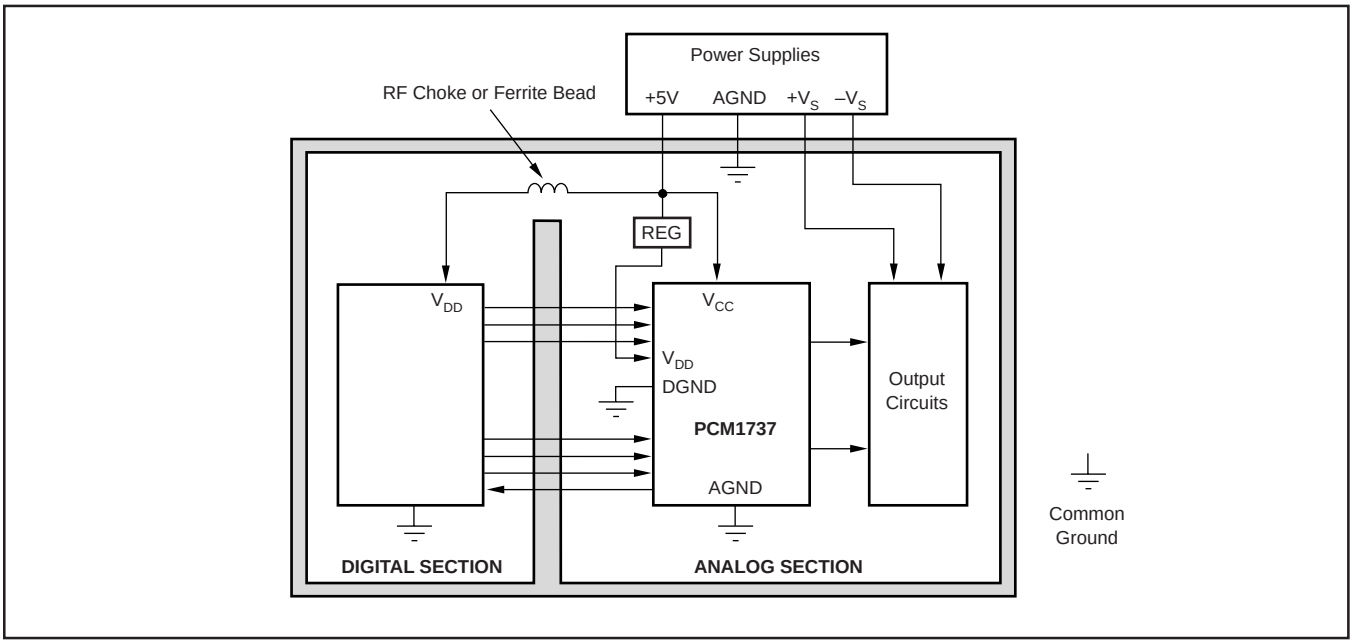


FIGURE 16. Single-Supply PCB Layout.

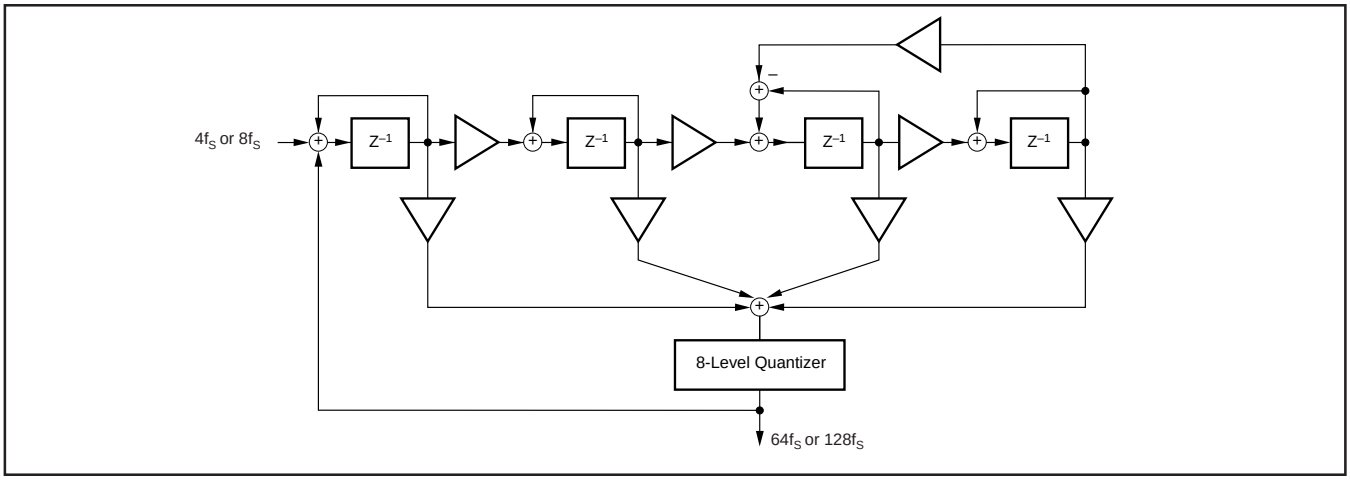


FIGURE 17. Eight-Level Delta-Sigma Modulator.

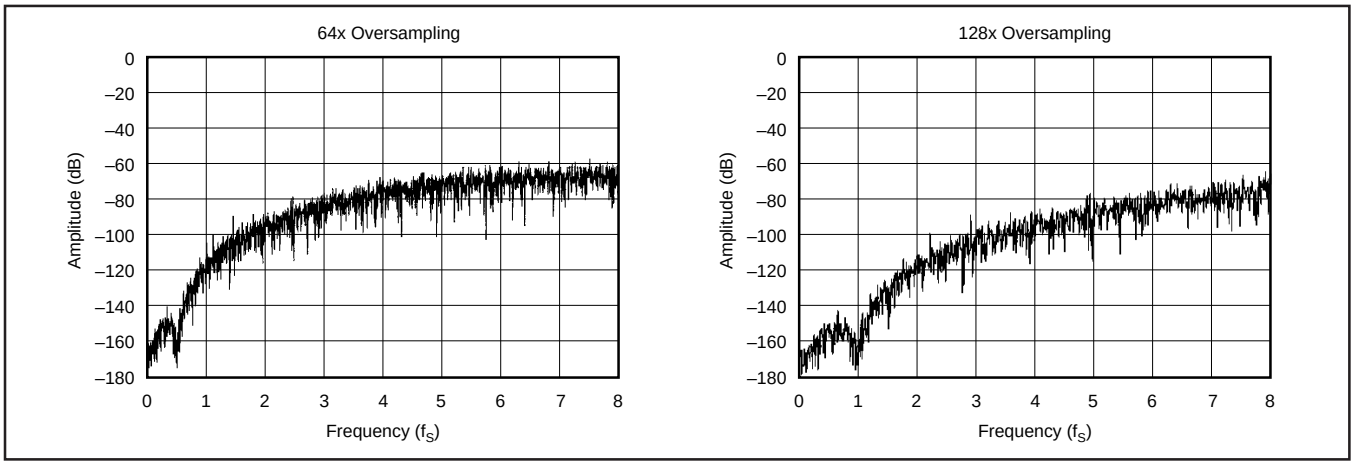


FIGURE 18. Quantization Noise Spectrum (64x/128x oversampling).

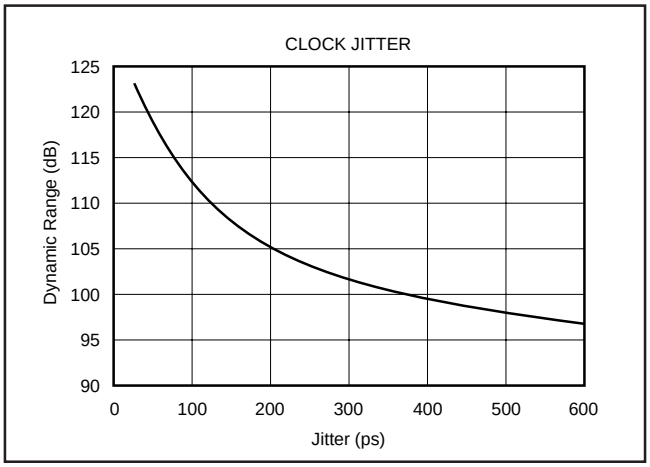


FIGURE 19. Jitter Sensitivity.

THEORY OF OPERATION

The delta-sigma section of PCM1600 is based on a 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 17. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the interpolation filter is $64f_S$ or $128f_S$.

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 18. The enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multi-level quantizer, with the simulated jitter sensitivity shown in Figure 19.

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1737. In all cases, an Audio Precision System Two Cascade or equivalent audio measurement system is utilized to perform the testing.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion + Noise (THD+N) is a significant figure of merit for audio D/A converters since it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N.

For the PCM1737, THD+N is measured with a full scale, 1kHz digital sine wave as the test stimulus at the input of the

DAC. The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1kHz, 96kHz, or 192kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1737 demo board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurment system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

DYNAMIC RANGE

Dynamic range is specified as A-Weighted, THD+N measured with a –60dBFS, 1kHz digital sine wave stimulus at the input of the D/A converter. This measurement is designed to give a good indicator of how the DAC will perform given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 21, and is similar to the THD+N test setup discussed previously. The differences include the bandlimit filter selection, the additional A-Weighting filter, and the –60dBFS input level.

IDLE CHANNEL SIGNAL-TO-NOISE RATIO

The SNR test provides a measure of the noise floor of the D/A converter. The input to the D/A is all 0's data, and the D/A converter's Infinite Zero Detect Mute function must be disabled (default condition at power up for the PCM1737). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and effect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all '0's data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level. (see the notes provided in Figure 21).

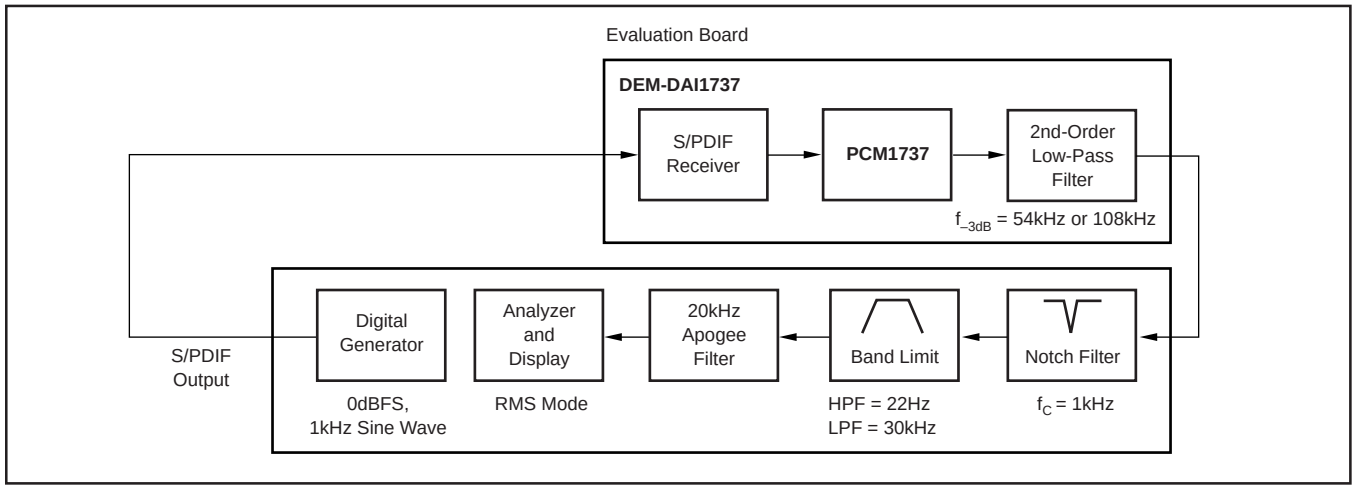


FIGURE 20. Test Setup for THD+N Measurement.

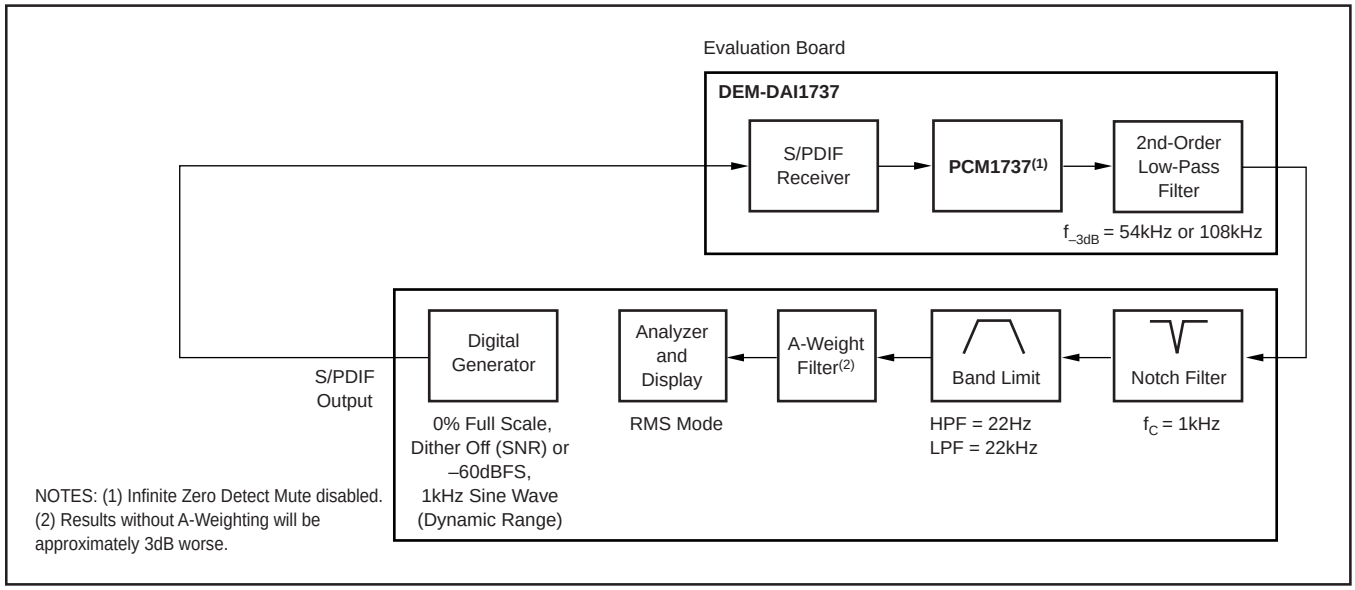


FIGURE 21. Test Set-Up for Dynamic Range and SNR Measurements.