INTEGRATED CIRCUITS

DATA SHEET

PCK2509SA
50–150 MHz 1:9 SDRAM clock driver

Product specification 2000 Dec 01

ICL03 — PC Motherboard ICs; Logic Products Group

Philips Semiconductors

PHILIPS

FEATURES

- Phase-Locked Loop Clock distribution for PC100/PC133 SDRAM applications
- JEDEC compliant operation—PLL reamins locked when outputs are disabled.
- See PCK2509SL for low power version where PLL goes into standby when outputs are disabled..
- Spread Spectrum clock compatible
- Operating frequency 50 to 150 MHz
- ($t_{phase\ error}$ – jitter) at 100 to133 MHz = ±50 ps
- Jitter (peak-peak) at 100 to 133 MHz = ± 80 ps
- Jitter (cycle-cycle) at 100 to 133 MHz = 65 ps
- Pin-to-pin skew < 200 ps
- Available in plastic 24-Pin TSSOP
- Distributes one clock input to one bank of five outputs and one bank of four outputs
- External Feedback (FBIN) terminal Is used to synchronize the outputs to the clock input
- On-Chip series damping resistors
- No external RC network required
- Operates at 3.3 V
- Inputs compatible with 2.5 V and 3.3 V ranges
- See page 7 for Characteristic curves

DESCRIPTION

The PCK2509SA is a high-performance, low-skew, low-jitter, phase-locked loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The PCK2509SA operates at 3.3 V V_{CC} and is input compatible with both 2.5 V and 3.3 V input voltage ranges. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

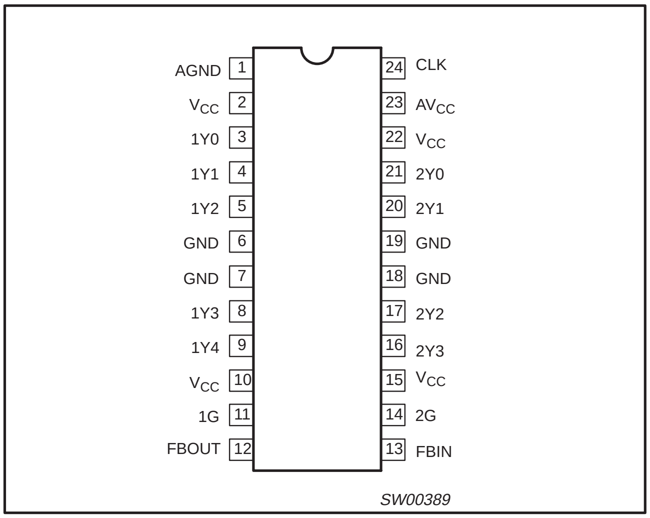
One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic–low state.

Unlike many products containing PLLs, the PCK2509SA does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the PCK2509SA requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, and following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

The PCK2509SA is characterized for operation from 0°C to +70°C.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic TSSOP	0 °C to +70 °C	PCK2509SADH	SOT355-1

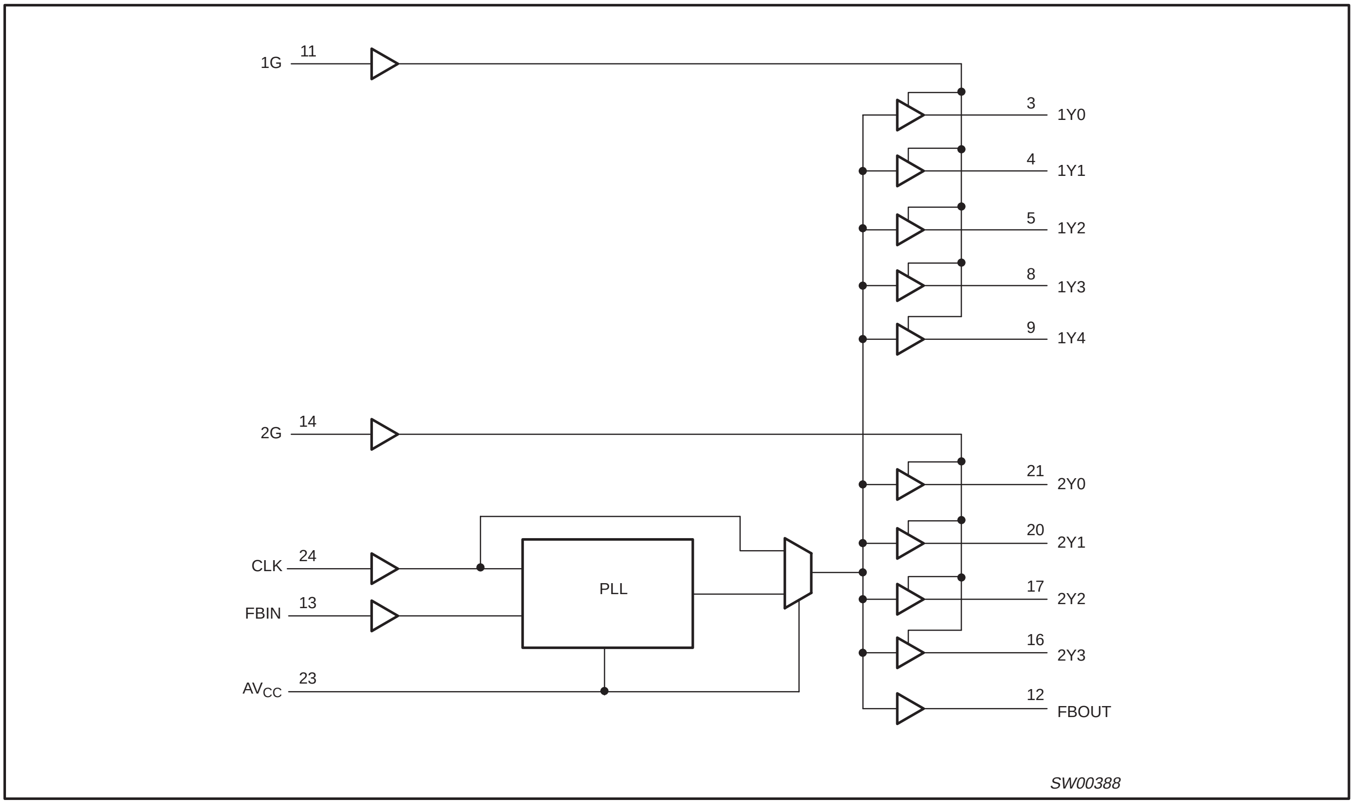
PIN DESCRIPTIONS

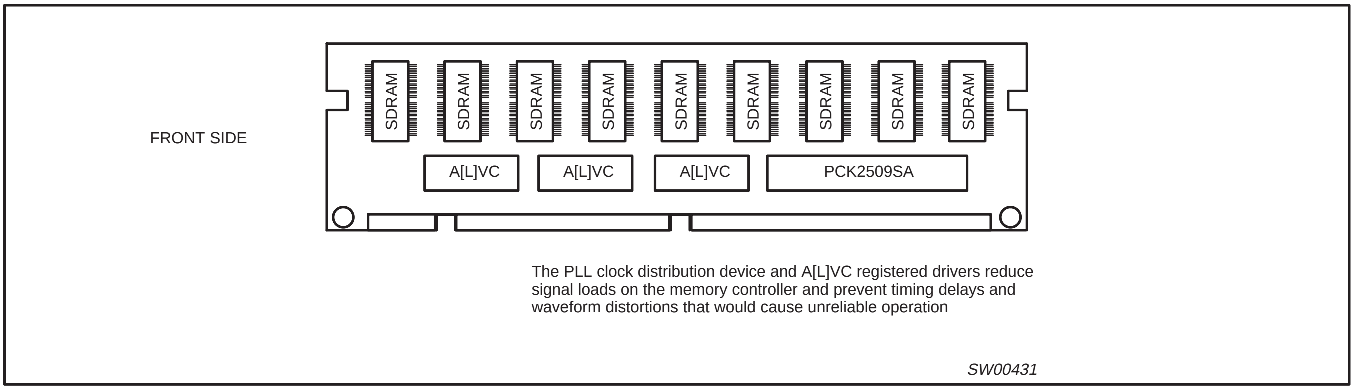
PIN NUMBER	SYMBOL	TYPE	NAME, FUNCTION, and DIRECTION
1	AGND	GND	**Analog ground.** AGND provides the ground reference for the analog circuitry.
2, 10, 15, 22	V_{CC}	PWR	**Power supply**
3, 4, 5, 8, 9	1Y (0–4)	OUT	**Clock outputs.** These outputs provide low-skew copies of CLK. Output bank 1Y(0–4) is enabled via the1G input. These outputs can be disabled to a logic LOW state by de-asserting the 1G control input. Each output has an integrated 25 Ω series-damping resistor.
6, 7, 18, 19	GND	GND	**Ground**
11	1G	IN	**Output bank enable.** 1G is the output enable for outputs 1Y(0–4). When 1G is LOW, outputs 1Y(0–4) are disabled to a logic LOW state. When 1G is HIGH, all outputs 1Y(0–4) are enabled and switch at the same frequency as CLK.
12	FBOUT	OUT	**Feedback output.** FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25 Ω series-damping resistor.
13	FBIN	IN	**Feedback input.** FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
14	2G	IN	**Output bank enable.** 2G is the output enable for outputs 2Y(0–3). When 2G is LOW, outputs 2Y(0–3) are disabled to a logic LOW state. When 2G is HIGH, all outputs 2Y(0–3) are enabled and switch at the same frequency as CLK.
16, 17, 20, 21	2Y (0–3)	OUT	**Clock outputs.** These outputs provide low-skew copies of CLK. Output bank 2Y(0–3) is enabled via the 2G input. These outputs can be disabled to a logic LOW state by de-asserting the 2G control input. Each output has an integrated 25 Ω series-damping resistor.
23	AV_{CC}	PWR	**Analog power supply.** AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
24	CLK	IN	**Clock input.** CLK provides the clock signal to be distributed by the PCK2509SA clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.

FUNCTION TABLE

INPUTS			OUTPUTS		
1G	**2G**	**CLK**	**1Y (0–4)**	**2Y (0–3)**	**FBOUT**
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
AV_{CC}	Supply voltage range	Note 2		$< V_{CC} + 0.7$	V
V_{CC}	Supply voltage range		–0.5	+4.6	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
V_I	Input voltage range	Note 3	–0.5	6.5	V
I_{OK}	Output clamp current	$V_O > V_{CC}$ or $V_O < 0$		±50	mA
V_O	Output voltage range	Notes 3, 4	–0.5	$V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}		±50	mA
T_{STG}	Storage temperature range		–65	+150	°C
P_{TOT}	Power dissipation per package			700	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. AV_{CC} must not exceed V_{CC}
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. This value is limited to 4.6 V maximum.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}, AV_{CC}	Supply voltage		3	3.6	V
V_{IH}	HIGH level input voltage		2		V
V_{IL}	LOW level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

NOTE:
1. Unused inputs must be held high or low to prevent them from floating.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
		AV_{CC}, V_{CC} (V)	OTHER	MIN	TYP	MAX	
V_{IK}	Input clamp voltage	3	$I_I = –18mA$			–1.2	V
V_{OH}	HIGH level output voltage	MIN to MAX	$I_{OH} = – 100\mu A$	$V_{CC} – 0.2$			V
		3	$I_{OH} = – 12mA$	2.1			
		3	$I_{OH} = – 6mA$	2.4			
V_{OL}	LOW level output voltage	MIN to MAX	$I_{OL} = 100\mu A$	–		0.2	V
		3	$I_{OL} = 12mA$	–		0.8	
		3	$I_{OL} = 6mA$	–		0.55	
I_I	Input current	3.6	$V_I = V_{CC}$ or GND			±5	µA
I_{CC} [1]	Quiescent supply current	3.6	$V_I = V_{CC}$ or GND; $I_O = 0$, outputs: LOW or HIGH			10	µA
ΔI_{CC}	Additional supply current per input pin	3.3 to 3.6	One input at $V_{CC} – 0.6V$; other inputs at V_{CC} or GND			500	µA
C_I	Input capacitance	3.3	$V_I = V_{CC}$ or GND		2.8		pF
C_O	Output capacitance	3.3	$V_O = V_{CC}$ or GND		5.4		pF

NOTE:
1. For I_{CCA} and I_{CC} vs. Frequency, see Figures 1 and 2.

TIMING REQUIREMENTS

Over recommended ranges of supply voltage and operating free-air temperature.

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{CLK}	Clock frequency	50	150	MHz
	Input clock duty cycle	40	60	%
	Stabilization time[1]		1	ms

NOTE:

1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

SWITCHING CHARACTERISTICS

Over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF

PARAMETER	FROM (INPUT)/CONDITION	TO (OUTPUT)	V_{CC}, AV_{CC} = 3.3 V ±0.3 V			UNIT
			MIN	TYP	MAX	
$t_{phase\ error}$ [2]	CLKIN↑ = 100 MHz to 133 MHz	FBIN↑	–100		100	ps
	CLKIN↑ = 66 MHz		–125		125	ps
$t_{phase\ error}$, – jitter [1, 3]	CLKIN↑ = 100 MHz to 133 MHz	FBIN↑	–50		50	ps
$t_{SK(0)}$ [4]	Any Y or FBOUT	Any Y or FBOUT			200	ps
$jitter_{(peak\text{-}peak)}$	CLKIN = 66 MHz to 133 MHz	Any Y or FBOUT	–80		80	ps
$jitter_{(cycle\text{-}cycle)}$ [1]				|65|		
Duty cycle reference [1]	F(CLKIN > 60 MHz)	Any Y or FBOUT	47		53	%
t_r [1]	V_O = 0.4 to 2 V	Any Y or FBOUT	2.5		1	V/ns
t_f [1]	V_O = 0.4 to 2 V	Any Y or FBOUT	2.5		1	V/ns

NOTES:

1. These parameters are not production tested.
2. This is considered as static phase offset.
3. Phase error does not include jitter. ($t_{phase\ error}$ = static $t_{phase\ error}$ – $jitter_{(cycle\text{-}cycle)}$).
4. The $t_{SK(0)}$ specification is only valid for outputs with equal loading.

CHARACTERISTIC CURVES

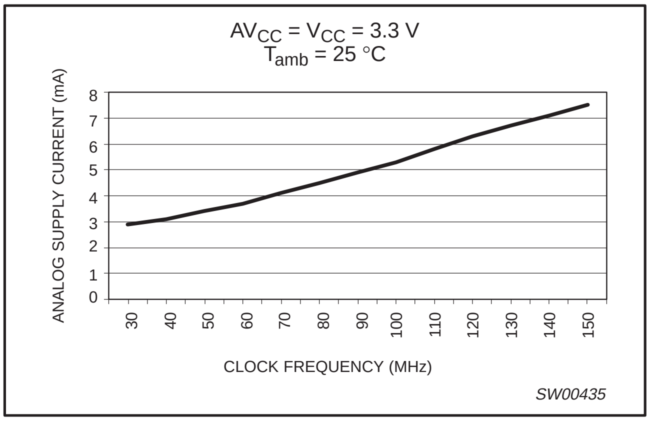


Figure 1. Analog supply current vs. clock frequency

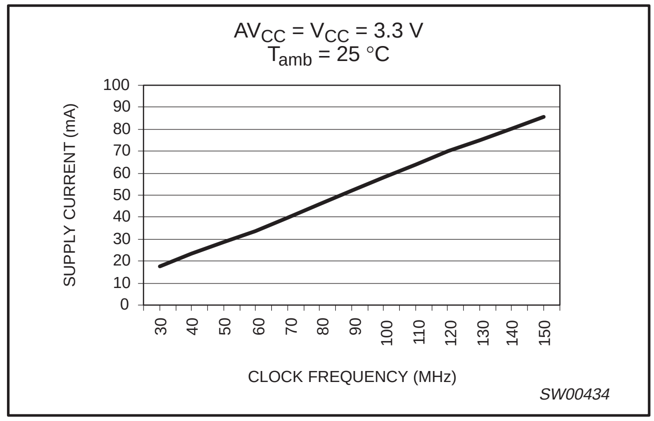


Figure 2. Supply current vs. clock frequency

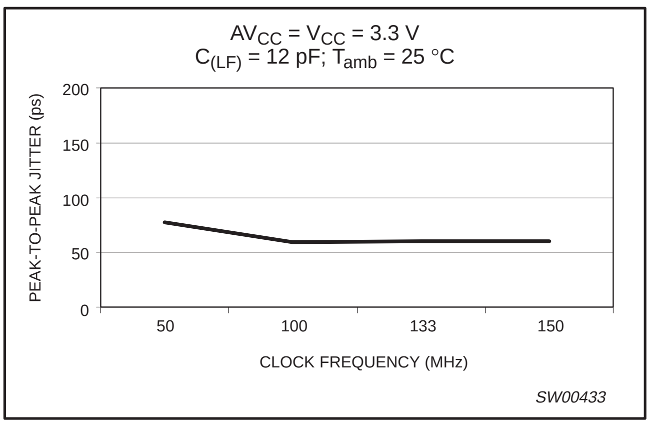


Figure 3. Peak-to-peak jitter vs. clock frequency

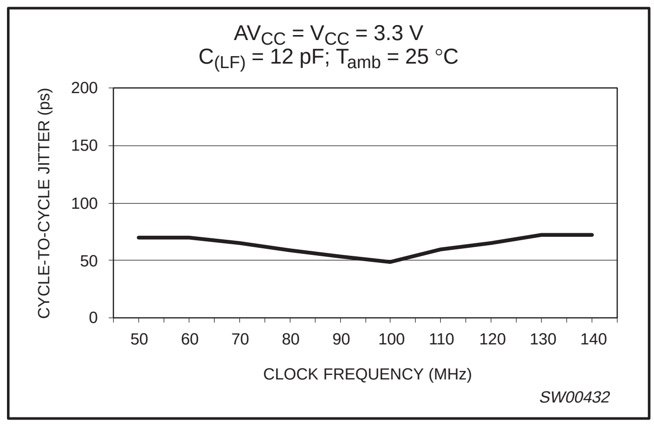


Figure 4. Cycle-to-cycle jitter vs. clock frequency

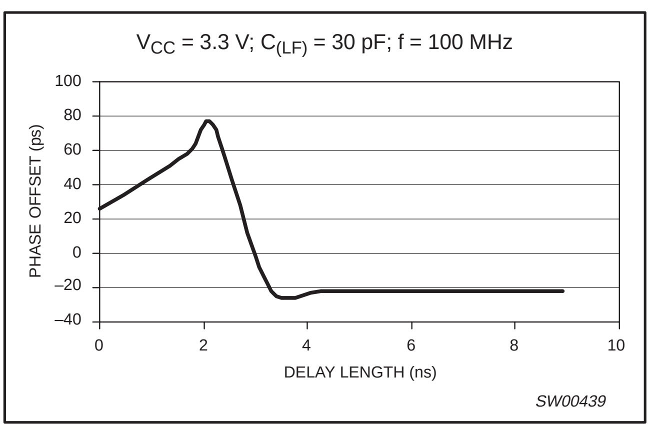
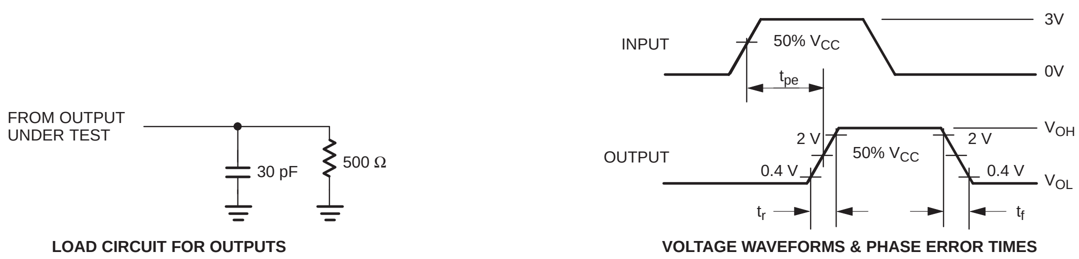


Figure 5. Phase offset vs. delay length

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω , t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
3. The outputs are measured one at a time with one transition per measurement.

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Figure 6. Load Circuit and Voltage Waveforms

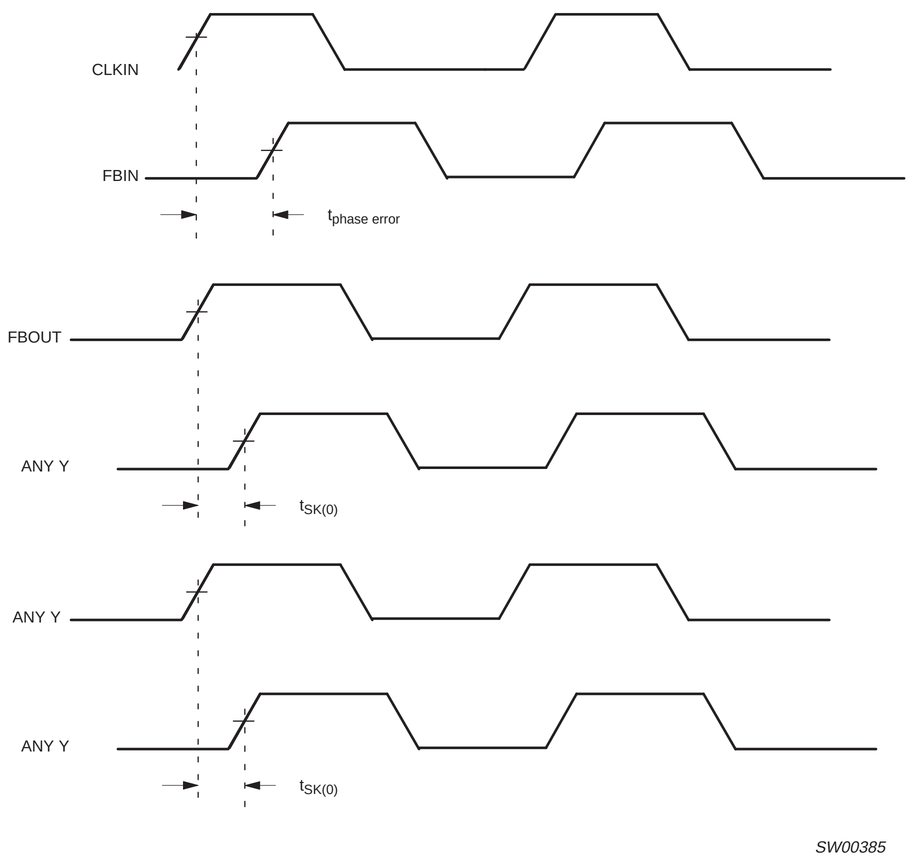
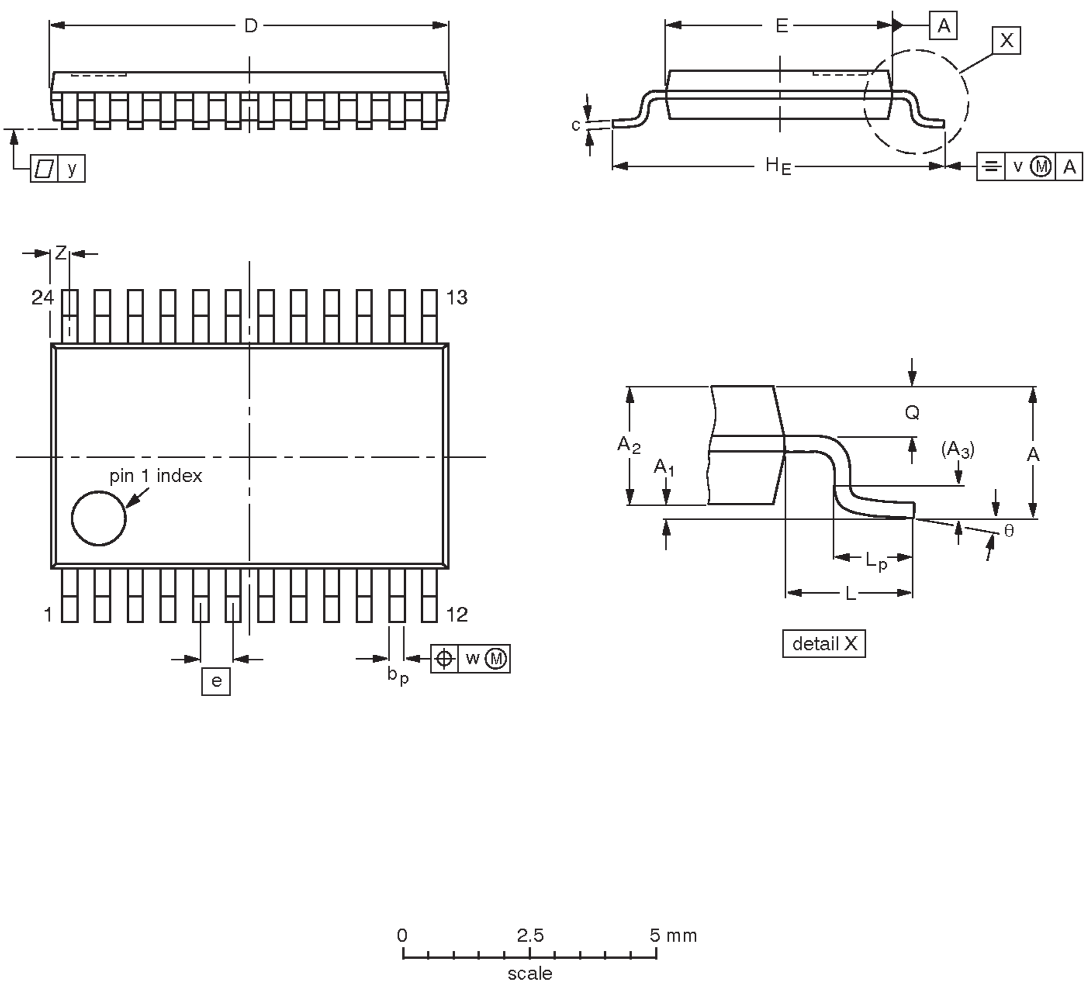


Figure 7. Phase Error and Skew Calculations

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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