DATA SHEET

PCF8820

67 × 101 Grey-scale/ECB colour dot matrix LCD driver

Product specification
File under Integrated Circuits, IC12

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Philips
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CONTENTS

67 × 101 Grey-scale/ECB colour dot matrix LCD driver

PCF8820

1 FEATURES

- Single-chip LCD controller and driver for grey-scale/ Electrically Controlled Birefringence (ECB) colour
- 4 grey levels/colours (2-bit) definable from 64 levels
- 67 row and 101 column outputs
- Display data RAM 67 × 101 × 2-bit with linear RAM addressing
- Partial screen mode with reduced current consumption (8 rows at top or bottom of display)
- On-chip:
  - Generation of LCD supply voltage (V_{LCDOUT}); external supply also possible
  - Configurable voltage multiplier factor of 8, 7, 6, 5, 4, 3 or 2; direct drive also possible
  - Selectable linear temperature compensation of V_{LCDOUT}
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components; external clock also possible.
- Temperature read-out
- Fast mode I²C-bus interface (400 kbits/s)
- Frame frequency calibration via software
- Software selectable bias configuration
- Compatible with 4-bit, 8-bit or 16-bit microcontrollers
- Multiplex rates of 1 : 67 or 1 : 8
- Logic supply voltage range from 2.5 to 5.5 V (V_{DD1} to V_{SS1})
- High voltage generator supply voltage range from 2.7 to 5.5 V (V_{DD2} to V_{SS1} and V_{DD3} to V_{SS2})
- Bias voltage generator supply voltage range (V_{LCDIN} to V_{SS1}):
  - From 7 to 14.5 V at a multiplex rate of 1 : 67
  - From 4.5 to 14.5 V in partial screen mode at a multiplex rate of 1 : 8.
- Low power consumption, suitable for battery operated systems
- Slim chip layout, suitable for chip-on-glass applications
- Software selectable top and bottom row swap for adapting driver to different glass-layouts
- CMOS compatible inputs
- Manufactured in silicon gate CMOS process.

2 APPLICATIONS

- Mobile telecommunication systems
- Battery powered equipment
- Point of sale terminals
- Instrumentation
- Automotive information systems.

3 GENERAL DESCRIPTION

The PCF8820 is a low power CMOS LCD row/column driver, designed to drive grey-scale/ ECB colour dot matrix graphic displays at a multiplex rate of 1 : 67. In the partial screen mode, only 8 rows are driven at a multiplex rate of 1 : 8.

This chip provides all the necessary display functions, including on-chip generation of the LCD supply voltage and LCD bias voltages. Consequently, fewer external components are required and the power consumption is low.

The PCF8820 interfaces with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). All inputs are CMOS compatible.

Remark: the waveform generation for ECB colour is identical to that used for grey-scale.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8820U	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

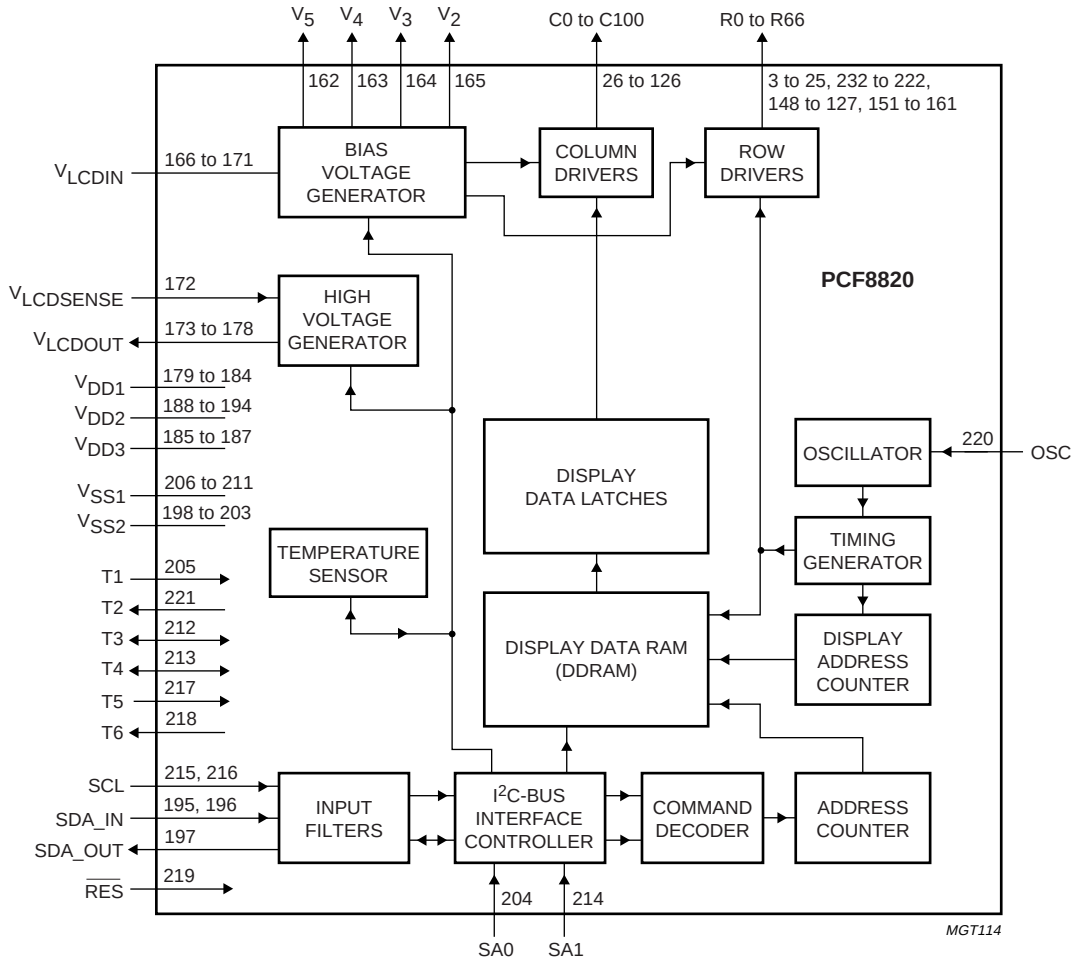


Fig.1 Block diagram.

6 PINNING

6.1 Pad configuration

SYMBOL	PAD	DESCRIPTION
R0 to R22	3 to 25	LCD row driver outputs (block 1)
R23 to R33	232 to 222	LCD row driver outputs (block 2)
R34 to R55	148 to 127	LCD row driver outputs (block 3)
R56 to R66	151 to 161	LCD row driver outputs (block 4)
C0 to C100	26 to 126	LCD column driver outputs
V_{SS1}	206 to 211	ground supply 1
V_{SS2}	198 to 203	ground supply 2
V_{DD1}	179 to 184	supply voltage 1 of logic
V_{DD2}	188 to 194	supply voltage 2 of high voltage generator; temperature read-out
V_{DD3}	185 to 187	supply voltage 3 of high voltage generator; temperature read-out
V_{LCDOUT}	173 to 178	voltage multiplier output
$V_{LCDSENSE}$	172	voltage multiplier regulation input
V_{LCDIN}	166 to 171	supply voltage for LCD (bias voltage generator)
V_2	165	LCD intermediate bias voltage 2; for test purposes only
V_3	164	LCD intermediate bias voltage 3; for test purposes only
V_4	163	LCD intermediate bias voltage 4; for test purposes only
V_5	162	LCD intermediate bias voltage 5; for test purposes only
SDA_IN	195 and 196	serial data input
SDA_OUT	197	serial data output (acknowledge)
SCL	215 and 216	serial clock input
SA0	204	I^2C-bus slave address input 0 (bit 0)
SA1	214	I^2C-bus slave address input 1 (bit 1)
OSC	220	oscillator signal input
$\overline{RES}$	219	external reset input (active LOW)
T1	205	test 1 input
T2	221	test 2 output
T3	212	test 3 I/O
T4	213	test 4 I/O
T5	217	test 5 input
T6	218	test 6 output

The pad configuration is shown in Fig.32.

6.2 Pad functions

6.2.1 Row driver outputs

Row driver outputs (R0 to R66) are the outputs for the LCD row drive signals. They should be connected directly to the 67 rows of the LCD. If less than 67 rows are required, the unused outputs must be left open-circuit.

6.2.2 Column driver outputs

Column driver outputs (C0 to C100) are the outputs for the LCD column drive signals. They should be connected directly to the 101 columns of the LCD. If less than 101 columns are required, the unused column outputs must be left open-circuit.

6.2.3 Ground supply

The ground supply rails (V_{SS1} and V_{SS2}) must be connected together. V_{SS1} is related to V_{DD1} and V_{DD3}; V_{SS2} is related to V_{DD2}.

6.2.4 Supply voltage

The supply voltage rails (V_{DD1}, V_{DD2} and V_{DD3}) must be connected together when the same supply is used for both the logic circuits and for the voltage multiplier. When the circuits are fed separately, V_{DD2} and V_{DD3} must be connected to the same supply.

6.2.5 Voltage multiplier output

V_{LCDOUT} is the output of the voltage multiplier of the high voltage generator.

6.2.6 Voltage multiplier regulation input

$V_{LCDSENSE}$ is the regulation input of the high voltage multiplier and must be connected to V_{LCDOUT}.

6.2.7 Supply voltage of bias voltage generator

V_{LCD} is the supply voltage on pad V_{LCDIN} for the bias voltage generator which supplies the LCD outputs. The voltage on pad V_{LCDIN} must not be lower than V_{DD1}.

If V_{LCD} is generated internally, pad V_{LCDOUT} must be connected to pad V_{LCDIN}.

If V_{LCD} is supplied externally, the external supply voltage must be connected to pad V_{LCDIN}. An external supply voltage must be applied after applying V_{DD1}, and it must be removed before or when removing V_{DD1} (see Fig.25). It is recommended that an external supply voltage is applied after leaving the reset state. The external supply voltage can stay applied in the Power-down mode.

When an external supply voltage is used, pads V_{LCDIN}, $V_{LCDSENSE}$ and V_{LCDOUT} do not have to be connected together. However, if pads $V_{LCDSENSE}$ and V_{LCDOUT} are both connected to pad V_{LCDIN}, the current consumption can be reduced under the following conditions:

- The output of V_{LCDOUT} is set to high-impedance (see Table 8)
- The HIGH voltage programming range is selected by setting bit PRS = 1, the maximum voltage multiplier on factor 8 and the V_{LCD} control register on the maximum value (see Table 2).

6.2.8 LCD intermediate bias voltages

The LCD intermediate bias voltages (V_2, V_3, V_4 and V_5) which are applied to the LCD columns and rows are present on these pads for test purposes. They must be left open-circuit in the application.

6.2.9 Serial data input

SDA_IN is the serial data input from the I^2C-bus.

6.2.10 Serial data output

SDA_OUT is the serial data output (data, acknowledge) for the I^2C-bus. Connecting pad SDA_OUT to pad SDA_IN makes the SDA line fully I^2C-bus compatible.

Not connecting pad SDA_IN to pad SDA_OUT allows the device to be used in applications in which the acknowledge bit is not required. In Chip-On-Glass (COG) applications, it is sometimes beneficial not to connect pad SDA_OUT to pad SDA_IN. This is because in COG applications where the track resistance from pad SDA_OUT to the system SDA line is significant, a voltage divider is created by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. This divider could prevent the PCF8820 from asserting a valid logic 0 level during an acknowledge cycle.

In COG applications, where the acknowledge cycle is required, the track resistance from the pad SDA_OUT to the system SDA line must be minimized to guarantee a valid LOW-level.

6.2.11 Serial clock input

SCL is the serial clock input from the I^2C-bus.

6.2.12 SLAVE ADDRESS INPUTS

These inputs (SA0 and SA1) allow up to four PCF8820 drivers to be controlled on the same I²C-bus. Inputs SA0 and SA1 represent respectively bit 0 and bit 1 of the slave address.

6.2.13 OSCILLATOR SIGNAL INPUT

Pad OSC must be connected directly to V_{DD1} when the on-chip oscillator is used. No external components are required. It should be noted that any voltage drop of V_{DD1} may affect the performance of the on-chip oscillator.

An external clock must be connected to input OSC.

6.2.14 EXTERNAL RESET INPUT

A LOW-level on input $\overline{RES}$ initializes the chip.

6.2.15 TEST PADS

The test pads (T1, T2, T3, T4, T5 and T6) must not be accessible to the user.

Pads T1, T3 and T4 must be connected to V_{SS1}, pad T5 must be connected to V_{DD1}, and pads T2 and T6 must be left open-circuit.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

The on-chip oscillator provides the clock signal for the LCD system. The clock mode is controlled via the I²C-bus interface. A clock signal must always be present, except in the Power-down mode, to prevent the LCD entering a DC state.

7.2 I²C-bus interface controller

The I²C-bus interface controller receives and executes the commands sent via the I²C-bus. The PCF8820 acts as an I²C-bus slave receiver/transmitter and therefore it cannot control the bus communication.

7.3 Input filters

RC low-pass filters are provided on inputs SDA_IN, SCL and $\overline{RES}$ to enhance noise immunity in electrically adverse environments.

7.4 Display Data RAM (DDRAM)

The PCF8820 contains a 67 × 101 × 2-bit static RAM, which stores the display data. The RAM comprises 17 banks of 101 bytes (17 × 101 × 8 bits). Not all of the last bank is implemented. During RAM access, data is transferred to the RAM via the I²C-bus interface controller.

7.5 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the I²C-bus.

7.6 Address counter

The address counter generates write addresses to the DDRAM. During a write operation, display data is stored at the addressed locations.

7.7 Display address counter

The display address counter generates read addresses to the DDRAM. During a read operation, display data is read out to the LCD.

7.8 Command decoder

The command decoder receives command words which are followed by data byte(s) from the I²C-bus. The command decoder identifies the command words and determines the destination for the data byte(s).

7.9 Column driver outputs

The LCD driver section has 101 outputs (C0 to C100) which should be connected directly to the column drive inputs of the LCD. The column driver signals are generated in accordance with the multiplexed row signals and with the data in the display data latch.

The programmed grey-scale levels are built-up in the LCD over four frames ($N1_1$, $N1_2$, $N1_3$ and $N1_4$) as shown in Figs 3, 4 and 5.

7.10 Row driver outputs

The LCD driver section has 67 outputs (R0 to R66) which should be connected directly to the row drive inputs of the LCD. The row driver signals are generated in accordance with the selected LCD drive mode.

7.11 Bias voltage generator

The bias voltage generator generates 4 buffered intermediate LCD bias voltages. It contains 4 operational amplifiers and an input reference voltage generator. It can operate in two voltage ranges:

- Normal mode (from 7.0 to 14.5 V)
- Partial screen mode (from 4.5 to 14.5 V).

7.12 High voltage generator

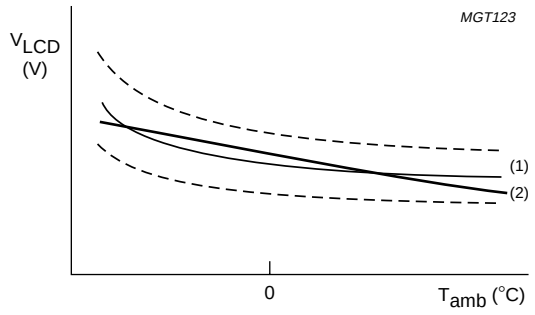
The high voltage generator contains a voltage multiplier which uses a charge pump circuit supplied by V_{DD2} and V_{DD3}.

The multiplier is software programmable with a factor from 2 to 8. In the direct drive mode the output voltage $V_{LCDOUT} = V_{DD2}$.

7.13 Temperature compensation

The viscosity of the liquid crystal depends on the temperature; so to maintain optimum contrast at lower temperatures V_{LCD} needs usually to be increased. Fig.2 shows V_{LCD} as a function of the temperature for a typical high multiplex rate liquid crystal.

Linear temperature compensation is supported in the PCF8820. The temperature coefficient for V_{LCDOUT} can be set to one of 8 values by setting bits TC_2 to TC_0.



(1) LCD characteristic.
(2) Linear temperature compensation.

Fig.2 LCD supply voltage as a function of the temperature.

7.14 Temperature sensor

The PCF8820 has a built-in temperature sensor. The sensor monitors the temperature and writes an 8-bit number into the status register. The temperature sensor and status register can both be accessed via the I^2C-bus interface controller.

The temperature sensor allows any temperature compensation to be implemented; any programmable parameter can be optimized as a function of the sensor read-out temperature.

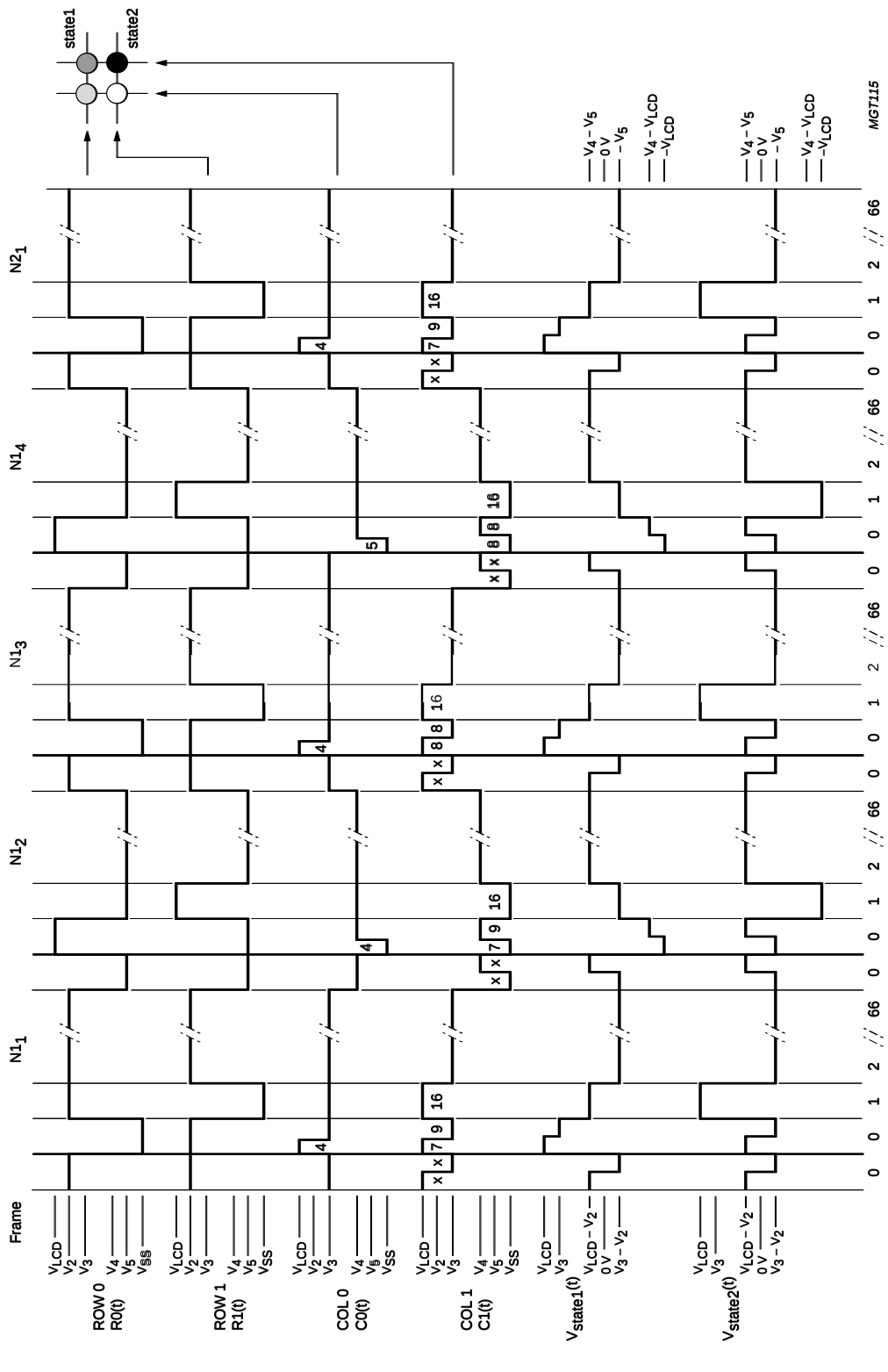
7.15 LCD driver waveforms

The LCD waveforms are shown in Figs 3, 4 and 5.

At frame inversion, the PCF8820 generates a dummy row cycle, where no row is selected. This ensures equal conditions for the first row after frame inversion as for the other rows. Therefore the effective multiplex rate in all modes is 1 : (multiplex rate + 1).

7.16 DDRAM to display mapping

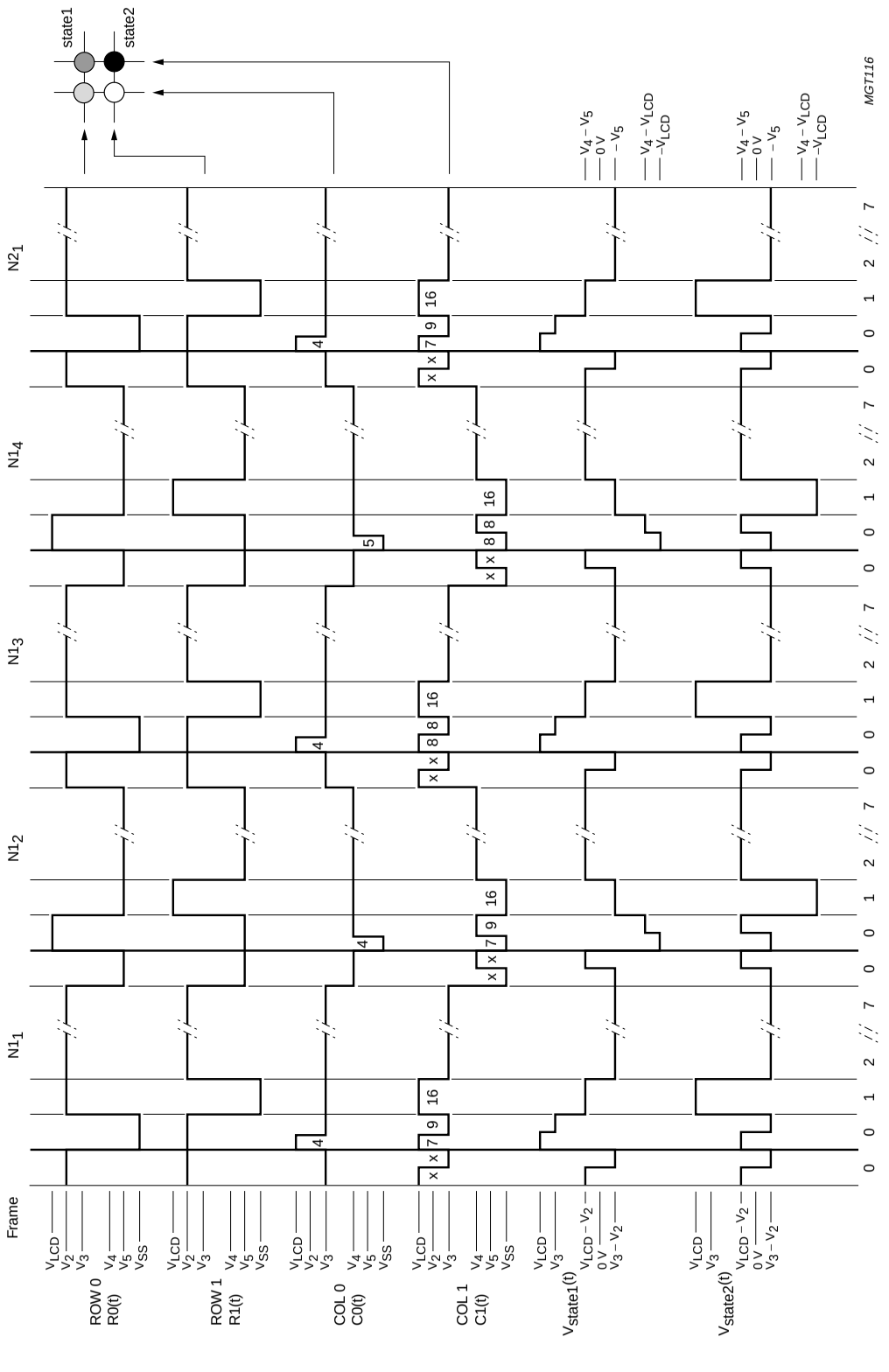
DDRAM to display mapping is shown in Fig.6.



Example for setting grey-scale register.
ROW0, COL0: GS = 17
ROW1, COL0: GS = 0
ROW0, COL1: GS = 30
ROW1, COL0: GS = 63 (63 will be set to 64; see Section 8.1.8).

$V_{state1}(t) = C1(t) - R0(t)$
$V_{state2}(t) = C1(t) - R1(t)$

Fig.3 Typical LCD driver waveforms at a multiplex rate of 1 : 67.



Example for setting grey-scale register.
ROW0, COL0: GS = 17
ROW1, COL0: GS = 0
ROW0, COL1: GS = 30
ROW1, COL0: GS = 63 (63 will be set to 64; see Section 8.1.8).

$V_{state1}(t) = C1(t) - R0(t)$
$V_{state2}(t) = C1(t) - R1(t)$

Fig.4 Typical LCD driver waveforms at a multiplex rate of 1 : 8 for partial screen mode.

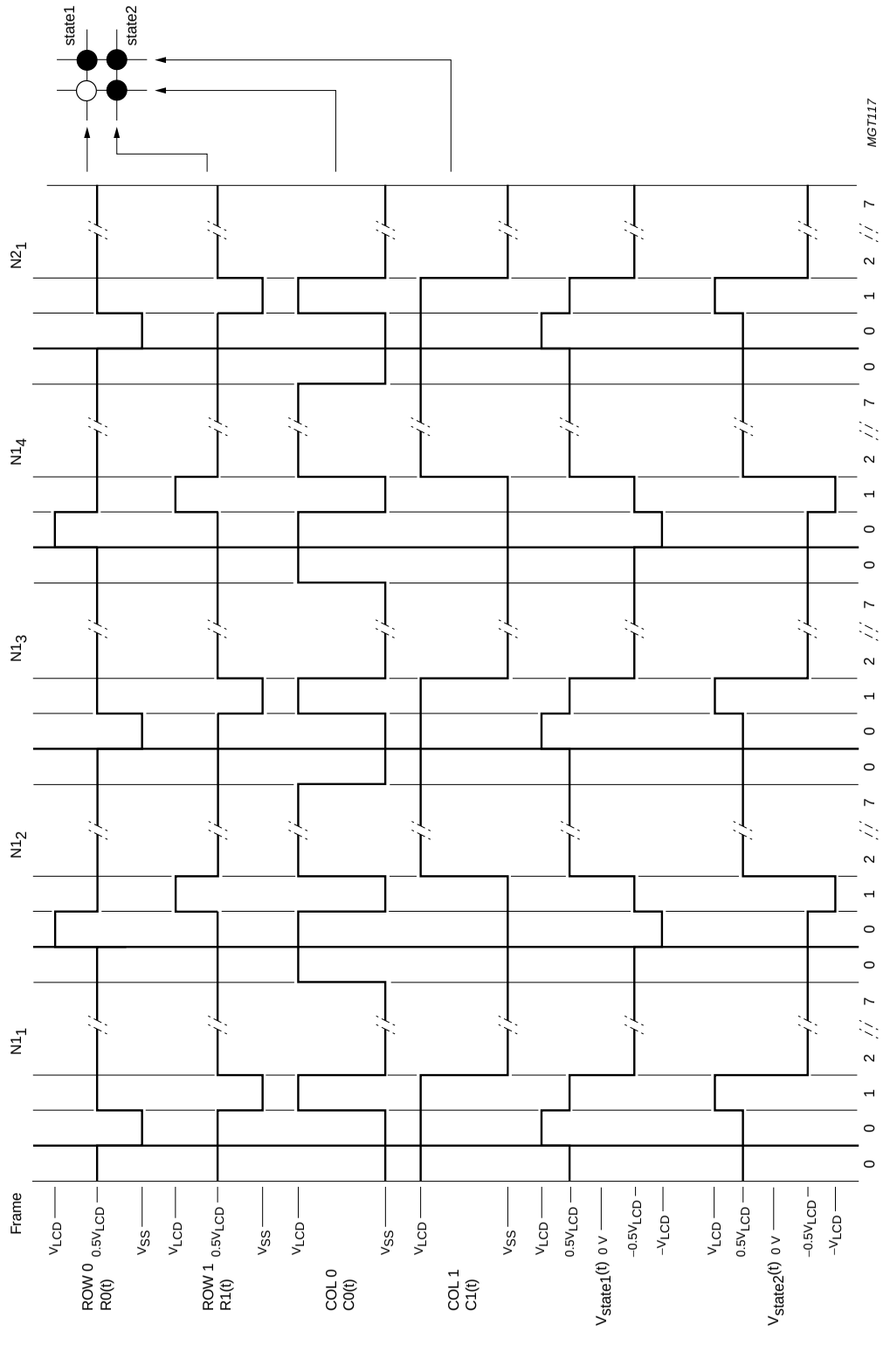


Fig.5 Typical LCD driver waveforms at a multiplex rate of 1 : 8, for partial screen mode and bias system $^{1}/_{2}$.

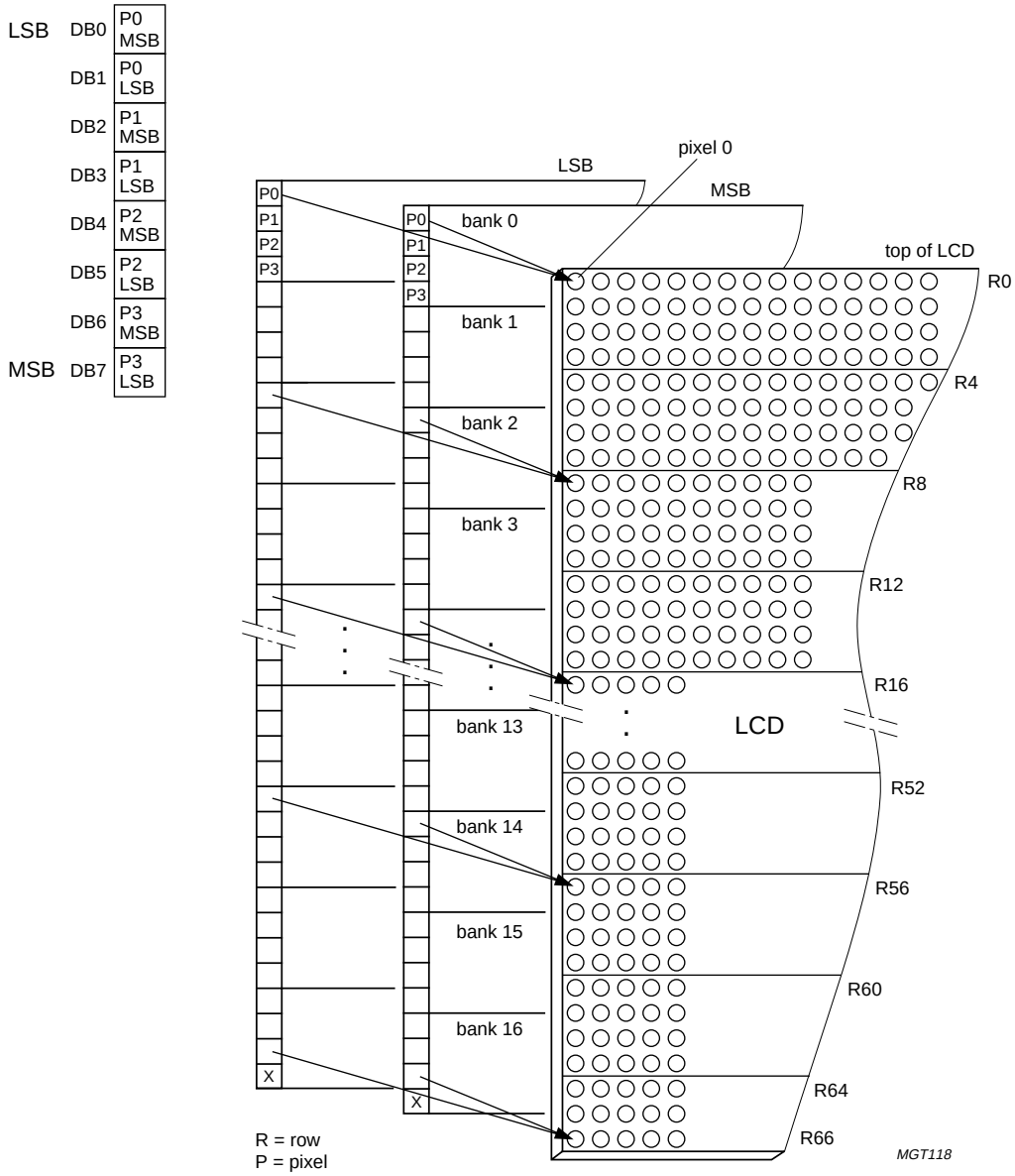


Fig.6 DDRAM to display mapping.

7.17 DDRAM addressing

Data is written in 8-bit bytes into the display data RAM matrix of the PCF8820 (see Figs 6 to 8). The display data RAM comprises a matrix of 67 × 101 × 2 bits. The columns are addressed by the address pointer. The address ranges are: X = 0 to 100 (64H) and Y = 0 to 16 (10H). It should be noted that only 3 rows are addressed in bank 16. Addresses outside these ranges are not allowed.

Bit MX (see Table 3) enables or disables horizontal address space mirroring:

- When bit MX = 0, mirroring is disabled. The address corresponds to Col0 (see Fig.7).
- When bit MX = 1, mirroring is enabled and address X = 0 corresponds to Col0 (see Fig.8). Bit MX determines how data is written to the RAM. If bit MX is changed after writing data to the RAM, no change on the display will be visible.

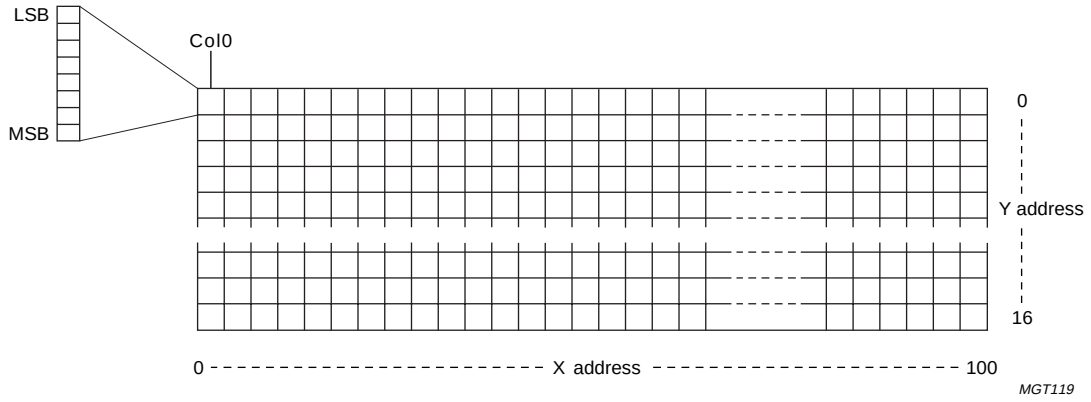


Fig.7 RAM X-address format for mirroring disabled.

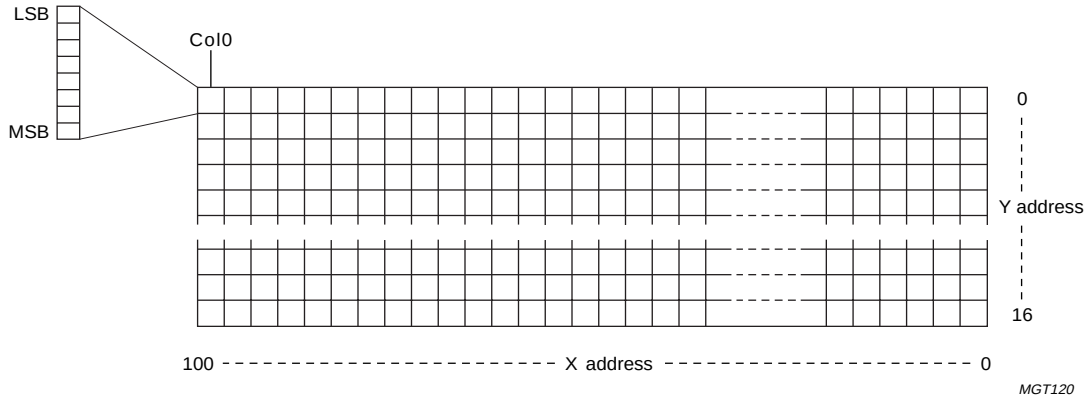


Fig.8 RAM X-address format for mirroring enabled.

Bit V (see Table 3) selects either horizontal or vertical address mode:

- In vertical address mode (bit V = 1), the Y-address is incremented after each byte (see Fig.9). After Y = 16, the Y-address sequence returns to Y = 0 and the X-address is incremented to address the next column.
- In horizontal address mode (bit V = 0) the X-address is incremented after each byte (see Fig.10). After X = 100, the X-address sequence returns to X = 0 and the Y-address is incremented to address the next row.

After the very last address (X = 100 and Y = 16), the address pointers return to the first address (X = 0 and Y = 0). It should be noted that in bank 16 only bits DB0 to DB5 of the data will be written into the RAM.

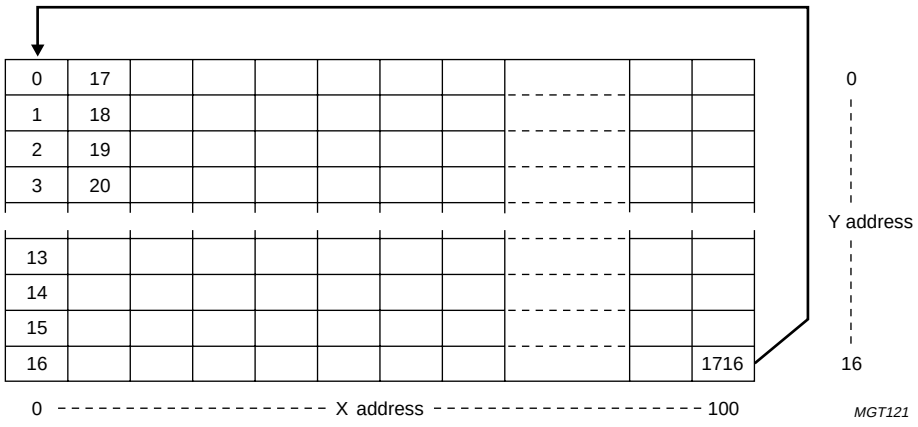


Fig.9 Writing data to RAM sequence in vertical address mode.

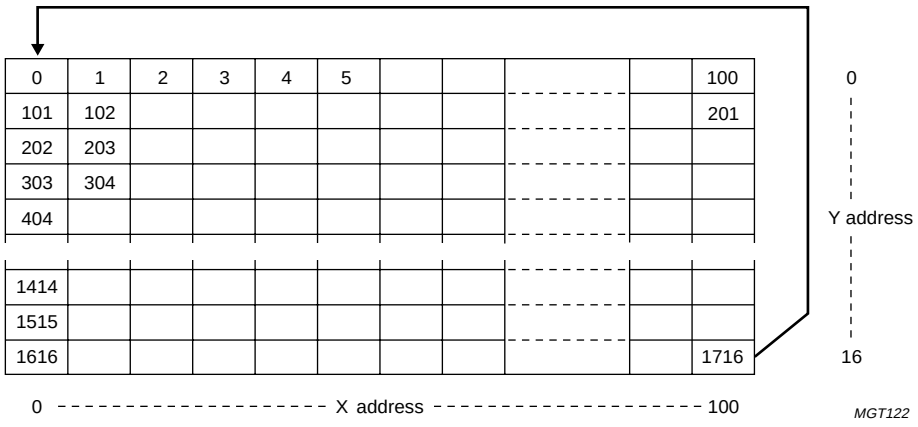


Fig.10 Writing data to RAM sequence in horizontal address mode.

7.18 I²C-bus interface

The I²C-bus allows bidirectional data communication between different ICs or modules. The serial data input line and serial data output line are connected together, so representing the Serial Data (SDA) line. See Section 13.4 for layout considerations. The SDA line and the Serial Clock Line (SCL) line must be connected to a positive supply voltage via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.18.1 BIT TRANSFER

One data bit is transferred during a clock pulse period. The data on the SDA line must remain stable during the HIGH period of the clock pulse, otherwise any change in the data within this period will be interpreted as a control signal (see Fig.11).

7.18.2 START AND STOP CONDITIONS

Both data and clock lines are HIGH when the bus is not busy (see Fig.12).

A START condition (S) occurs when the data line goes from HIGH-to-LOW while the clock is HIGH.

A STOP condition (P) occurs when the data line goes from LOW-to-HIGH while the clock is HIGH.

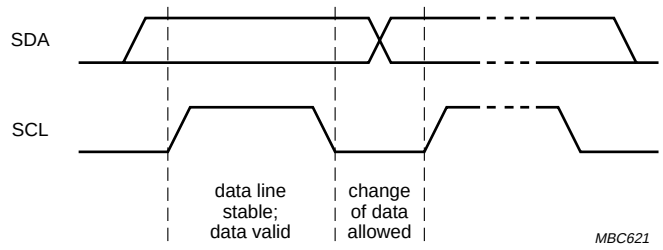


Fig.11 Bit transfer.

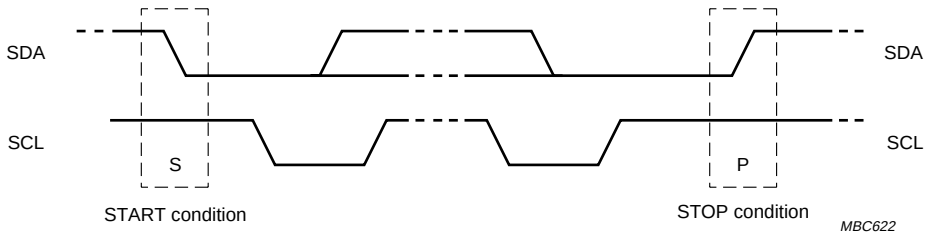


Fig.12 Definition of START and STOP conditions.

7.18.3 SYSTEM CONFIGURATION

Thd system components are defined below (see Fig.13):

- Transmitter: the device which sends data to the bus
- Receiver: the device which receives data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

7.18.4 ACKNOWLEDGE

Each 8-bit data byte transferred over the bus must be followed by an acknowledge bit (see Fig.14).

During the acknowledge clock pulse a HIGH-level signal is put on the bus by the transmitter.

A slave receiver which is addressed must generate an acknowledge bit after the reception of each data byte. A master receiver must generate an acknowledge bit after receiving a data byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line to a LOW-level during the acknowledge clock pulse. Set-up and hold times must be taken into consideration to ensure that the SDA line is stable during the HIGH period of the acknowledge related clock pulse.

A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge bit on the last byte that has been clocked out of the slave transmitter. In this event the slave transmitter must leave the data line HIGH to allow the master to generate a STOP condition.

For the PCF8820 the acknowledge bit is output at pad SDA_OUT.

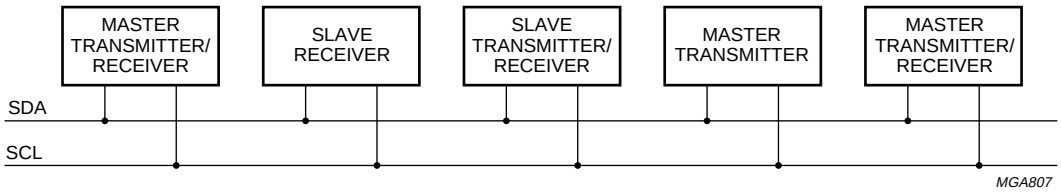


Fig.13 System configuration.

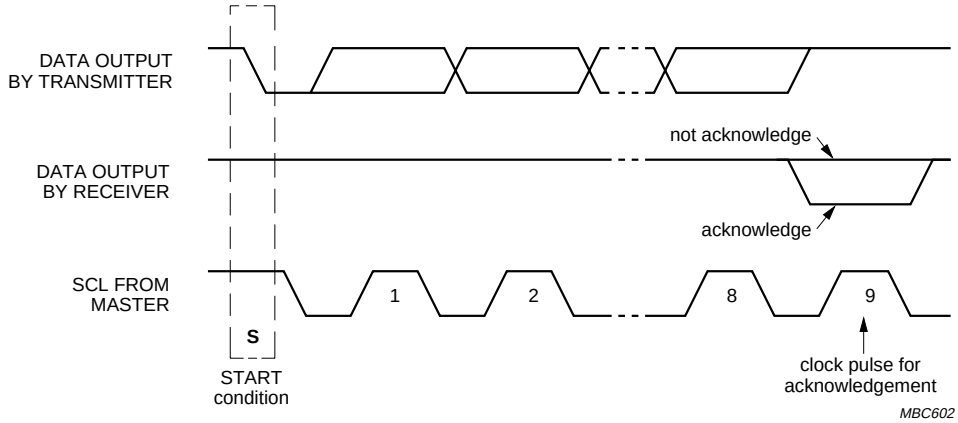


Fig.14 Acknowledgement on the I^2C-bus.

7.18.5 I²C-BUS PROTOCOL

The PCF8820 is a slave transmitter/receiver. If data is to be read from the device, the SDA_OUT output must be used.

Before any data is transferred over the I²C-bus, the destination device is addressed first (see Fig.15).
The PCF8820 has four 7-bit slave addresses reserved: 0111 100, 0111 101, 0111 110 and 0111 111. The two least significant bits of the slave address are set by connecting slave address inputs SA1 and SA0 to either V_{SS1} (logic 0) or V_{DD1} (logic 1).

A write sequence (see Fig.17) is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. Only the addressed slave acknowledges. After acknowledgement, one or more command words follow which define the status of the addressed slave.

A command word consists of a control byte (see Fig.16) defining 'continuation' bit Co and 'register selection' bit RS, plus a data byte. The last control byte is indicated by resetting bit Co = 0. The control and data bytes are also acknowledged by all addressed slaves on the bus.

Depending on the setting of bit RS in the last control byte, either a series of display data bytes or command data bytes may follow.

If bit RS = 1, the data bytes are stored as display data in the DDRAM at the address specified by the data pointer. The data pointer is automatically incremented.
If bit RS = 0, the data byte is interpreted as a command byte to be decoded and the device will be set according to the received commands.

Only the addressed PCF8820 acknowledges after each byte is received. The I²C-bus master issues a stop condition (P) at the end of the transmission.

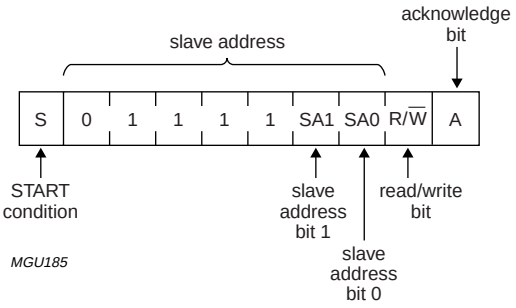


Fig.15 Slave address.

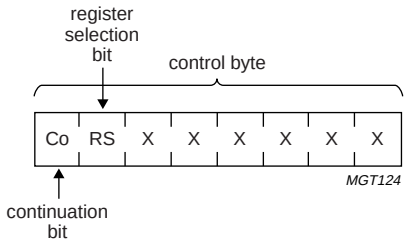


Fig.16 Control byte.

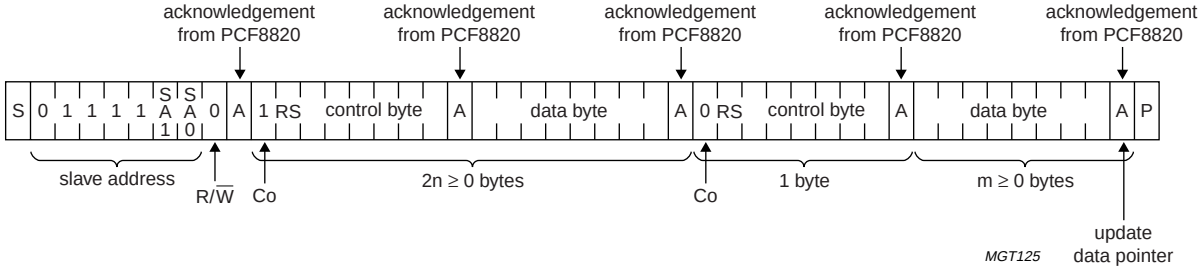


Fig.17 Write sequence: master transmits bytes to slave receiver.

For a read sequence (see Fig.18), the addressed PCF8820 will immediately start to output the requested data until a NOT acknowledge is transmitted by the master. Before the read access, the user has to set bit RS to the appropriate value by a preceding write access. The sequence should be terminated by a STOP condition when no further access is required, or by a RE-START condition if further access is required.

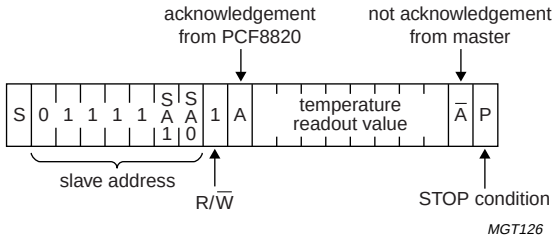


Fig.18 Read sequence: master receives bytes from slave transmitter status register.

7.18.6 Command decoder

The command decoder identifies command words received via the I^2C-bus.

Bit 7 of the control byte is named bit Co (see Fig.16):

- Bit Co = 1 indicates that only one command byte or DDRAM data byte will follow next
- Bit Co = 0 indicates that a stream of command bytes or DDRAM data bytes will follow next depending on last status of bit RS.

Bit 6 of a control byte is named bit RS:

- Bit RS = 1 indicates that another DDRAM data byte will follow next
- Bit RS = 0 indicates that another command byte will follow next.

The definition of bits Co and RS is shown in Table 1.

7.18.7 Display data byte

A display data byte for grey-scale is shown in Fig.19.

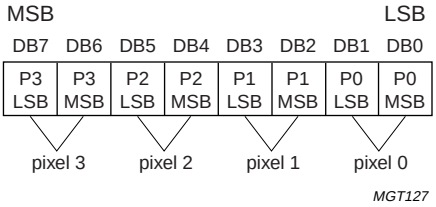


Fig.19 Grey-scale display data byte.

Table 1 Definition of bits Co and RS

BIT	VALUE	ACTION
Co	0	last control byte to be sent; only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or RE-START condition
	1	another control byte will follow the data byte unless a STOP or RE-START condition is received
RS	0	data byte will be decoded and used to set up the device
		data byte will return the sensor temperature read-out
	1	data byte will be stored in the DDRAM
		RAM read-back (not supported)

8 INSTRUCTIONS

The PCF8820 interfaces via the I²C-bus. The clock of the LCD is not required to process instructions.

The data received by the PCF8820 is either instruction data which defines its operating mode or display data to be stored in its DDRAM. The type of data is identified by bit RS. When bit RS = 0, the PCF8820 will respond to the instructions. When bit RS = 1, the PCF8820 will load the data into its DDRAM.

There are four types of instruction data whose functions are listed below:

- Define PCF8820 functions, such as display configuration, etc.
- Set DDRAM addresses
- Perform data transfers to DDRAM
- Other functions.

In normal use, the most frequently used instructions are those which perform data transfers to the DDRAM. Address pointer update follows after the data byte has been written to the DRAM. This reduces the program load of the microcontroller.

Undefined register locations are not allowed.

The instruction set comprises several command pages. A command page is selected by setting bits H_0 to H_2.

The instruction set is given in Table 2.

The bit functions are described in detail in Section 8.1.

Table 2 Instruction set

INSTRUCTION	CONTROL BITS(1)		COMMAND BYTE								DESCRIPTION
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Independent command page (H_2 = X, H_1 = X, H_0 = X); note 2											
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to DDRAM
Read temperature	0	1	TR_7	TR_6	TR_5	TR_4	TR_3	TR_2	TR_1	TR_0	reads sensor temperature read-out
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Default H_2 to H_0	0	0	0	0	0	0	0	0	0	1	jumps to function and RAM command page
Function and RAM command page (H_2 = 0, H_1 = 0, H_0 = 0)											
Instruction set	0	0	0	0	0	0	1	H_2	H_1	H_0	selects a command page
Select function	0	0	0	0	0	1	DO	PD	V	0	data order; power-down control; address mode
Set Y address of DDRAM	0	0	0	1	0	Y_4	Y_3	Y_2	Y_1	Y_0	selects Y-address of DDRAM: 0 ≤ Y ≤ 16
Set X address of DDRAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	selects X-address of DDRAM: 0 ≤ X ≤ 100
Display setting command page (H_2 = 0, H_1 = 0, H_0 = 1)											
Display control	0	0	0	0	0	0	0	1	D	E	selects display mode
External display control	0	0	0	0	0	0	1	MX	MY	PS	mirror X; mirror Y; partial screen mode
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	selects bias system
Bias system $^1/_2$	0	0	0	0	1	1	1	0	0	$BS^1/_2$	set bias system $^1/_2$ for partial screen mode

INSTRUCTION	CONTROL BITS(1)		COMMAND BYTE								DESCRIPTION
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display part	0	0	0	1	0	0	0	DP_2	DP_1	DP_0	set display for partial screen mode
HVGen command page (H_2 = 0, H_1 = 1, H_0 = 0)											
High voltage generator control	0	0	0	0	0	0	0	1	PRS	HVE	set V_{LCDOUT} programming range and high voltage generator on
High voltage generator configuration	0	0	0	0	0	0	1	S_2	S_1	S_0	set voltage multiplier factor
Temperature control	0	0	0	0	0	1	0	TC_2	TC_1	TC_0	set temperature coefficient
Temperature measurement control	0	0	0	0	1	0	0	0	0	SM	start temperature measurement
V_{LCD} control	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	set V_{LCD} register value: $0 \leq V_{OP} \leq 127$
Grey-scale/colour command page (H_2 = 0, H_1 = 1, H_0 = 1)											
Grey-scale register control	0	0	0	1	0	0	0	0	GR_1	GR_0	select grey-scale register: $0 \leq GR \leq 3$
Grey-scale level control	0	0	1	0	GS_5	GS_4	GS_3	GS_2	GS_1	GS_0	set grey-scale register value: $0 \leq GS \leq 63$
Special feature command page (H_2 = 1, H_1 = 0, H_0 = 0)											
Display off, direct drive mode	0	0	0	0	0	0	0	1	DOF	DM	display off; voltage multiplier in direct drive mode
Oscillator setting	0	0	0	0	0	0	1	0	EC	OC	select external clock; start oscillator calibration
Row block swapping	0	0	0	1	0	TRS	BRS	0	0	0	top row swap; bottom row swap

Notes

1. Bit R/$\overline{W}$ is set in the slave address byte; bit RS is set in the control byte.
2. X = don’t care.

8.1 Description of the bit functions

Table 3 Instruction set bit functions

BIT	RESET STATE	VALUE	FUNCTION
D_7 to D_0	–	–	data to be written to DDRAM
TR_7 to TR_0	–	–	read-out value of sensor temperature
H_2 to H_0			command page numbers
	000	000	function and RAM
		001	display setting
		010	high voltage generator setting
		011	grey-scale/colour
		100	special features
DO			data order when written to DDRAM
	0	0	normal (see Fig.6)
		1	swapped: DB7 <-> DB0, DB6 <-> DB1, etc.
PD			operation mode
		0	operating mode
	1	1	Power-down mode; see Section 8.1.1
V			address mode
	0	0	horizontal address mode: data is written to DDRAM (see Fig.10)
		1	vertical address mode: data is written to DDRAM (see Fig.9)
Y_4 to Y_0	0	–	Y-address of the DDRAM points to the rows; the address range is from 0 to 16 (10H); see Section 8.1.3
X_6 to X_0	0	–	X-address of the DDRAM points to the columns; the address range is from 0 to 100 (64H)
D, E			display mode
	00	00	display blank: using the value in grey-scale register 0
		01	all display segments on: using the value in grey-scale register 3
		10	normal mode: using the values of the four grey-scale registers appropriate to the RAM data
		11	inverse video: using the values in all four grey-scale registers as in normal mode but with their values swapped (GS_0 and GS_3 values transposed, GS_1 and GS_2 values transposed)
MX			horizontal address space mirroring; see Figs 7 and 8; see Table 10
	0	0	disabled: data to DDRAM is written from left (X = 0) to right (X = 100)
		1	enabled: data to DDRAM is written from right (X = 0) to left (X = 100)
MY			vertical address space mirroring; see Table 10
	0	0	disabled: normal display
		1	enabled: data is immediately mirrored vertically on the LCD. The status of bit MY takes effect when data is read from the DDRAM and when generating column signals.

BIT	RESET STATE	VALUE	FUNCTION
PS			screen mode
	0	0	full display mode: multiplex rate is 1 : 67
		1	partial screen mode: multiplex rate is 1 : 8; see Section 8.1.2.
BS_2, BS_1, BS_0	000	–	bias system selection bits; see Section 8.1.4
$BS^1/_2$			bias system selection
	0	0	setting of bits BS2 to BS0
		1	bias system $^1/_2$; see Section 8.1.4
DP_2, DP_1, DP_0			display part
	000	000	DDRAM bank 0 to 1: first 8 rows
		111	DDRAM bank 14 to 15: last 8 rows
PRS			V_{LCDOUT} programming range; see Fig.20
	0	0	LOW range
		1	HIGH range
HVE			high voltage generator
	0	0	disabled
		1	enabled
S_2, S_1, S_0			voltage multiplier factor; see Section 8.1.5
	000	000	$2 \times V_{DD2}$
		001	$3 \times V_{DD2}$
		010	$4 \times V_{DD2}$
		011	$5 \times V_{DD2}$
		100	$6 \times V_{DD2}$
		101	$7 \times V_{DD2}$
		110	$8 \times V_{DD2}$
TC_2, TC_1, TC_0			temperature coefficient; see Chapter 11
	000	000	coefficient 0
		001	coefficient 1
		010	coefficient 2
		011	coefficient 3
		100	coefficient 4
		101	coefficient 5
		110	coefficient 6
		111	coefficient 7
SM			temperature measurement
	0	0	no measurement
		1	start measurement
V_{OP6} to V_{OP0}	0	–	V_{LCD} control register bits; see Section 8.1.7

BIT	RESET STATE	VALUE	FUNCTION
GR_1, GR_0			grey-scale register selection:
	00	00	register 0: applied if DDRAM content is 00
		01	register 1: applied if DDRAM content is 01
		10	register 2: applied if DDRAM content is 10
		11	register 3: applied if DDRAM content is 11
GS_5 to GS_0	0	–	grey-scale level bits; in the reset state all 4 grey-scale registers are reset to 0; see Section 8.1.8
DOF			display on/off
		0	display on
	1	1	display off: the state of the PCF8820 is equivalent to Power-down mode (bit PD = 1). However, temperature measurement is still possible
DM			drive of voltage multiplier
	0	0	no direct drive
		1	direct drive: $V_{LCDOUT} = V_{DD2}$; see Section 8.1.9
EC			clock selection
		0	internal clock
		1	external clock
OC			oscillator setting; see Section 8.1.10
	0	0	stop calibration of frame frequency
		1	start calibration of frame frequency
TRS			top rows
	0	0	not swapped
		1	swapped: the signals for row driver outputs R23 to R33 appear at outputs R56 to R66, and the signals for row driver outputs R56 to R66 appear at outputs R23 to R33
BRS			bottom rows
	0	0	not swapped
		1	swapped: the signals for row driver outputs R0 to R22 appear at outputs R34 to R55, and the signals for row driver outputs R34 to R55 appear at outputs R0 to R22

8.1.1 POWER-DOWN MODE

During power-down (bit PD = 1) all static currents are switched off (no internal oscillator, no timing, no LCD segment drive system) and all LCD outputs are internally connected to V_{SS}.

To decrease the voltage at V_{LCDOUT} very fast the following features can be used:

- Select the direct drive mode by setting bit DM = 1 resulting in $V_{LCDOUT} = V_{DD2}$
- Select the non direct drive mode by setting bit DM = 0, resulting in V_{LCDOUT} = 0 V (output high-impedance).

During power-down:

- All LCD outputs at V_{SS} (display off)
- Oscillator is off
- Intermediate bias voltage generator is off
- High voltage generator is disabled; however, the status of bit HVE is unchanged (see Table 8)
- An external V_{LCD} can be disconnected from V_{LCDIN}
- The I^2C-bus is operational; commands can be executed
- DDRAM contents is not cleared; DDRAM data can be written
- Register settings remain unchanged
- Temperature measurement is not possible.

8.1.2 PARTIAL SCREEN MODE

Partial screen mode allows data to be displayed of DDRAM bank 0 to 1 on the first 8 rows or bank 14 to 15 on the last 8 rows, depending on the status of bits DP_2 to DP_0.

If bit MY = 0, data is displayed either on rows 0 to 7 (first 8 rows) or on rows 56 to 63 (last 8 rows).

If bit MY = 1, data is displayed either on rows 66 to 59 (first 8 rows) or on rows 10 to 3 (last 8 rows).

The partial screen mode also allows V_{LCDIN} to be reduced to save power.

Frame frequency calibration is not allowed in the partial screen mode.

8.1.3 Y-ADDRESS OF DDRAM

Bits Y_4 to Y_0 define the Y-address of the DDRAM.

Table 4 Y-address

Y_4	Y_3	Y_2	Y_1	Y_0	RAM BANK
0	0	0	0	0	bank 0
0	0	0	0	1	bank 1
0	0	0	1	0	bank 2
0	0	0	1	1	bank 3
0	0	1	0	0	bank 4
0	0	1	0	1	bank 5
0	0	1	1	0	bank 6
0	0	1	1	1	bank 7
0	1	0	0	0	bank 8
0	1	0	0	1	bank 9
0	1	0	1	0	bank 10
0	1	0	1	1	bank 11
0	1	1	0	0	bank 12
0	1	1	0	1	bank 13
0	1	1	1	0	bank 14
0	1	1	1	1	bank 15
1	0	0	0	0	bank 16

8.1.4 BIAS SYSTEM

Different LCD bias voltage settings are required at different multiplex rates. The status of bits BS_2 to BS_0 and bit $BS^1/_2$ select different 'bias systems' which determine the intermediate bias voltage levels between V_{LCDIN} and V_{SS1}. It should be noted that the bias system selected by bit $BS^1/_2$ is independent of the bias systems selected by bits BS_2 to BS_0.

A value 'n' attributed to each bias system is used to calculate these levels (see Table 5).

The optimum value for 'n' is given by: $n = \sqrt{M} - 3$ where M is the multiplex rate.

Table 6 shows how bias voltage levels are calculated for three of the available bias systems using supported 'n' values.

Table 5 Programming the required bias system

BS2	BS1	BS0	BS$^1/_2$	n	BIAS SYSTEM	COMMENT
0	0	0	0	7	$^1/_{11}$	
0	0	1	0	6	$^1/_{10}$	
0	1	0	0	5	$^1/_9$	recommended at multiplex rate 1 : 67
0	1	1	0	4	$^1/_8$	
1	0	0	0	3	$^1/_7$	
1	0	1	0	2	$^1/_6$	
1	1	0	0	1	$^1/_5$	
1	1	1	0	0	$^1/_4$	recommended at multiplex rate 1 : 8
X	X	X	1	–2	$^1/_2$	allows a lower V_{LCDIN} at multiplex rate 1 : 8

Table 6 Examples of LCD bias voltages

BIAS VOLTAGE LEVEL ON PAD	CALCULATING BIAS VOLTAGE	BIAS SYSTEM		
		$^1/_9$ (n = 5)	$^1/_4$ (n = 0)	$^1/_2$ (n = –2)
V_{LCDOUT}	V_{LCDIN}	V_{LCDIN}	V_{LCDIN}	V_{LCDIN}
V_2	$\frac{n+3}{n+4} \times V_{LCDIN}$	$^8/_9 \times V_{LCDIN}$	$^3/_4 \times V_{LCDIN}$	$^1/_2 \times V_{LCDIN}$
V_3	$\frac{n+2}{n+4} \times V_{LCDIN}$	$^7/_9 \times V_{LCDIN}$	$^1/_2 \times V_{LCDIN}$	V_{SS1}
V_4	$\frac{2}{n+4} \times V_{LCDIN}$	$^2/_9 \times V_{LCDIN}$	$^1/_2 \times V_{LCDIN}$	V_{LCDIN}
V_5	$\frac{1}{n+4} \times V_{LCDIN}$	$^1/_9 \times V_{LCDIN}$	$^1/_4 \times V_{LCDIN}$	$^1/_2 \times V_{LCDIN}$
V_{SS1}	V_{SS1}	V_{SS1}	V_{SS1}	V_{SS1}

8.1.5 High voltage generator configuration

The PCF8820 incorporates a software configurable voltage multiplier which uses a charge pump circuit supplied by V_{DD2} and V_{DD3}. After a reset the voltage multiplier factor is set to 2 ($V_{LCDOUT} = 2 \times V_{DD2}$). Other voltage multiplier factors are set by bits S_2 to S_0.

To reduce high current peaks at voltage multiplier start-up, it is recommended that the voltage multiplier is switched on using the following procedure:

1. Set bit DM = 1 and bit PD = 1
2. Set multiplication factor to 2 by setting bits S_2 to S_0 to logic 0
3. Set register value V_{OP} to the desired value, bit PRS = 1 and bit HVE = 1
4. Set bit PD = 0, which switches on the charge pump (at multiplication factor 2)
5. Increment the multiplication factor to the desired value for V_{LCDOUT} using bits S_2 to S_0.

8.1.6 Temperature read-out

The PCF8820 has a built-in temperature sensor. At the end of a temperature measurement, the sensor writes a temperature value to the status register. The temperature value is an 8-bit number represented by bits TR_7 to TR_0 in the status register which can be read via the I^2C-bus.

To save power, the sensor need only be enabled when a measurement is required. A measurement is initialized by setting bit SM = 1 which will be automatically cleared after 5 clock cycles (from internal oscillator or external clock). The internal oscillator will be initialized and allowed to warm-up for approximately 2 frame periods, after which a measurement will be initiated at the start of the next frame and completing after 2 frames.

It is not possible to measure temperature in Power-down mode.

During a temperature measurement, the status register value remains zero until the measurement has completed and then the register is updated with the current temperature value (non-zero value). Because the I^2C-bus interface is asynchronous to the temperature measurement, the value read from the status register should be validated by reading the status register a few times.

During a temperature measurement, the temperature coefficient (TC) has to be selected.

The ideal temperature read-out can be calculated by the equation: $TR_{ideal} = 128 + (T - 27\ °C) \times \frac{1}{a}$

where T is the on-chip temperature in °C and 'a' is the conversion constant (see Chapter 11).

To improve the accuracy of the temperature measurement, it is recommended that the temperature read-out is calibrated during the product's final assembly. Calibration of the temperature read-out requires a measurement to be made at a defined ideal temperature. The offset between the ideal temperature value and the measured temperature value is calculated by:

$TR_{offset} = TR_{ideal} - TR_{meas}$

where TR_{meas} is the actual temperature read-out of the PCF8820. The offset value must be stored in a non-volatile register, such as an EEPROM.

A calibrated temperature read-out can be calculated for each measurement by the equation:

$TR_{cal} = TR_{meas} + TR_{offset}$

The accuracy after the calibration is ±10% ±1 bit of the difference between the measured temperature and the calibration temperature. For this reason, it is recommended that a calibration is performed at or near the most sensitive LCD temperature.

For example: calibration temperature is 25 °C and the measured temperature is –20 °C. The relative error $A = \pm 0.10 \times \{25 - (-20)\}\ \pm 1\ \text{bit} \times a$

$A = \pm 4.5\ \pm 1.13$

$A = \pm 5.63$ °C.

This calibration accuracy is valid for temperature measurements made when the supply voltage value is the same as when it was calibrated.

8.1.7 V_{LCD} CONTROL REGISTER

The V_{LCDOUT} value can be set by software using the bits V_{OP6} to V_{OP0} of the V_{LCD} control register.

The programmed value for V_{LCD} has to be calculated for a reference temperature, called the cut-point temperature T_{cp}, using the equation:

$V_{LCD}\ (\text{at } T_{cp}) = a + b \times V_{OP}$

The values for parameters T_{cp}, a and b are given in Table 7, and their relationship with the V_{LCD} control register values are shown in Fig.20.

The V_{LCDOUT} generated is dependent on the operating temperature T_{oper}, the selected temperature coefficient TC and the programmed value for V_{LCD} at the reference temperature T_{cp} and is calculated by the equation:

$V_{LCD}\ (\text{at } T_{oper}) = V_{LCD}\ (\text{at } T_{cp}) \times \{1 + TC \times (T_{oper} - T_{cp})\}$

Two overlapping V_{LCD} ranges are selectable by bit PRS (see Table 7 and Fig.20). The maximum voltage that can be generated depends on the values of V_{DD2} and V_{DD3}, and the display load current. At a multiplex rate of 1 : 67, the optimum operating voltage for the LCD can be calculated by the equation:

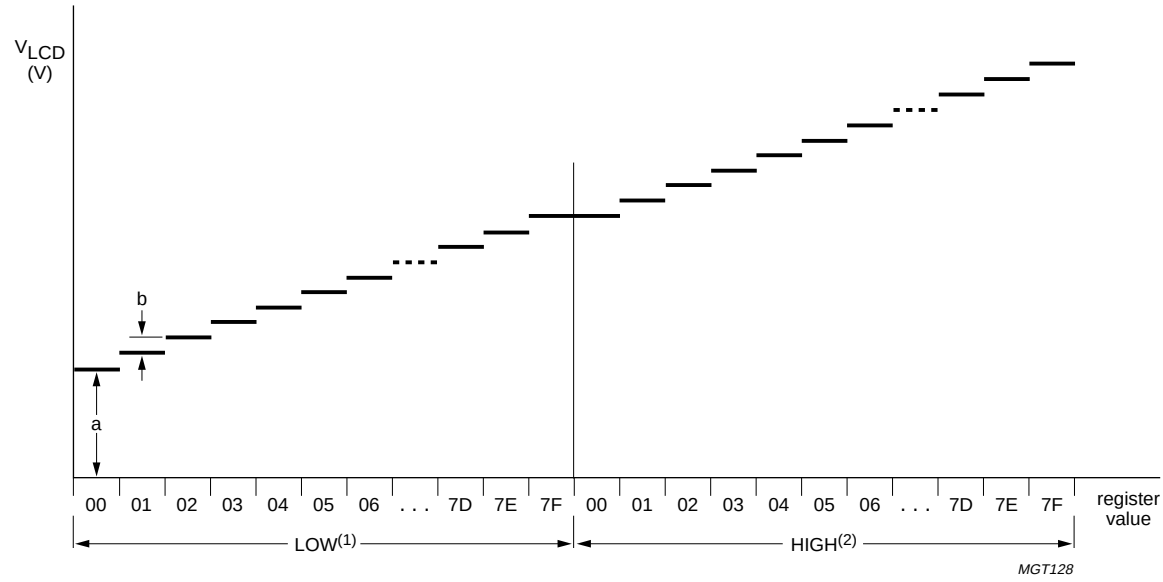
$$V_{LCD} = \frac{1 + \sqrt{67 + 1}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{67 + 1}}\right)}} \times V_{th} \cong 6.975 \times V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

The practical value for V_{LCD} is determined by equating $V_{off(rms)}$ with the defined LCD threshold voltage (V_{th}), which is the typically value when the LCD exhibits approximately 10% contrast.

Table 7 Parameter values for programming V_{LCD} control register

SYMBOL	VALUE		UNIT
	BIT PRS = 0	BIT PRS = 1	
T_{cp}	23.0	23.0	°C
a	4.500	10.215	V
b	0.045	0.045	V
programming range	4.5 to 10.215	10.215 to 15.93	V



(1) Bit PRS = 0: V_{LCD} programming range is LOW.
(2) Bit PRS = 1: V_{LCD} programming range is HIGH.

Fig.20 Generated V_{LCDOUT} set by programming V_{LCD} control register value (bits V_{OP6} to V_{OP0}).

The programming range for the generated V_{LCDOUT} allows values above the maximum value of V_{LCD}. Therefore, the user must ensure that the V_{LCD} control register value and the temperature coefficient selected, will never allow the maximum V_{LCD} limit to be exceeded for all conditions and including all tolerances. The customer must also ensure that the V_{LCD} control register value will never be lower than V_{DD1} or V_{DD2}, except in the Power-down mode, for all conditions and including all tolerances.

8.1.8 Grey-scale register and grey-scale level

The PCF8820 has 4 grey-scale registers selected by bits GR_0 and GR_1, which define the four grey intensity levels. Each of the 4 registers contain 6 bits allowing to select one out of the 64 grey levels. A grey-scale register must be addressed before it can be written to by using the instruction 'Grey-scale register' (see Table 2). The content of the grey-scale register (bits GS_5 to GS_0) is set by the instruction 'Grey-scale level control' (see Table 2). It should be noted that a grey-scale register setting of 63 is internally converted to 64. Even numbers are preferred; odd numbers produce a small DC component in the waveform of the respective column (see Fig.3).

The grey-scale level for each pixel is effected by writing the resultant grey-scale register value into the DDRAM (see Fig.6).

One of the grey-scale registers can be used to create a blinking cursor. The intensity of the pixels comprising the cursor are to be defined by the value in the grey-scale register. The brightness/colour of the cursor pixels can be changed by selecting a different grey-scale register containing a different grey-scale value.

A blinking cursor can be effected by continuously switching the content of one grey-scale register between the two grey-scales from e.g. white to black and back again with a frequency of 2 Hz giving the impression of a blinking cursor. This procedure causes less load for the microcontroller than changing all pixels which form the desired cursor. This implies the display has 3 grey-scale levels left e.g. off, grey and on.

8.1.9 DIRECT DRIVE MODE

The voltage multiplier is in the direct drive mode ($V_{LCDOUT} = V_{DD2}$) in the following settings (see Table 8):

- If bit DM = 1 and Power-down mode (bit PD = 1)
- If bit DM = 1 and display off mode (bit DOF = 1)
- If bit DM = 1 and high voltage generator is disabled (bit HVE = 0).

It is recommended to always select the direct drive mode before switching on the voltage multiplier. This is a feature which can be used to reduce V_{LCDOUT} very quickly, or to avoid high current when the voltage multiplier starts up.

Output V_{LCDOUT} is high-impedance when bit DM = 0 and bit PD = 1, bit DM = 0 and bit DOF = 0 or when bit DM = 0, bit PD = 0 and bit HVE = 0.

Table 8 Output V_{LCDOUT} as a function of bits DM, HVE, PD and DOF; note 1

DM	HVE	PD	DOF	V_{LCDOUT}
0	X	1	X	high Z
0	X	X	1	high Z
0	0	0	0	high Z
1	0	0	0	V_{DD2}
1	X	1	X	V_{DD2}
1	X	X	1	V_{DD2}
X	1	0	0	internally generated V_{LCD}

Note

1. X = don't care.

8.1.10 FRAME FREQUENCY CALIBRATION

The PCF8820 uses on-chip software to calibrate the frame frequency. After reset, the frame frequency calibration is disabled (bit OC = 0). Frame frequency calibration can only be performed if the PCF8820 is not in Power-down mode or in the partial screen mode.

The calibration is initiated by setting bit OC = 1 and is stopped by setting bit OC = 0. The time between calibration start and stop must be 190 μs to give a frame frequency of 77 Hz (typical value).

All other commands are allowed during a calibration.

The frame frequency calibration uses a pre-divider which has a range from 1 : 1 to 1 : 15. The default ratio after reset is 1 : 4. The calibration period determines the pre-divider ratio for the oscillator frequency or external clock signal.

The resulting frame frequency is calculated by the equation: $f_{frame} = \frac{f_{clk}}{1088} \times \text{pre-divider ratio}\ [\text{Hz}]$

where f_{clk} can be either the internal oscillator clock signal or an external clock signal source.

Figure 21 shows the resulting frame frequency at different clock frequencies and at different pre-divider ratios, for a calibration period of 190 μs.

The frame frequency calibration can also be used to set the frame frequency to a lower than typical value with a corresponding reduction in current consumption. The necessary calibration period (time between calibration start and stop) can be estimated by the equation:

$$t_{cal} = \frac{77\ (\text{Hz}) \times 190\ (\mu\text{s})}{f_{frame}}$$

where t_{cal} is the calibration time in μs and f_{frame} is the desired frame frequency in Hz.

Figure 22 shows the resulting frame frequency as a function of the calibration period at different pre-divider ratios at a clock frequency of 336 kHz.

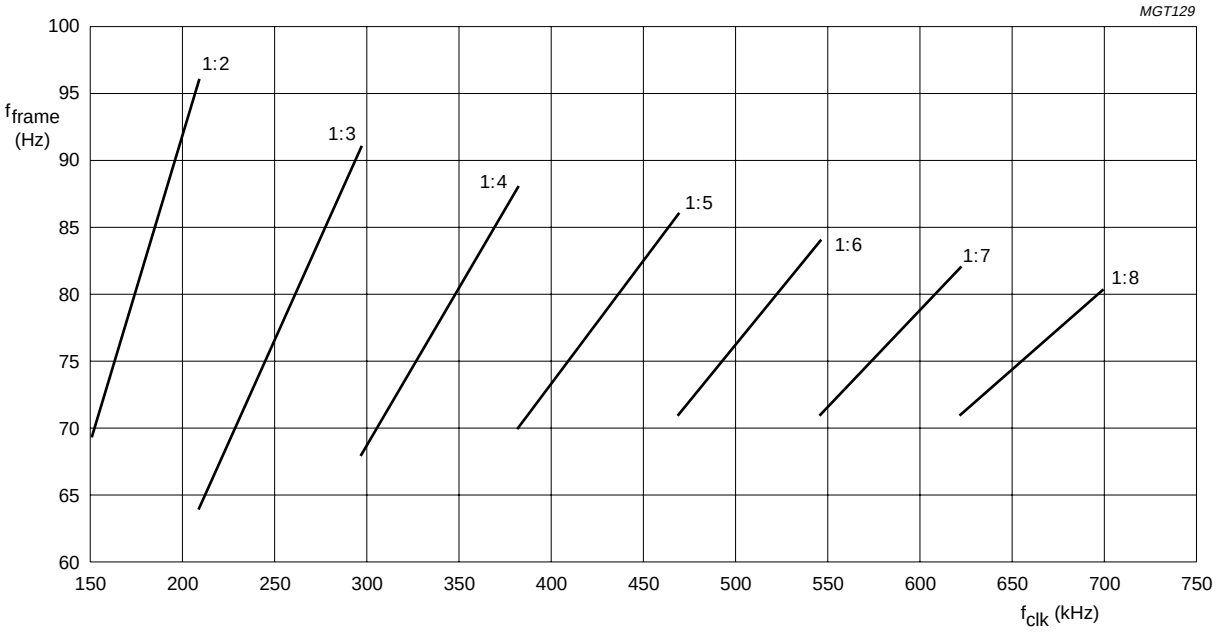
8.2 Reset and initialization

After power-on the content of all internal registers including the DDRAM are in an undefined state. A reset pulse must be applied within a specified time to reset all internal registers. A reset can be achieved by applying an external reset pulse (active LOW) to pad $\overline{RES}$. When reset occurs within the specified time all internal registers are reset, however the DDRAM is still undefined.

After V_{DD1} has reached its minimum value, the $\overline{RES}$ input level must be $\leq 0.3V_{DD1}$ after a maximum time t_{su} (see Fig.24).

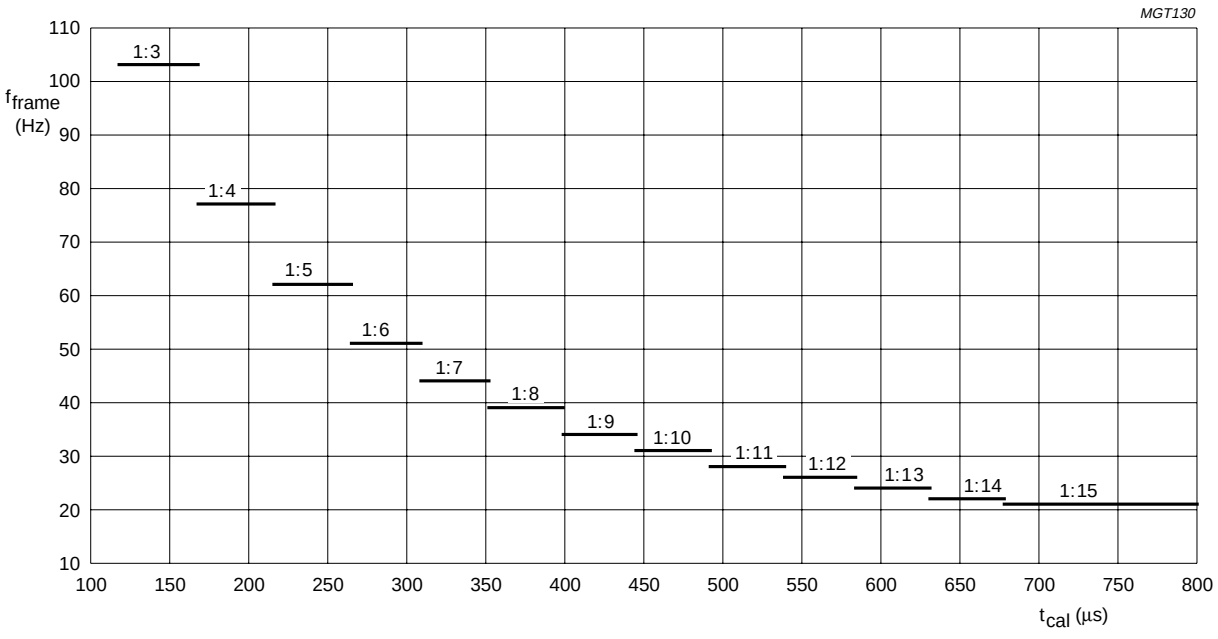
After reset the state of the PCF8820 is as follows:

- Default values of bits and registers as seen in Table 3
- All row and column outputs are at V_{SS} (display off)
- V_{LCDOUT} is high-impedance
- RAM data is undefined.



t_{cal} = 190 µs.

Fig.21 Calibrated frame frequency as a function of clock frequency and pre-divider ratio.



f_{clk} = 336 kHz.

Fig.22 Frame frequency as a function of the calibration time and pre-divider ratio.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_{LCDIN}	supply voltage for the LCD	–0.5	+15	V
V_n	voltage on			V
	any V_{LCD} related pin	–0.5	V_{LCDIN} + 0.5	V
	any other pin	–0.5	V_{DD1} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{SS}	ground supply current	–50	+50	mA
P_{tot}	total power dissipation	–	100	mW
P/out	power dissipation per output	–	10	mW
T_{amb}	ambient temperature	–40	+85	°C
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C

Note

1. All voltages are referred to V_{SS} = 0 V. Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. Parameters are valid over operating temperature range unless otherwise specified.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

11 CHARACTERISTICS

V_{DD1} = 2.5 to 5.5 V; V_{DD2} = V_{DD3} = 2.7 to 5.5 V; V_{SS1} = V_{SS2} = 0 V; V_{LCDIN} = 4.5 to 14.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	supply voltage 1 of logic circuits		2.5	–	5.5	V
V_{DD2}	supply voltage 2 of voltage multiplier		2.7	–	5.5	V
V_{DD3}	supply voltage 3 of voltage multiplier		2.7	–	5.5	V
V_{LCDIN}	supply voltage of LCD	graphic mode	7.0	–	14.5	V
		partial screen mode; note 1	V_{DD}	–	14.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(tot)}$	total supply current into pins V_{DD1}, V_{DD2} and V_{DD3}	Power-down mode; V_{LCDIN} = 8.6 V (external); notes 2 and 3	–	0.5	10	μA
		partial screen mode; V_{LCDIN} = 4.5 V (external); note 3	–	15	35	μA
		partial screen mode; V_{LCDIN} = 4.5 V (internal); LCD load is 10 μA; voltage multiplier factor 3; bias system = $^1/_6$; notes 3 and 4	–	210	300	μA
		normal mode; V_{LCDIN} = 8.6 V (external); note 3	–	20	35	μA
		normal mode; V_{LCDIN} = 8.6 V (internal); LCD load is 10 μA; voltage multiplier factor 5; bias system = $^1/_9$; notes 3 and 4	–	430	680	μA
I_{LCDIN}	supply current of V_{LCDIN}	Power-down mode; V_{LCDIN} = 8.6 V (external); bias system = $^1/_9$; V_{LCD} control value = 28H; bit PRS = 1; notes 3 and 5	–	6	15	μA
		partial screen mode; V_{LCDIN} = 4.5 V (external); LCD load is 10 μA; bias system = $^1/_6$; V_{LCD} control value = 00H; bit PRS = 0; notes 3, 4 and 5	–	45	70	μA
		normal mode; V_{LCDIN} = 8.6 V (external); LCD load is 10 μA; bias system = $^1/_9$; V_{LCD} control value = 5CH; bit PRS = 0; notes 3, 4 and 5	–	60	95	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic inputs						
PADS SA0, SA1, $\overline{RES}$, T1, T3, T4 and T5						
V_{IL}	LOW-level input voltage		V_{SS1}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
I_L	leakage current	$V_I = V_{DD1}$ or V_{SS1}	–1	–	+1	µA
PAD OSC						
V_I	LOW-level input voltage		V_{SS1}	–	V_{SS1} + 0.1	V
V_I	HIGH-level input voltage		V_{DD1} – 0.1	–	V_{DD1}	V
I_L	leakage current	$V_I = V_{DD1}$ or V_{SS1}	–1	–	+1	µA
I^2C-bus						
PADS SDA_IN and SCL						
V_{IL}	LOW-level input voltage		V_{SS1}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	5.5	V
I_L	leakage current	$V_I = V_{DD1}$ or V_{SS1}	–1	–	+1	µA
PAD SDA_OUT						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD1} = 5 V	3.0	–	–	mA
I_L	leakage current	$V_I = V_{DD1}$ or V_{SS1}	–1	–	+1	µA
Column and row outputs						
R_{col}	column output resistance C0 to C100	V_{DD1} = 5 V; V_{LCDIN} = 12 V; I_L = 100 µA; outputs tested one at a time	–	–	10	kΩ
R_{row}	row output resistance R0 to R66	V_{DD1} = 5 V; V_{LCDIN} = 12 V; I_L = 100 µA; outputs tested one at a time	–	–	3.0	kΩ
$V_{bias(col)}$	bias voltage tolerance C0 to C100		–100	0	+100	mV
$V_{bias(row)}$	bias voltage tolerance R0 to R66		–100	0	+100	mV
LCD supply voltage generator						
STABILITY						
ΔV_{LCDOUT}	tolerance of internally generated V_{LCDOUT}	T_{amb} = –20 to +85 °C; $V_{LCDOUT} \leq 12$ V	–	–	4.6	%
TEMPERATURE COEFFICIENT OF V_{LCDOUT}; T_{amb} = –20 TO +85 °C						
TC_0	temperature coefficient 0		–	-0.04×10^{-3}	–	K^{-1}
TC_1	temperature coefficient 1		–	-1.89×10^{-3}	–	K^{-1}
TC_2	temperature coefficient 2		–	-2.05×10^{-3}	–	K^{-1}
TC_3	temperature coefficient 3		–	-2.22×10^{-3}	–	K^{-1}
TC_4	temperature coefficient 4		–	-2.38×10^{-3}	–	K^{-1}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TC_5	temperature coefficient 5		–	-2.55×10^{-3}	–	K^{-1}
TC_6	temperature coefficient 6		–	-2.72×10^{-3}	–	K^{-1}
TC_7	temperature coefficient 7		–	-2.98×10^{-3}	–	K^{-1}
REFERENCE TEMPERATURE						
T_{cp}	cut-point temperature		–	23	–	°C
Temperature read-out						
a	conversion constant		–	1.13	–	°C/bit
a_{tol}	tolerance of a	same supply voltage V_{DD}	–	–	10	%
		repeatability	–	–	1	bit
		affect of changing V_{DD}	–	–	0.5	bit/V

Notes

1. The minimum value for V_{LCDIN} is limited by the supply voltages V_{DD1} and V_{DD2}:
   a) For $V_{DD1} \leq 4.5$ V and $V_{DD2} \leq 4.5$ V: $V_{LCDIN} > 4.5$ V.
   b) For $V_{DD1} > 4.5$ V or $V_{DD2} > 4.5$ V: V_{LCDIN} > highest value of V_{DD1} or V_{DD2}.
2. All static currents are switched off in Power-down mode; no external clock.
3. $V_{DD1} = V_{DD2} = V_{DD3} = 2.75$ V; LCD outputs are open-circuit; inputs connected to V_{DD1} or V_{SS1}; I^2C-bus inactive; external clock with $f_{ext} = 336$ kHz; $T_{amb} = 27$ °C.
4. The typical currents are measured on a sample base with the DDRAM and grey-scale registers loaded with data which would produce the display shown in Fig.23 if an LCD was connected. Extensive use of grey-scales will increase current consumption compared to black and white mode. If specified, the maximum current is tested with a regular pattern which is equivalent in current to the display shown in Fig.23.
5. Voltage multiplier disabled; pins V_{LCDIN}, V_{LCDOUT} and $V_{LCDSENSE}$ connected together.

Fig.23 Display used to define DDRAM and grey-scales for current measurements.

12 TIMING

V_{DD1} = 2.5 to 5.5 V; V_{DD2} = V_{DD3} = 2.7 to 5.5 V; V_{SS1} = V_{SS2} = 0 V; V_{LCDIN} = 4.5 to 14.5 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock signal						
f_{frame}	LCD frame frequency	not calibrated; note 1	44	77	158	Hz
$f_{frame(cal1)}$	LCD frame frequency	calibrated; accurate calibration timing of 190 µs; note 2	68	77	91	Hz
$f_{frame(cal2)}$	LCD frame frequency	calibrated; accurate calibration timing of 190 µs	63	77	96	Hz
f_{osc}	oscillator frequency	not calibrated; note 3	190	336	670	kHz
PAD OSC						
f_{ext}	external clock frequency	not calibrated	190	336	670	kHz
Reset timing; see Fig.24						
PAD $\overline{RES}$						
t_{WL}	reset pulse width LOW		1.0	–	–	µs
t_{WH}	reset pulse width HIGH		1.5	–	–	µs
$t_{W(spike)}$	tolerable spike width on $\overline{RES}$ input		–	–	10	ns
t_{su}	reset-LOW pulse set-up time after power-on	V_{DD} = 2.75 V; note 4	–	–	30	µs
t_{oper}	end of reset to interface being operational		–	–	3	µs
LCD on and off timing; see Fig.25						
PAD V_{LCDIN}						
$t_{LCD(on)}$	external LCD turn-on time	after V_{DD1} turns on	1	–	–	ms
$t_{LCD(off)}$	external LCD turn-off time	before V_{DD1} turns off	1	–	–	ms
I^2C-bus timing; see Fig.26; note 5						
PADS SCL and SDA						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
t_r	rise time SDA and SCL	note 6	20 + 0.1 C_b	–	300	ns
t_f	fall time SDA and SCL	note 6	20 + 0.1 C_b	–	300	ns
C_b	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	set-up time repeated START		0.6	–	–	µs
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
$t_{W(spike)}$	tolerable spike width on bus		–	–	50	ns
t_{BUF}	BUS free time		1.3	–	–	µs

Notes

1. Frame frequency: $f_{frame} = \frac{f_{ext}}{4352}$ or $f_{frame} = \frac{f_{osc}}{4352}$
2. V_{DD} unchanged after frequency calibration.
3. Not available at any pad.
4. Decoupling capacitor between V_{LCDIN} and V_{SS1} is 100 nF. A higher capacitance increases t_{su} and a higher V_{DD1}, V_{DD2} or V_{DD3} reduces t_{su}.
5. All timing values are valid within V_{DD1}, V_{DD2}, V_{DD3} and T_{amb} ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing from V_{SS1} to V_{DD1}.
6. C_b is the total capacitance (in pF) of one bus line.

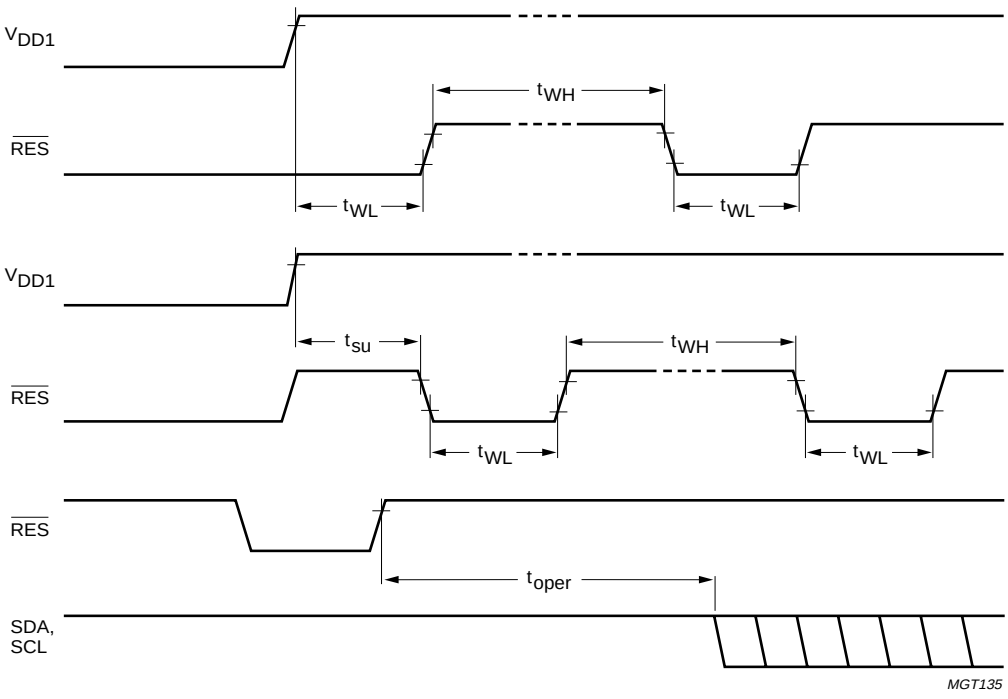


Fig.24 Reset timing.

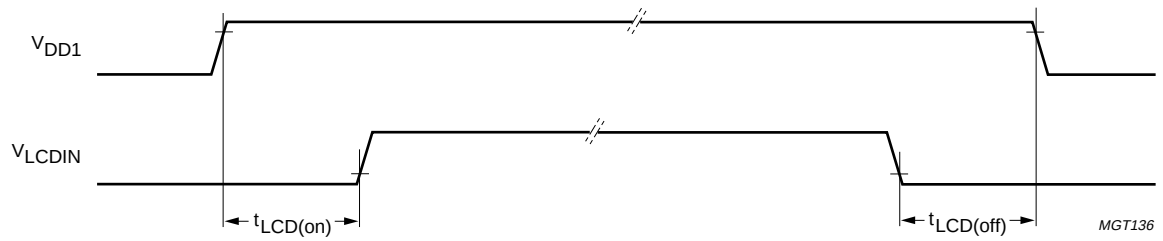


Fig.25 Timing diagram of applying and removing the external LCD supply voltage to and from pad V_{LCDIN}.

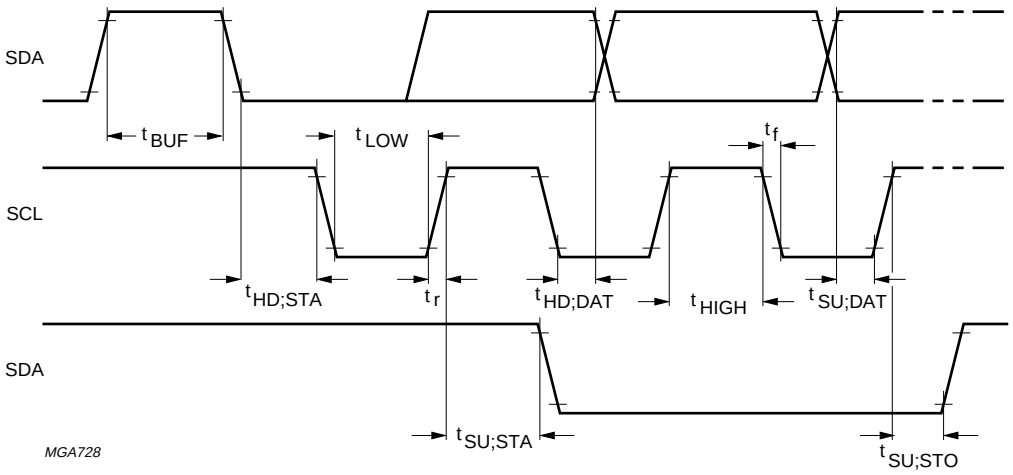


Fig.26 I^2C-bus timing.

13 APPLICATION INFORMATION

13.1 Programming example for the PCF8820

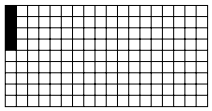
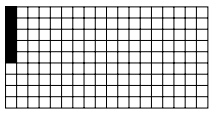
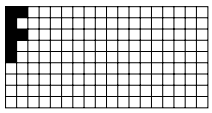
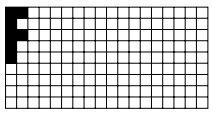
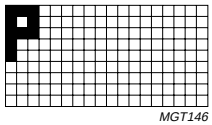
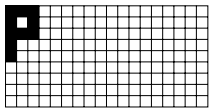
It should be noted that only a part of the LCD is shown in the LCD column of Table 9.

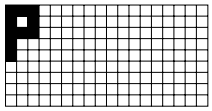
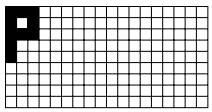
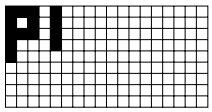
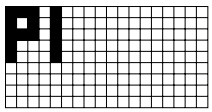
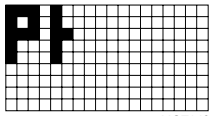
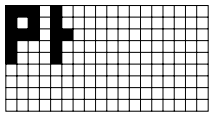
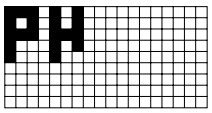
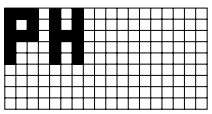
Table 9 Programming example

STEP	SERIAL BUS BYTE								LCD	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	0	1	1	1	1	SA1	SA0	0		start slave address, R/$\overline{W}$ = 0
2	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
3	0	0	0	0	0	0	0	1		H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)
4	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
5	0	0	0	0	1	0	0	1		function and RAM command page: select display setting command page (H_2 to H_0 = 001)
6	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
7	0	0	0	0	0	1	1	0		display setting command page: set normal display mode (D = 1, E = 0)
8	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
9	0	0	0	1	0	0	1	0		display setting command page: set bias system = $^1/_9$ (BS_2 to BS_0 = 010)
10	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
11	0	1	0	0	0	0	0	0		display setting command page: select first 8 rows for partial screen mode (DP_2 to DP_0 = 000)
12	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
13	0	0	0	0	0	0	0	1		H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)
14	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
15	0	0	0	1	0	1	1	0		function and RAM command page: select Power-down mode (PD = 1) and vertical address mode (V = 1)
16	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
17	0	0	0	0	1	1	0	0		function and RAM command page: select special feature command page (H_2 to H_0 = 100)
18	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
19	0	0	0	0	0	1	0	1		special feature command page: enable display (DOF = 0) and enable direct drive (DM = 1) to pre-charge the charge pump
20	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0

STEP	SERIAL BUS BYTE								LCD	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
21	0	0	0	0	0	0	0	1		H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)
22	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
23	0	0	0	0	1	0	1	0		function and RAM command page: select HVGen command page (H_2 to H_0 = 010)
24	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
25	0	0	0	0	1	0	0	0		HVGen command page: select voltage multiplier factor 2× (S_2 to S_0 = 000)
26	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
27	0	0	0	1	0	0	1	0		HVGen command page: select temperature coefficient 2 (TC_2 to TC_0 = 010)
28	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
29	0	0	0	0	0	1	0	0		HVGen command page: select LOW V_{LCD} programming range (PRS = 0), HVGen off (HVE = 0)
30	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
31	1	1	0	1	1	0	1	1		HVGen command page: set V_{LCD} to 8.595 V (V_{OP6} to V_{OP0} = 1011011)
32	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
33	0	0	0	0	0	0	0	1		H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)
34	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
35	0	0	0	0	1	0	1	1		function and RAM command page: select grey-scale/colour command page (H_2 to H_0 = 011)
36	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
37	0	1	0	0	0	0	0	0		grey-scale/colour command page: select grey-scale register 0 (GR_1 to GR_0 = 00)
38	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
39	1	0	0	0	0	0	0	0		grey-scale/colour command page: set grey-scale to 0 (GS_5 to GS_0 = 000000)
40	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
41	0	1	0	0	0	0	0	1		grey-scale/colour command page: select grey-scale register 1 (GR_1 to GR_0 = 01)
42	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0

STEP	SERIAL BUS BYTE								LCD	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
43	1	0	0	1	0	1	0	0		grey-scale/colour command page: set grey-scale to 20 (GS_5 to GS_0 = 010100)
44	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
45	0	1	0	0	0	0	1	0		grey-scale/colour command page: select grey-scale register 2 (GR_1 to GR_0 = 10)
46	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
47	1	0	1	0	1	0	0	0		grey-scale/colour command page: set grey-scale register 2 to 40 (GS_5 to GS_0 = 101000)
48	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
49	0	1	0	0	0	0	1	1		grey-scale/colour command page: select grey-scale register 3 (GR_1 to GR_0 = 11)
50	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
51	1	0	1	1	1	1	1	1		grey-scale/colour command page: set grey-scale register 3 to 63 (GS_5 to GS_0 = 111111)
52	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
53	0	0	0	0	0	0	0	1		H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)
54	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
55	0	0	0	0	1	0	1	0		function and RAM command page: select HVGen command page (H_2 to H_0 = 010)
56	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
57	0	0	0	0	0	1	0	1		HVGen command page: enable HVGen (HVE = 1) and select LOW V_{LCD} programming range (PRS = 0)
58	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
59	0	0	0	0	0	0	0	1		H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)
60	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
61	0	0	0	1	0	0	1	0		function and RAM command page: select normal operation (PD = 0) and vertical address mode (V = 1)
62	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
63	0	0	0	0	1	0	1	0		function and RAM command page: select HVGen command page (H_2 to H_0 = 010)

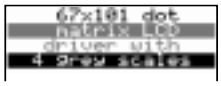
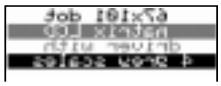
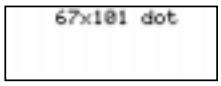
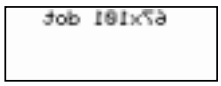
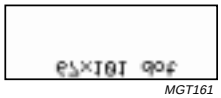
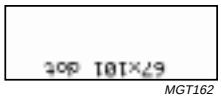
STEP	SERIAL BUS BYTE								LCD	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
64	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
65	0	0	0	0	1	0	0	1		HVGen command page: select voltage multiplier factor 3× (S_2 to S_0 = 001, incremented to 3x)
66	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
67	0	0	0	0	1	0	1	0		HVGen command page: select voltage multiplier factor 4 (S_2 to S_0 = 010)
68	1	0	0	0	0	0	0	0		control byte: Co = 1, RS = 0
69	0	0	0	0	1	0	1	1		HVGen command page: select voltage multiplier factor 5 (S_2 to S_0 = 011, incremented to 5x)
70	0	1	0	0	0	0	0	0		control byte: Co = 0, RS = 1
71	1	1	1	1	1	1	1	1	 MGT143	data write column 0 (vertical addressing): address X and Y are initialized to 0 by default, so they are not set here
72	0	0	0	0	0	0	1	1	 MGT144	data write: next write to subsequent rows filling up column 0 with ‘00H’
73 to 89	0	0	0	0	0	0	0	0	no display change	data writes (17 bytes)
90	0	0	1	1	0	0	1	1	 MGT145	data write column 1 (vertical addressing)
91	0	0	0	0	0	0	0	0	 MGT145	data write
92 to 108	0	0	0	0	0	0	0	0	no display change	data writes (17 bytes)
109	0	0	1	1	1	1	1	1	 MGT146	data write column 2 (vertical addressing)
110	0	0	0	0	0	0	0	0	 MGT146	data write
111 to 127	0	0	0	0	0	0	0	0	no display change	data writes (17 bytes)

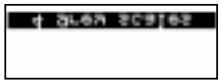
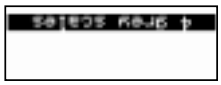
STEP	SERIAL BUS BYTE								LCD	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
128	0	0	0	0	0	0	0	0	 MGT146	data write column 3 (vertical addressing)
129	0	0	0	0	0	0	0	0	 MGT146	data write
130 to 146	0	0	0	0	0	0	0	0	no display change	data writes (17 bytes)
147	1	1	1	1	1	1	1	1	 MGT147	data write column 4 (vertical addressing)
148	0	0	0	0	0	0	1	1	 MGT148	data write
149 to 165	0	0	0	0	0	0	0	0	no display change	data writes (17 bytes)
166	0	0	1	1	0	0	0	0	 MGT149	data write column 5 (vertical addressing)
167	0	0	0	0	0	0	0	0	 MGT149	data write
168 to 184	0	0	0	0	0	0	0	0	no display change	data writes (17 bytes)
185	1	1	1	1	1	1	1	1	 MGT150	data write column 6 (vertical addressing)
186	0	0	0	0	0	0	1	1	 MGT151	data write: last data; stop transmission
187	0	1	1	1	1	SA1	SA0	0	no display change	restart, slave address, R/$\overline{W}$ = 0
188	1	0	0	0	0	0	0	0	no display change	control byte: Co = 1, RS = 0
189	0	0	0	0	0	0	0	1	no display change	H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)

STEP	SERIAL BUS BYTE								LCD	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
190	1	0	0	0	0	0	0	0	no display change	control byte: Co = 1, RS = 0
191	0	0	0	0	1	0	0	1	no display change	function and RAM command page: select display setting command page (H_2 to H_0 = 001)
192	1	0	0	0	0	0	0	0	no display change	control byte: Co = 1, RS = 0
193	0	0	0	0	0	1	1	1	 MGT152	display mode: set inverse video mode (D = 1, E = 1)
194	1	0	0	0	0	0	0	0	no display change	control byte: Co = 1, RS = 0
195	0	0	0	0	0	0	0	1	no display change	H_2 to H_0 independent command: select function and RAM command page (H_2 to H_0 = 000)
196	1	0	0	0	0	0	0	0	no display change	control byte: Co = 1, RS = 0
197	1	0	0	0	0	0	0	0	no display change	set X address of RAM to ‘0000000’
198	1	0	0	0	0	0	0	0	no display change	control byte: Co = 1, RS = 0
199	0	1	0	0	0	0	0	0	no display change	set Y address of RAM to ‘00000’
200	0	1	0	0	0	0	0	0	no display change	control byte: Co = 0, RS = 1
201	0	1	0	1	0	1	0	1	 MGT153	data write column 1 (vertical addressing mode)
202	0	0	0	0	0	0	0	1	 MGT154	data write: last data; stop transmission

13.2 Examples of effects on the display

Table 10 Examples showing the effects on the LCD of setting bits PS, DP_2 to DP_0, MX and MY

EXAMPLE	PS	DP_2	DP_1	DP_0	MX	MY	DISPLAY	DESCRIPTION
1	0	X	X	X	0	0	 MGT155	normal display
2	0	X	X	X	1	0	 MGT156	X mirrored only
3	0	X	X	X	0	1	 MGT157	Y mirrored only
4	0	X	X	X	1	1	 MGT158	X and Y mirrored
5	1	0	0	0	0	0	 MGT159	partial screen mode only; first 8 rows selected
6	1	0	0	0	1	0	 MGT160	partial screen mode; X mirrored; first 8 rows selected
7	1	0	0	0	0	1	 MGT161	partial screen mode; Y mirrored; first 8 rows selected
8	1	0	0	0	1	1	 MGT162	partial screen mode; X and Y mirrored; first 8 rows selected
9	1	1	1	1	0	0	 MGT163	partial screen mode; last 8 rows selected

EXAMPLE	PS	DP_2	DP_1	DP_0	MX	MY	DISPLAY	DESCRIPTION
10	1	1	1	1	1	0	 MGT164	partial screen mode; X mirrored; last 8 rows selected
11	1	1	1	1	0	1	 MGT165	partial screen mode; Y mirrored; last 8 rows selected
12	1	1	1	1	1	1	 MGT166	partial screen mode; X and Y mirrored; last 8 rows selected

13.3 High voltage generator

The high voltage generator contains a voltage multiplier which uses a charge pump circuit supplied by V_{DD2} and V_{DD3}. The multiplier is software programmable with a factor from 2 to 8. In the direct drive mode the output voltage $V_{LCDOUT} = V_{DD2}$.

When the charge pump is used the total supply current of the PCF8820 at a supply voltage of 3, 4 and 5 V is shown in Figs 27, 28 and 29.

The separate graphs are shown for each voltage multiplier factor with the following conditions:

- At T_{amb}
- V_{DD1}, V_{DD2} and V_{DD3} connected to the same power supply
- Supply line resistors of 50 Ω (typical value)
- Internal clock not calibrated
- No LCD connected to the PCF8820
- All pixels defined at grey-scale level 32; this is the worst case
- Bias system 1/9
- Full screen mode (bit PS = 0) at a multiplex rate of 1 : 67
- Normal display mode.

The characteristics shown for each voltage multiplier factor are terminated before V_{LCDOUT} has been reached the maximum value to indicate that the voltage cannot be increased any further. If a higher voltage is required, a higher voltage multiplier factor must be selected.

Connecting a LCD may increase the current into pad V_{LCDIN} which may affect the current taken by the charge pump and also its efficiency. The amount of current load may depend on the type of LCD used.

It is advisable to evaluate the PCF8820 connected to the desired LCD and set to the required mode(s) to produce characteristics similar to Figs 27, 28 and 29. The customer can then use these graphs to select the most efficient and safe voltage multiplier factor for each mode required.

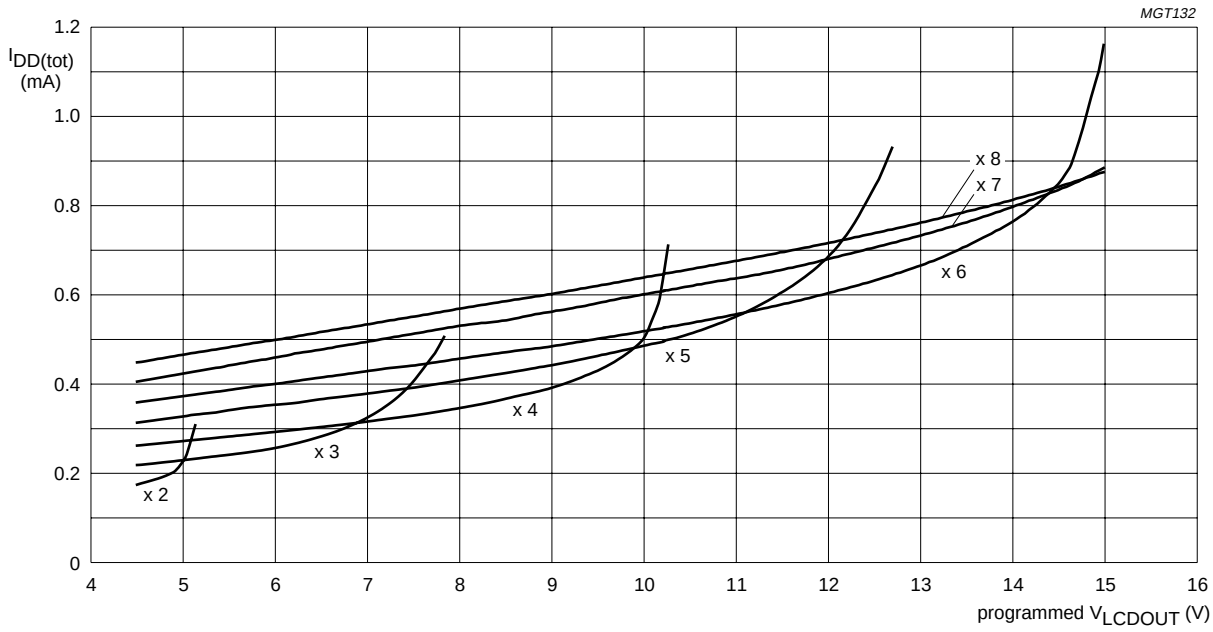


Fig.27 Charge pump characteristics for V_{DD} = 3 V.

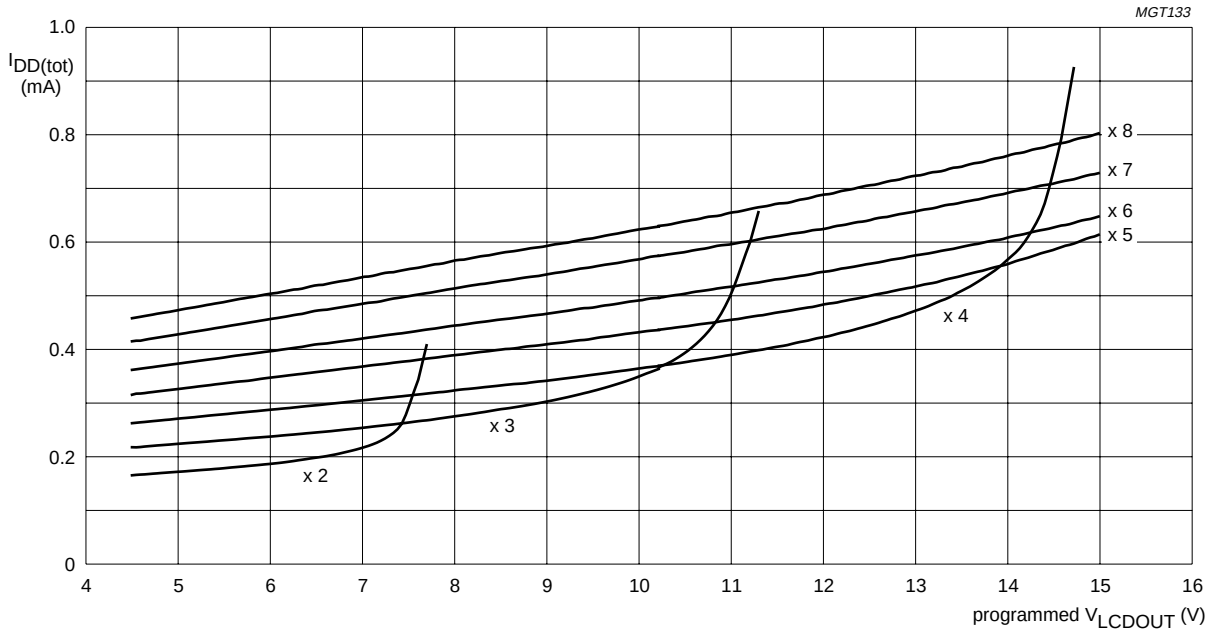


Fig.28 Charge pump characteristics for V_{DD} = 4 V.

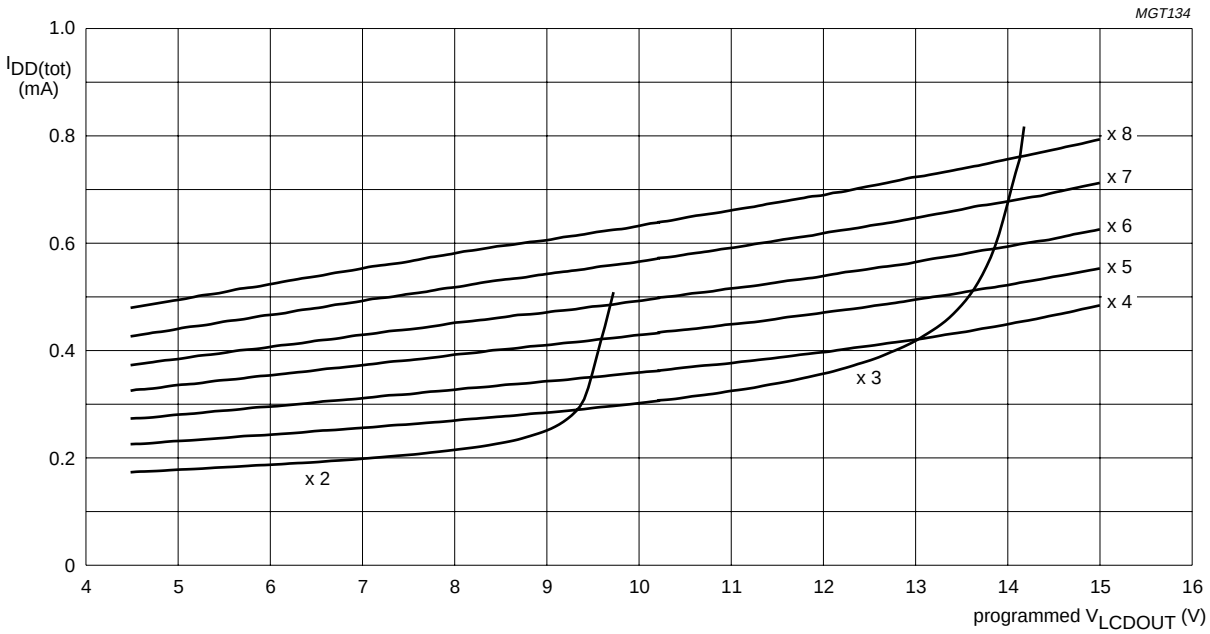


Fig.29 Charge pump characteristics for V_{DD} = 5 V.

13.4 Application for COG

The PCF8820 physical pad positions are optimized for single plane wiring e.g. for Chip-On-Glass (COG) display modules (see Fig.30). The pad lines are as follows:

- 3 input/output lines: SDA, SCL and $\overline{RES}$
- 101 column driver lines
- 33 and 34 row driver lines
- pads SA0, SA1 and OSC can be tied in the application to appropriate levels.

For COG applications, it is recommended that the Indium Tin Oxide (ITO) track resistance is minimized for the I/O and power supply connections. These connections should have an optimum track resistance of <50 Ω for the power supply connections and <100 Ω for the I/O connections. Increasing the track resistance reduces the performance and increases the current consumption.

The common supply resistor values especially, have to be minimized (<5 Ω for high supply voltage V_{P1}, V_{LCD} and GND).

The minimum value required for the external capacitors is:

- C_{ext1} > 470 nF (C_{ext1} > C_{ext2} recommended)
- C_{ext2} > 100 nF (470 nF to 1 μF recommended).

A higher value of the capacitors is recommended to reduce the ripple voltage.

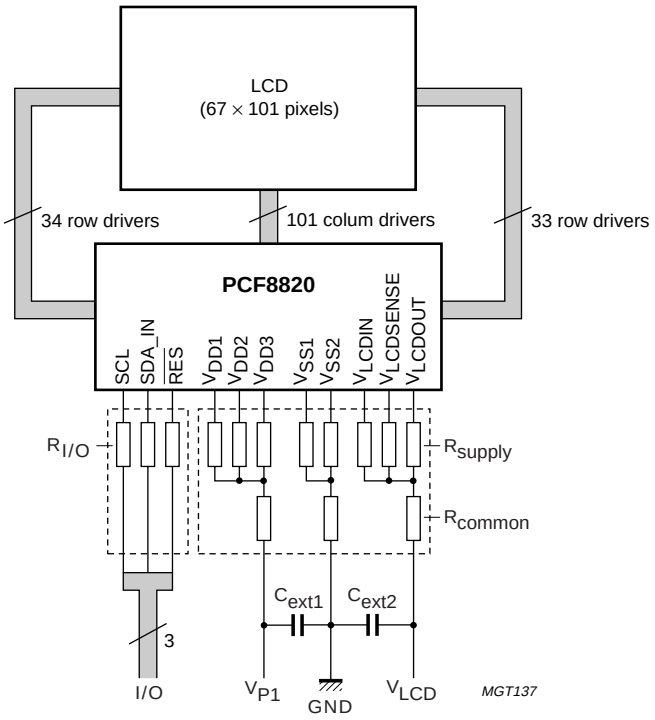


Fig.30 Application diagram for COG display module.

13.5 Typical system configuration

The PCF8820 is a low power LCD driver designed to interface with microcontrollers and a wide variety of LCDs.

The host microcontroller and the PCF8820 are both connected to the I²C-bus. The SDA and SCL lines must be connected to the positive power supply via pull-up resistors.

The internal oscillator requires no external components.

The appropriate intermediate biasing voltage for the multiplexed LCD waveforms are generated on-chip.

The only other connections required to complete the system are the power supplies (V_{DD1}, V_{DD2} and V_{DD3}) and ground supplies (V_{SS1} and V_{SS2}), LCD supply (V_{LCDIN}) and system reset ($\overline{RES}$), including suitable capacitors for decoupling.

13.6 External supply of V_{LCDIN}

If an external LCD supply voltage is used, it must be connected to pad V_{LCDIN}. If pads V_{LCDOUT}, $V_{LCDSENSE}$ and V_{LCDIN} are connected together, the impedance of pad V_{LCDOUT} should be set high-impedance by setting the status of bits shown in Table 8. To obtain the highest resistance and the lowest current into pad $V_{LCDSENSE}$, it is recommended to set the V_{LCD} programming range to HIGH (bit PRS = 1) and the V_{LCD} control register value to 127 (maximum value) with bits V_{OP6} to V_{OP0}.

It should be noted that V_{LCDIN} is not allowed to be lower than V_{DD1}.

An external V_{LCD} must be applied after applying V_{DD1}, and it must be turned off before (or when) V_{DD1} is turned off (see Fig.25). It is recommended that the external V_{LCD} is applied after leaving the reset state. The external V_{LCD} can stay turned on in Power-down mode.

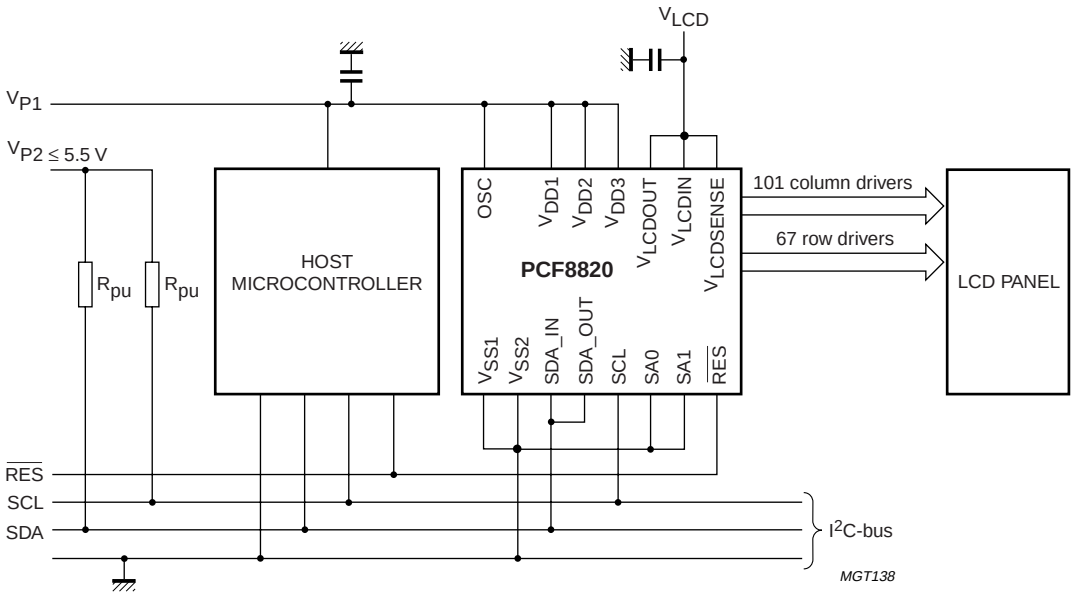


Fig.31 Typical system configuration.

14 BONDING PAD INFORMATION

SYMBOL	PAD	COORDINATES(1)	
		x	y
dummy	1	–5443.7	–1162.5
dummy	2	–5373.7	–1162.5
row 0	3	–5233.7	–1162.5
row 1	4	–5163.7	–1162.5
row 2	5	–5093.7	–1162.5
row 3	6	–5023.7	–1162.5
row 4	7	–4953.7	–1162.5
row 5	8	–4883.7	–1162.5
row 6	9	–4813.7	–1162.5
row 7	10	–4743.7	–1162.5
row 8	11	–4673.7	–1162.5
row 9	12	–4603.7	–1162.5
row 10	13	–4533.7	–1162.5
row 11	14	–4463.7	–1162.5
row 12	15	–4393.7	–1162.5
row 13	16	–4323.7	–1162.5
row 14	17	–4253.7	–1162.5
row 15	18	–4183.7	–1162.5
row 16	19	–4113.7	–1162.5
row 17	20	–4043.7	–1162.5
row 18	21	–3973.7	–1162.5
row 19	22	–3903.7	–1162.5
row 20	23	–3833.7	–1162.5
row 21	24	–3763.7	–1162.5
row 22	25	–3693.7	–1162.5
col 0	26	–3483.7	–1162.5
col 1	27	–3413.7	–1162.5
col 2	28	–3343.7	–1162.5
col 3	29	–3273.7	–1162.5
col 4	30	–3203.7	–1162.5
col 5	31	–3133.7	–1162.5
col 6	32	–3063.7	–1162.5
col 7	33	–2993.7	–1162.5
col 8	34	–2923.7	–1162.5
col 9	35	–2853.7	–1162.5
col 10	36	–2783.7	–1162.5
col 11	37	–2713.7	–1162.5
col 12	38	–2643.7	–1162.5
col 13	39	–2573.7	–1162.5
col 14	40	–2503.7	–1162.5
col 15	41	–2433.7	–1162.5
col 16	42	–2363.7	–1162.5
col 17	43	–2293.7	–1162.5
col 18	44	–2223.7	–1162.5
col 19	45	–2153.7	–1162.5
col 20	46	–2083.7	–1162.5
col 21	47	–2013.7	–1162.5
col 22	48	–1943.7	–1162.5
col 23	49	–1873.7	–1162.5
col 24	50	–1803.7	–1162.5
col 25	51	–1663.7	–1162.5
col 26	52	–1593.7	–1162.5
col 27	53	–1523.7	–1162.5
col 28	54	–1453.7	–1162.5
col 29	55	–1383.7	–1162.5
col 30	56	–1313.7	–1162.5
col 31	57	–1243.7	–1162.5
col 32	58	–1173.7	–1162.5
col 33	59	–1103.7	–1162.5
col 34	60	–1033.7	–1162.5
col 35	61	–963.7	–1162.5
col 36	62	–893.7	–1162.5
col 37	63	–823.7	–1162.5
col 38	64	–753.7	–1162.5
col 39	65	–683.7	–1162.5
col 40	66	–613.7	–1162.5
col 41	67	–543.7	–1162.5
col 42	68	–473.7	–1162.5
col 43	69	–403.7	–1162.5
col 44	70	–333.7	–1162.5
col 45	71	–263.7	–1162.5
col 46	72	–193.7	–1162.5
col 47	73	–123.7	–1162.5
col 48	74	–53.7	–1162.5
col 49	75	+16.3	–1162.5
col 50	76	+156.3	–1162.5
col 51	77	+226.3	–1162.5

SYMBOL	PAD	COORDINATES(1)	
		x	y
col 52	78	+296.3	−1162.5
col 53	79	+366.3	−1162.5
col 54	80	+436.3	−1162.5
col 55	81	+506.3	−1162.5
col 56	82	+576.3	−1162.5
col 57	83	+646.3	−1162.5
col 58	84	+716.3	−1162.5
col 59	85	+786.3	−1162.5
col 60	86	+856.3	−1162.5
col 61	87	+926.3	−1162.5
col 62	88	+996.3	−1162.5
col 63	89	+1066.3	−1162.5
col 64	90	+1136.3	−1162.5
col 65	91	+1206.3	−1162.5
col 66	92	+1276.3	−1162.5
col 67	93	+1346.3	−1162.5
col 68	94	+1416.3	−1162.5
col 69	95	+1486.3	−1162.5
col 70	96	+1556.3	−1162.5
col 71	97	+1626.3	−1162.5
col 72	98	+1696.3	−1162.5
col 73	99	+1766.3	−1162.5
col 74	100	+1836.3	−1162.5
col 75	101	+1976.3	−1162.5
col 76	102	+2046.3	−1162.5
col 77	103	+2116.3	−1162.5
col 78	104	+2186.3	−1162.5
col 79	105	+2256.3	−1162.5
col 80	106	+2326.3	−1162.5
col 81	107	+2396.3	−1162.5
col 82	108	+2466.3	−1162.5
col 83	109	+2536.3	−1162.5
col 84	110	+2606.3	−1162.5
col 85	111	+2676.3	−1162.5
col 86	112	+2746.3	−1162.5
col 87	113	+2816.3	−1162.5
col 88	114	+2886.3	−1162.5
col 89	115	+2956.3	−1162.5
col 90	116	+3026.3	−1162.5

SYMBOL	PAD	COORDINATES(1)	
		x	y
col 91	117	+3096.3	−1162.5
col 92	118	+3166.3	−1162.5
col 93	119	+3236.3	−1162.5
col 94	120	+3306.3	−1162.5
col 95	121	+3376.3	−1162.5
col 96	122	+3446.3	−1162.5
col 97	123	+3516.3	−1162.5
col 98	124	+3586.3	−1162.5
col 99	125	+3656.3	−1162.5
col 100	126	+3726.3	−1162.5
row 55	127	+3866.3	−1162.5
row 54	128	+3936.3	−1162.5
row 53	129	+4006.3	−1162.5
row 52	130	+4076.3	−1162.5
row 51	131	+4146.3	−1162.5
row 50	132	+4216.3	−1162.5
row 49	133	+4286.3	−1162.5
row 48	134	+4356.3	−1162.5
row 47	135	+4426.3	−1162.5
row 46	136	+4496.3	−1162.5
row 45	137	+4566.3	−1162.5
row 44	138	+4636.3	−1162.5
row 43	139	+4706.3	−1162.5
row 42	140	+4776.3	−1162.5
row 41	141	+4846.3	−1162.5
row 40	142	+4916.3	−1162.5
row 39	143	+4986.3	−1162.5
row 38	144	+5056.3	−1162.5
row 37	145	+5126.3	−1162.5
row 36	146	+5196.3	−1162.5
row 35	147	+5266.3	−1162.5
row 34	148	+5336.3	−1162.5
dummy	149	+5476.3	−1162.5
dummy	150	+5581.3	+1162.5
row 56	151	+5301.3	+1162.5
row 57	152	+5231.3	+1162.5
row 58	153	+5161.3	+1162.5
row 59	154	+5091.3	+1162.5
row 60	155	+5021.3	+1162.5

SYMBOL	PAD	COORDINATES(1)	
		x	y
row 61	156	+4951.3	+1162.5
row 62	157	+4881.3	+1162.5
row 63	158	+4811.3	+1162.5
row 64	159	+4741.3	+1162.5
row 65	160	+4671.3	+1162.5
row 66	161	+4601.3	+1162.5
V_5	162	+4421	+1162.5
V_4	163	+4261	+1162.5
V_3	164	+4101	+1162.5
V_2	165	+3941	+1162.5
V_{LCDIN}	166	+3806.3	+1162.5
V_{LCDIN}	167	+3726.3	+1162.5
V_{LCDIN}	168	+3646.3	+1162.5
V_{LCDIN}	169	+3566.3	+1162.5
V_{LCDIN}	170	+3486.3	+1162.5
V_{LCDIN}	171	+3406.3	+1162.5
$V_{LCDSENSE}$	172	+3326.3	+1162.5
V_{LCDOUT}	173	+3246.3	+1162.5
V_{LCDOUT}	174	+3166.3	+1162.5
V_{LCDOUT}	175	+3086.3	+1162.5
V_{LCDOUT}	176	+3006.3	+1162.5
V_{LCDOUT}	177	+2926.3	+1162.5
V_{LCDOUT}	178	+2846.3	+1162.5
V_{DD1}	179	+2451.3	+1162.5
V_{DD1}	180	+2371.3	+1162.5
V_{DD1}	181	+2291.3	+1162.5
V_{DD1}	182	+2211.3	+1162.5
V_{DD1}	183	+2131.3	+1162.5
V_{DD1}	184	+2051.3	+1162.5
V_{DD3}	185	+1921.3	+1162.5
V_{DD3}	186	+1841.3	+1162.5
V_{DD3}	187	+1761.3	+1162.5
V_{DD2}	188	+1681.3	+1162.5
V_{DD2}	189	+1601.3	+1162.5
V_{DD2}	190	+1521.3	+1162.5
V_{DD2}	191	+1441.3	+1162.5
V_{DD2}	192	+1361.3	+1162.5
V_{DD2}	193	+1281.3	+1162.5
V_{DD2}	194	+1201.3	+1162.5

SYMBOL	PAD	COORDINATES(1)	
		x	y
SDA_IN	195	+573.3	+1162.5
SDA_IN	196	+493.3	+1162.5
SDA_OUT	197	+65.9	+1162.5
V_{SS2}	198	–233.7	+1162.5
V_{SS2}	199	–313.7	+1162.5
V_{SS2}	200	–393.7	+1162.5
V_{SS2}	201	–473.7	+1162.5
V_{SS2}	202	–553.7	+1162.5
V_{SS2}	203	–633.7	+1162.5
SA0	204	–833.7	+1162.5
T1	205	–1033.7	+1162.5
V_{SS1}	206	–1113.7	+1162.5
V_{SS1}	207	–1193.7	+1162.5
V_{SS1}	208	–1273.7	+1162.5
V_{SS1}	209	–1353.7	+1162.5
V_{SS1}	210	–1433.7	+1162.5
V_{SS1}	211	–1513.7	+1162.5
T3	212	–1713.7	+1162.5
T4	213	–1913.7	+1162.5
SA1	214	–2113.7	+1162.5
SCL	215	–2355	+1162.5
SCL	216	–2435	+1162.5
T5	217	–2958	+1162.5
T6	218	–3158.7	+1162.5
$\overline{RES}$	219	–3454.7	+1162.5
OSC	220	–4158.7	+1162.5
T2	221	–4282.7	+1162.5
row 33	222	–4498.7	+1162.5
row 32	223	–4568.7	+1162.5
row 31	224	–4638.7	+1162.5
row 30	225	–4708.7	+1162.5
row 29	226	–4778.7	+1162.5
row 28	227	–4848.7	+1162.5
row 27	228	–4918.7	+1162.5
row 26	229	–4988.7	+1162.5
row 25	230	–5058.7	+1162.5
row 24	231	–5128.7	+1162.5
row 23	232	–5198.7	+1162.5
dummy	233	–5478.7	+1162.5

SYMBOL	PAD	COORDINATES(1)	
		x	y
dummy	234	–5548.7	+1162.5
dummy	235	–5618.7	+1162.5
Alignment marks			
Circle 1		–5594.0	–1162.5
Circle 2		+5594.0	–1162.5
Circle 3		+5469.0	+1162.5
Circle 4		–5369.0	+1162.5

Note

1. All x/y coordinates represent the position of the centre of each pad (in μm) with respect to the centre (x/y = 0) of the chip (see Fig.32).

Table 11 Bonding pad dimensions

NAME	DIMENSION
Pad pitch	70 μm (minimum value)
Pad size, aluminium	62 × 100 μm
Passivation opening at pad	36 × 76 μm
Bump dimensions	52 × 90 × 17.5 μm
Wafer thickness (excluding bumps)	381 μm

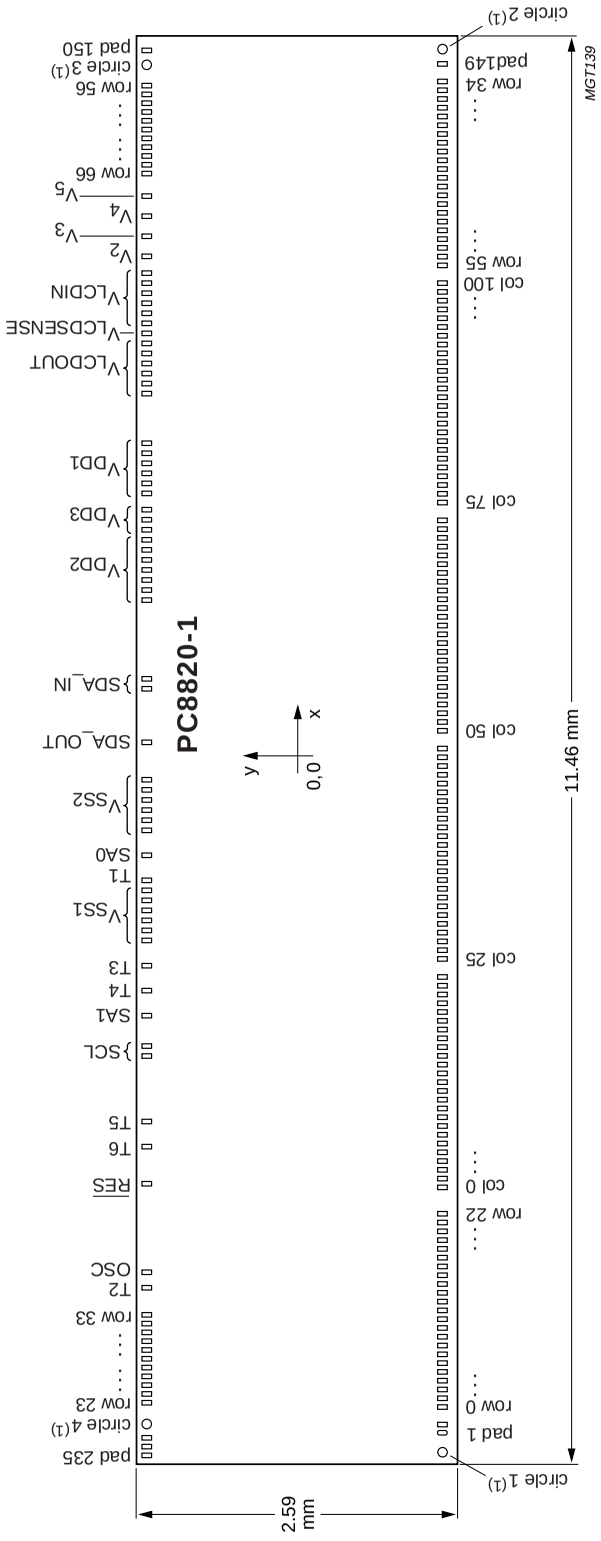
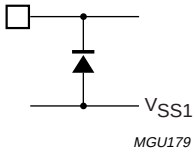
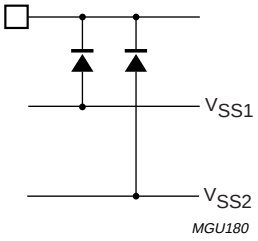
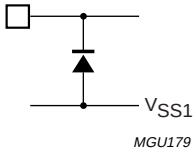
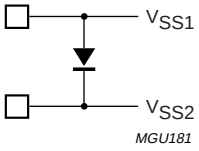
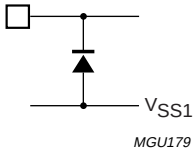
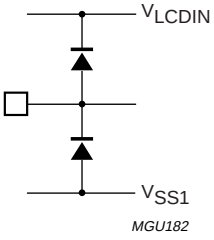
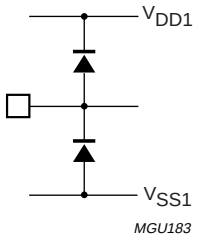
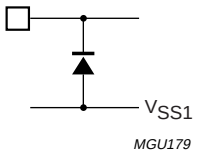
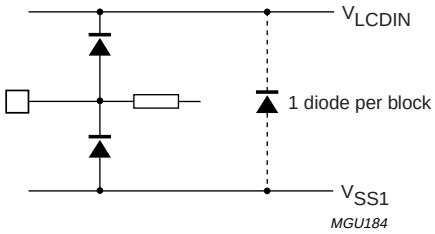


Fig.32 Bonding pad locations.

(1) Circles 1 to 4 are alignment marks with a diameter of 100 µm.

15 DEVICE PROTECTION CIRCUITS

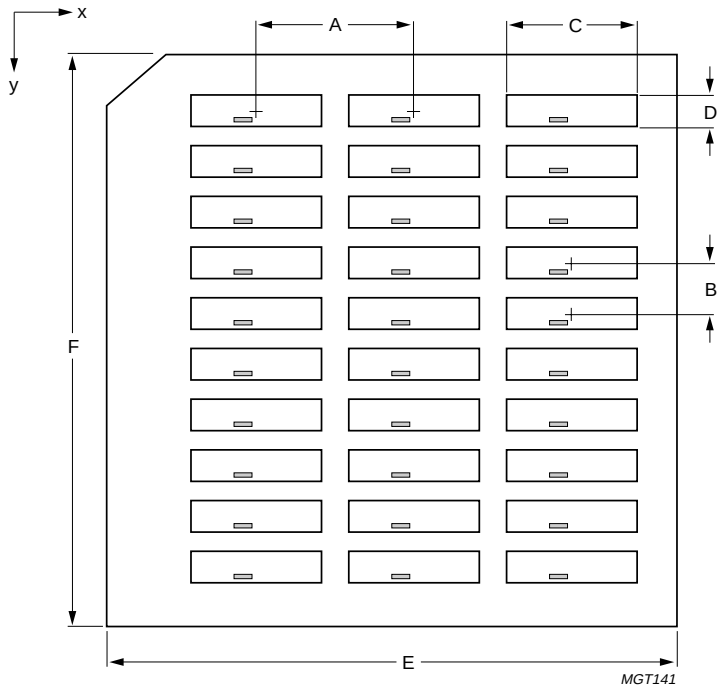
SYMBOL	PAD	REMARK	INTERNAL CIRCUIT
V_{DD1}	179 to 184	note 1	
V_{DD2}	188 to 194	note 1	
V_{DD3}	185 to 187	note 1	
V_{SS1}	206 to 211	note 1	
V_{SS2}	198 to 203	note 1	
V_{LCDIN}	166 to 171	note 1	
$V_{LCDSENSE}$	172		
V_{LCDOUT}	173 to 178	note 1	
V_2	162		
V_3	163		
V_4	164		
V_5	165		

SYMBOL	PAD	REMARK	INTERNAL CIRCUIT
SA0	204		
SA1	214		
T1	205		
T2	221		
T3	212		
T4	213		
T5	217		
T6	218		
OSC	220		
$\overline{RES}$	219		
SCL	215 and 216	note 1	
SDA_IN	195 and 196	note 1	
SDA_OUT	197		
R0 to R22 (block 1)	3 to 25		
R23 to R33 (block 2)	232 to 222		
R34 to R55 (block 3)	148 to 127		
R56 to R66 (block 4)	151 to 161		
C0 to C24 (block 5)	26 to 50		
C25 to C49 (block 6)	51 to 75		
C50 to C74 (block 7)	76 to 100		
C75 to C100 (block 8)	101 to 126		

Note

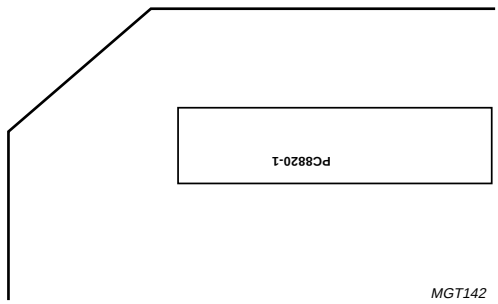
1. Internally shorted via metal.

16 TRAY INFORMATION



For the dimensions of A to F: see Table 12.

Fig.33 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to Fig.32 for the orientation and position of the type name on the die surface.

Fig.34 Tray alignment.

Table 12 Tray dimensions

DIMENSION	DESCRIPTION	VALUE
A	pocket pitch in x direction	13.77 mm
B	pocket pitch in y direction	4.45 mm
C	pocket width in x direction	11.61 mm
D	pocket width in y direction	2.75 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
–	no. pockets in x direction	3
–	no. pockets in y direction	10

17 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Note

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