DATA SHEET

PCF8812
65 × 102 pixels matrix LCD driver

Product specification
File under Integrated Circuits, IC12

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Philips
Semiconductors

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CONTENTS

65 × 102 pixels matrix LCD driver PCF8812

1 FEATURES

- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Configurable 5 (4, 3 and 2) voltage multiplier generating V_{LCD} (external V_{LCD} also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- External reset input pin
- Serial interface maximum 4.0 Mbit/s
- CMOS compatible inputs
- Mux rate: 1 : 65
- Logic supply voltage range V_{DD1} to V_{SS}:
  - 2.5 to 5.5 V.
- High voltage generator supply voltage range V_{DD2} to V_{SS} and V_{DD3} to V_{SS}
  - 2.5 to 4.5 V.
- Display supply voltage range V_{LCD} to V_{SS}:
  - 4.5 to 9.0 V.
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Temperature range: T_{amb} = –40 to +85 °C
- Slim chip layout, suited for Chip-On-Glass (COG) applications.

2 APPLICATIONS

- Telecom equipment.

3 GENERAL DESCRIPTION

The PCF8812 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8812 interfaces to microcontrollers via a serial bus interface.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8812U/2	Tray	chip with bumps in tray	–

5 BLOCK DIAGRAM

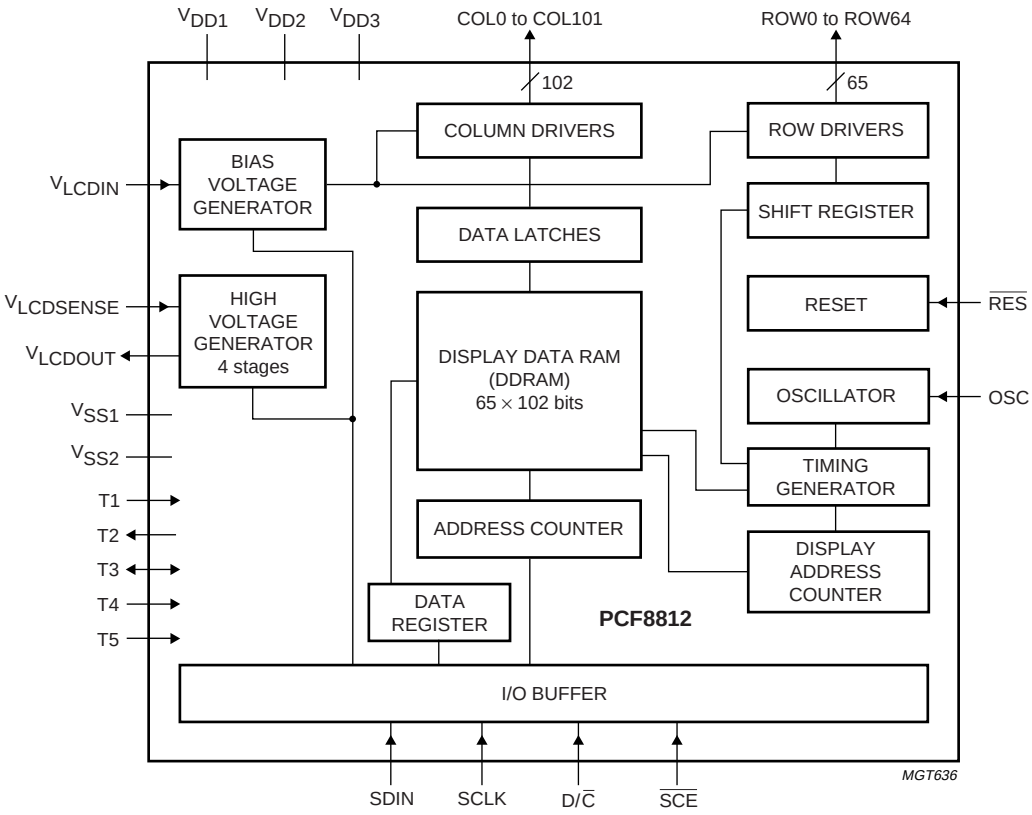


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	DESCRIPTION
$\overline{RES}$	1	external reset input (active LOW)
ROW 32 to ROW 19	2 to 15	LCD row driver outputs
ROW 0 to ROW 18	18 to 36	LCD row driver outputs
COL 0 to COL 101	37 to 138	LCD column driver outputs
ROW 50 to ROW 33	139 to 156	LCD row driver outputs
ROW 51 to ROW 64	159 to 172	LCD row driver outputs
V_{DD1}	174 to 179	supply voltage 1
V_{DD3}	180	supply voltage 3
V_{DD2}	181 to 193	supply voltage 2
OSC	194	oscillator input
SDIN	195	serial data input
D/$\overline{C}$	196	data/$\overline{command}$ input
$\overline{SCE}$	197	chip enable input (active LOW)
T2	198	test 2 output
SCLK	199	serial clock input
V_{SS2}	200 to 213	negative power supply 2
V_{SS1}	214 to 217	negative power supply 1
T1	218	test 1 input
T5	219	test 5 input
T4	220	test 4 input
V_{SS1}	221 and 222	negative power supply 1
T3	223	test 3 input/output
V_{LCDIN}	224 to 229	LCD supply voltage
V_{LCDOUT}	230 to 236	voltage multiplier output
$V_{LCDSENSE}$	237	voltage multiplier regulation input (V_{LCD})
	16, 17, 157, 158 and 173	dummy pads

7 PIN FUNCTIONS

7.1 Pin functions

7.1.1 ROW 0 TO ROW 64 ROW DRIVER OUTPUTS

These pads output the row signals.

7.1.2 COL 0 TO COL 101 COLUMN DRIVER OUTPUTS

These pads output the column signals.

7.1.3 V_{SS1} AND V_{SS2}: NEGATIVE POWER SUPPLY RAILS

The 2 supply rails V_{SS1} and V_{SS2} must be connected together.

7.1.4 V_{DD1} TO V_{DD3}: POSITIVE POWER SUPPLY RAILS

V_{DD2} and V_{DD3} are the supply voltage for the internal voltage generator. Both have the same voltage and may be connected together outside of the chip. V_{DD1} is used as supply for the rest of the chip. V_{DD1} can be connected together with V_{DD2} and V_{DD3} but in this case care must be taken to respect the supply voltage range (see Chapter 13).

If the internal voltage generator is not used then V_{DD2} and V_{DD3} must be connected to V_{DD1} or connected to power.

7.1.5 V_{LCDIN}: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. An external LCD supply voltage can be supplied using the V_{LCDIN} pad. In this case V_{LCDOUT} has to be left open-circuit and the internal voltage generator has to be programmed to zero. If the PCF8812 is in Power-down mode, the external LCD supply voltage has to be switched off.

7.1.6 V_{LCDOUT}: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCDIN} and V_{LCDOUT} must be connected together. If an external supply is used this pin must be left open-circuit.

7.1.7 $V_{LCDSENSE}$: VOLTAGE MULTIPLIER REGULATION INPUT (V_{LCD})

$V_{LCDSENSE}$ is the input of the internal voltage multiplier regulation.

If the internal voltage generator is used then $V_{LCDSENSE}$ must be connected to V_{LCDOUT}. If a external supply voltage is used then the $V_{LCDSENSE}$ can be let open-circuit or connected to ground.

7.1.8 T1 TO T5: TEST PADS

T1, T3, T4 and T5 must be connected to V_{SS}, T2 must be left open-circuit. Not accessible to user.

7.1.9 SDIN: SERIAL DATA LINE

Serial data input line.

7.1.10 SCLK: SERIAL CLOCK LINE

Input for the clock signal 0 to 4.0 Mbits/s.

7.1.11 D/$\overline{C}$: MODE SELECT

Input to select either $\overline{\text{command}}$/address or data input.

7.1.12 $\overline{SCE}$: CHIP ENABLE

The enable pin allows data to be clocked in; the signal is active LOW.

7.1.13 OSC: OSCILLATOR

When the on-chip oscillator is used this input must be connected to V_{DD}. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to V_{SS} the display is not clocked and may be left in a DC state. To avoid this the chip should always be put into Power-down mode before stopping the clock.

7.1.14 $\overline{RES}$: RESET

This signal will reset the device and must be applied to properly initialize the chip; the signal is active LOW.

8 FUNCTIONAL DESCRIPTION

8.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD}. An external clock signal, if used, is connected to this input.

8.2 Address Counter (AC)

The address counter assigns addresses to the display data RAM for writing. The X address X6 to X0 and the Y address Y3 to Y0 are set separately. After a write operation the address counter is automatically incremented by 1 according to the V flag (see Chapter 9).

8.3 Display Data RAM (DDRAM)

The PCF8812 contains a 65 × 102 bit static RAM which stores the display data. The RAM is divided into 8 banks of 102 bytes (8 × 8 × 102 bits) and one bank of 102 bits (1 × 102 bits). During RAM access, data is transferred to the RAM via the serial interface. There is a direct correspondence between the X address and the column output number.

8.4 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data buses.

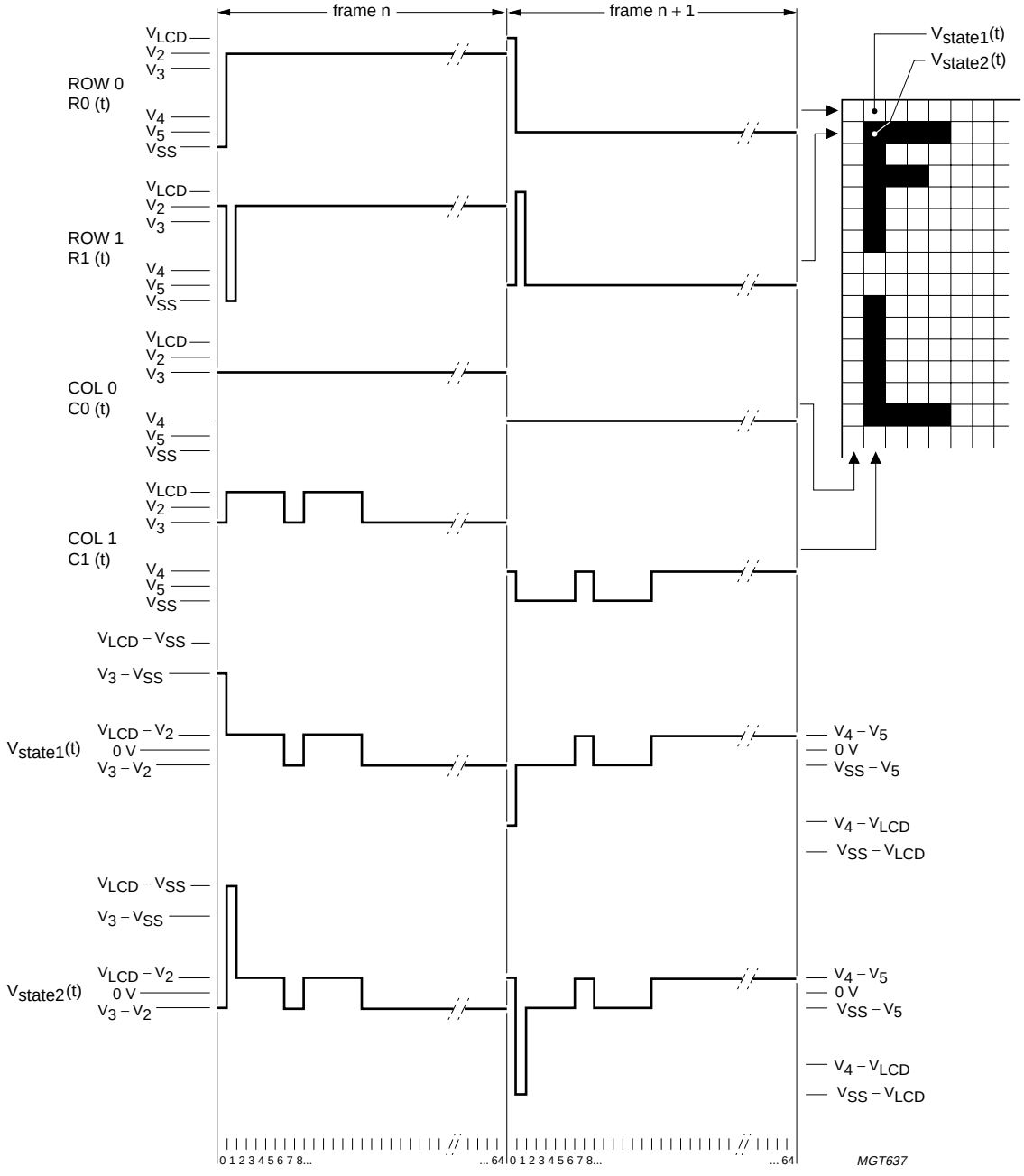
8.5 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs.

The display status (all dots on/off and normal/inverse video) is set by bits E and D in the command ‘display control’ (see Table 2).

8.6 LCD row and column drivers

The PCF8812 contains 65 row and 102 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.



(1) $V_{state1}(t) = C1(t) - R0(t)$.
(2) $V_{state2}(t) = C1(t) - R1(t)$.

Fig.2 Typical LCD driver waveforms.

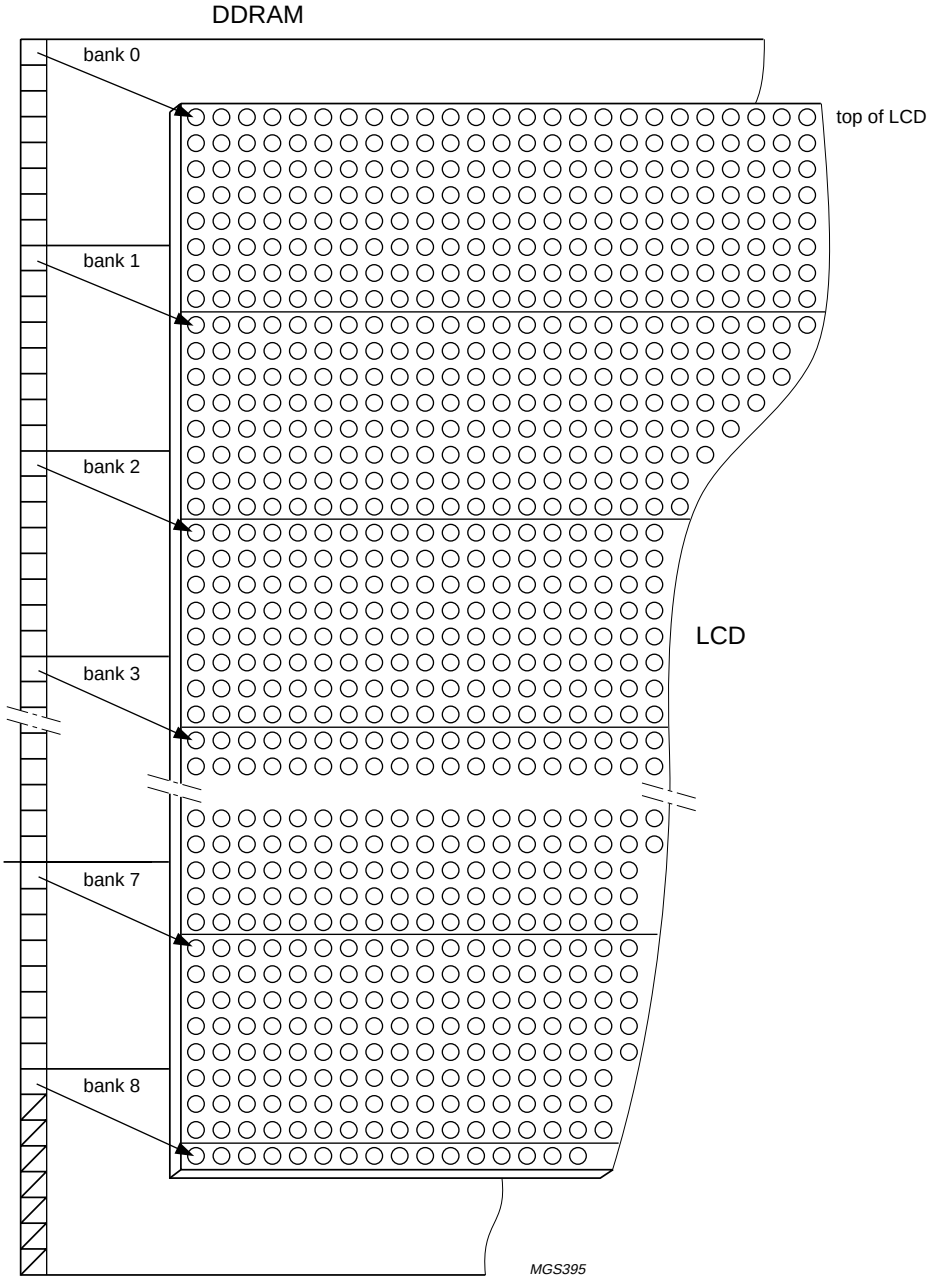


Fig.3 DDRAM to display mapping.

9 ADDRESSING

Data is downloaded in bytes into the RAM matrix of the PCF8812 as indicated in Figs.3, 4, 5 and 6. The display RAM has a matrix of 65 × 102 bits. The columns are addressed by the address pointer. The address ranges are: X0 to X101 (1100101) and Y0 to Y8 (1000). Addresses outside of these ranges are not allowed. In vertical addressing mode (V = 1) the Y address increments after each byte (see Fig.6). After the last Y address (Y = 8) Y wraps around to 0 and X increments to address the next column. In horizontal addressing mode (V = 0) the X address increments after each byte (see Fig.5). After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row. After the very last address (X = 101 and Y = 8) the address pointers wrap around to address (X = 0 and Y = 0).

9.1 Data structure

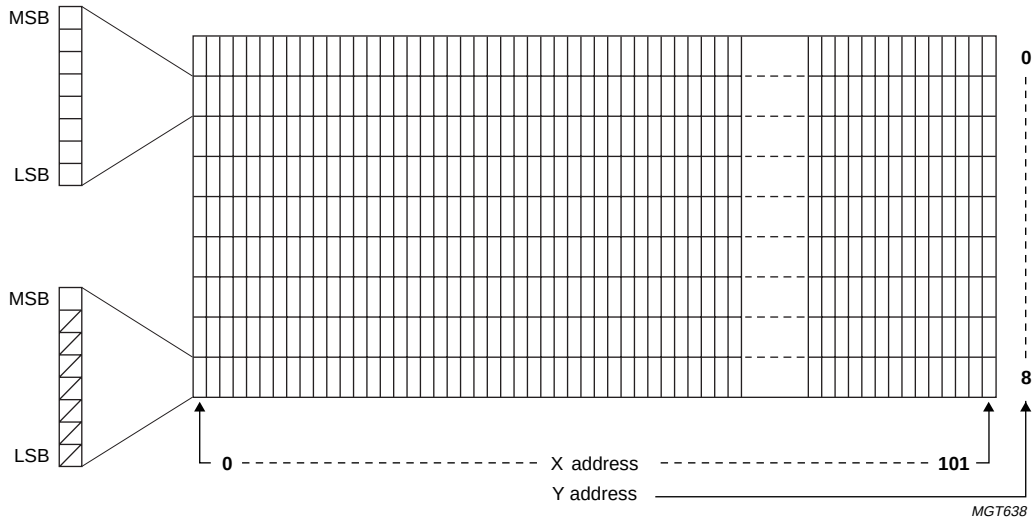


Fig.4 RAM format addressing.

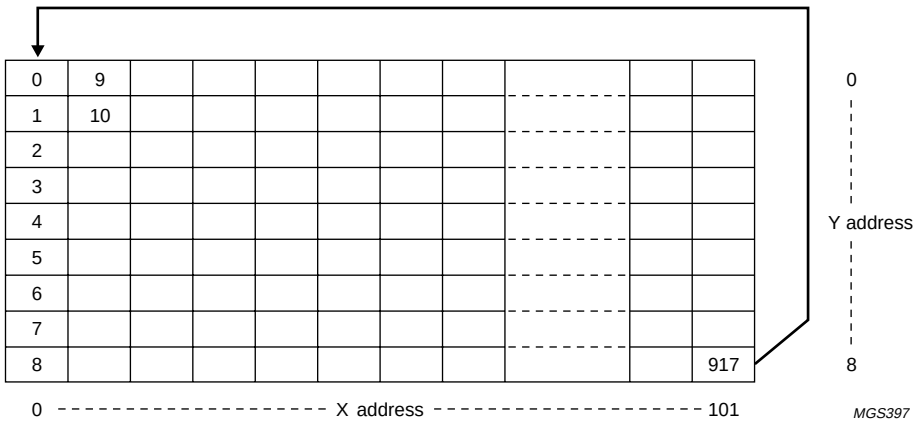


Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

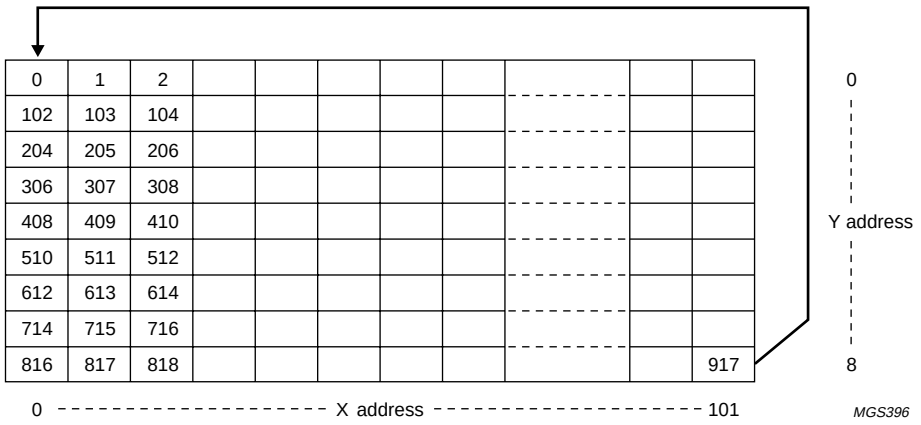


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

10 INSTRUCTIONS

The instruction format is divided into two modes: If D/$\overline{C}$ (mode select) is set LOW the current byte is interpreted as command byte (see Table 1). Figure 8 shows an example of a serial data stream for initializing the chip. If D/$\overline{C}$ is set HIGH the following bytes are stored in the display data RAM. After every data byte the address counter is incremented automatically. The level of the D/$\overline{C}$ signal is read during the last bit of the data byte. Every instruction can be sent in any order to the PCF8812. The MSB of a byte is transmitted first. Figure 8 shows one possible command stream, used to set-up the LCD driver. The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state SCLK clock pulses have no effect and no power is consumed by the serial interface. A negative edge on $\overline{SCE}$ enables the serial interface and indicates the start of a data transmission.

Figures 9 and 10 show the serial bus protocol:

- When $\overline{SCE}$ is HIGH, SCLK clocks are ignored. During the HIGH time of $\overline{SCE}$ the serial interface is initialized (see Fig.12)
- SDIN is sampled at the positive edge of SCLK
- D/$\overline{C}$ indicates whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1). It is read with the eighth SCLK pulse
- If $\overline{SCE}$ stays LOW after the last bit of a $\overline{command}$/data byte, the serial interface expects DB7 of the next byte at the next positive edge of SCLK (see Fig.12). If SCLK goes LOW after the last data bit (DB0), either:
  - A rising clock edge is required to latch the last data bit
  - Or the last bit is latched when SCE goes HIGH.
- A reset pulse with $\overline{RES}$ interrupts the transmission. No data is written into the RAM. The registers are cleared. If $\overline{SCE}$ is LOW after the positive edge of $\overline{RES}$, the serial interface is ready to receive bit 7 of a $\overline{command}$/data byte (see Fig.12).

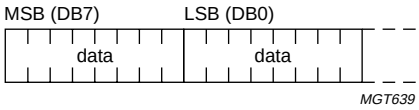


Fig.7 General format of data stream.

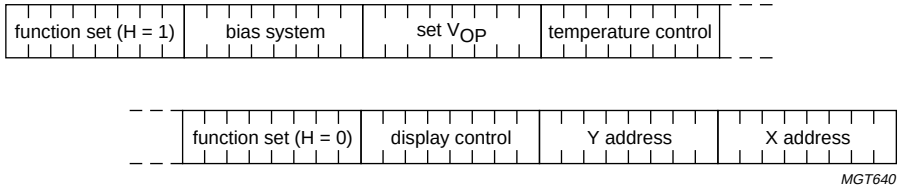


Fig.8 Example of serial data stream.

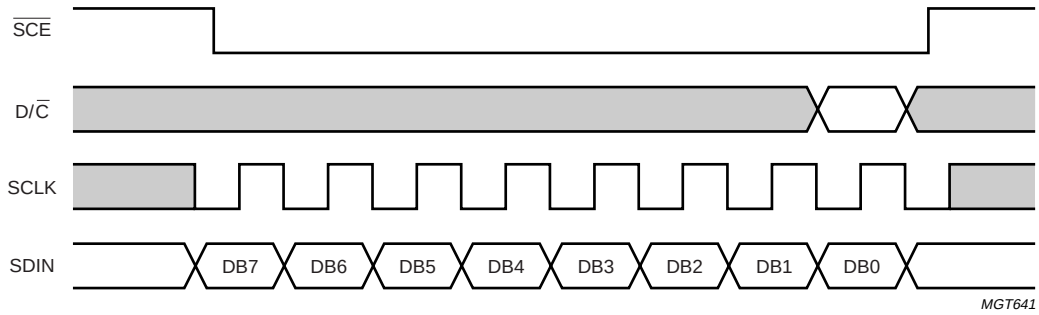


Fig.9 Serial bus protocol transmission of one byte.

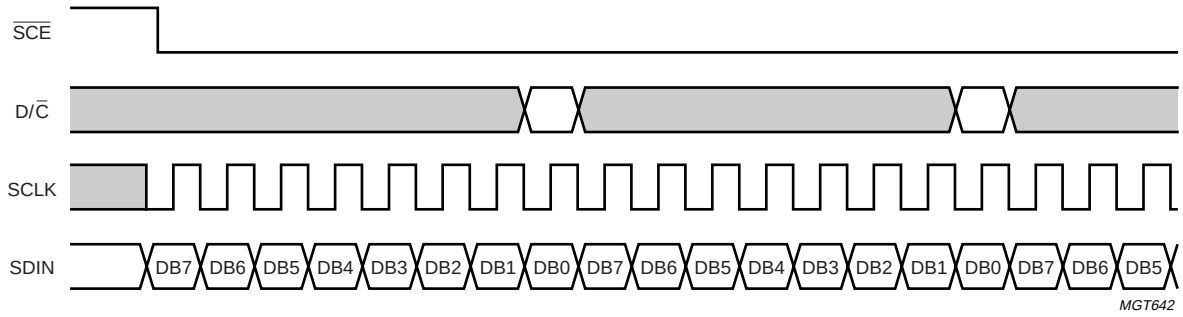


Fig.10 Serial bus protocol transmission of several bytes.

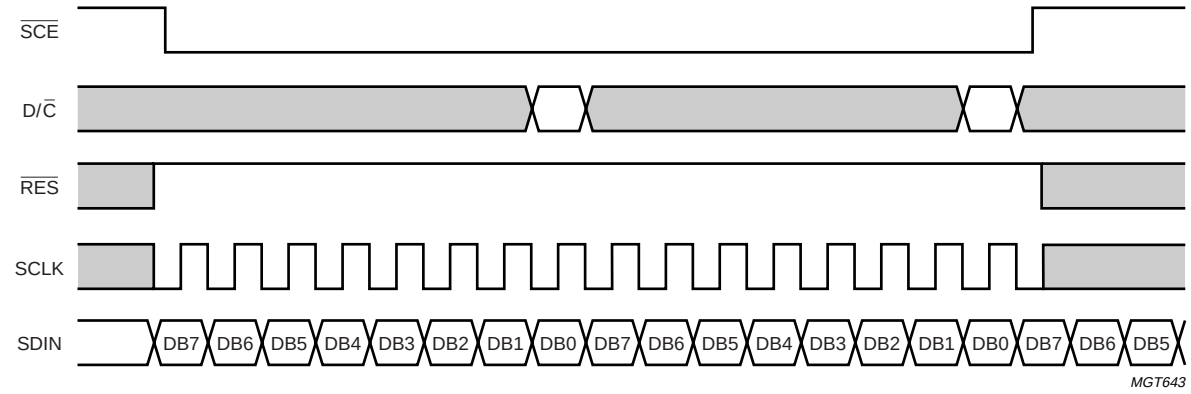


Fig.11 Serial bus reset function ($\overline{SCE}$).

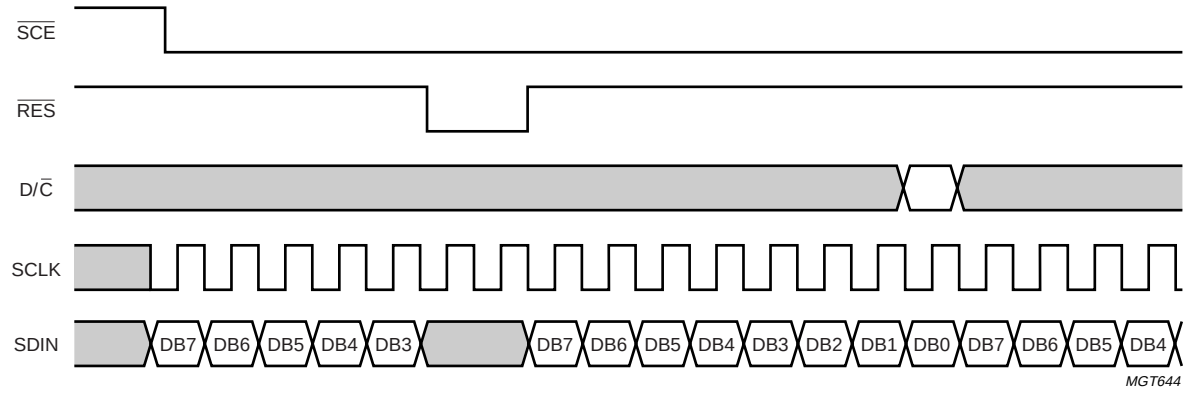


Fig.12 Serial bus reset function ($\overline{RES}$).

Table 1 Instruction set

INSTRUCTION	D/C	COMMAND BYTE								DESCRIPTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
(H = 0 or 1)										
NOP	0	0	0	0	0	0	0	0	0	no operation
Function set	0	0	0	1	0	0	PD	V	H	power-down control; entry mode; extended instruction set control (H)
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to display RAM
(H = 0)										
Reserved	0	0	0	0	0	0	1	X	X	do not use
Display control	0	0	0	0	0	1	D	0	E	sets display configuration
Set higher or lower programming range V_{op}	0	0	0	0	1	0	0	0	PRS	V_{LCD} programming range select
Set Y address of RAM	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	sets Y address of RAM; $0 \leq Y \leq 8$
Set X address of RAM	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X address part of RAM; $0 \leq X \leq 101$
(H = 1)										
Reserved	0	0	0	0	0	0	0	0	1	do not use
Reserved	0	0	0	0	0	0	0	1	X	do not use
Temperature control	0	0	0	0	0	0	1	TC_1	TC_0	set temperature coefficient (TCx)
HV-gen stages	0	0	0	0	0	1	0	S_1	S_0	# of HV-gen voltage multiplication
Bias system	0	0	0	0	1	0	BS_2	BS_1	BS_0	set bias system (BSx)
Reserved	0	0	1	X	X	X	X	X	X	do not use (reserved for test)
Set V_{op}	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations for symbols in Table 1

BIT		0	1	RESET STATE
PD		chip is active	chip is in Power-down mode	1
V		horizontal addressing	vertical addressing	0
H		use basic instruction set	use extended instruction set	0
PRS		V_{LCD} programming range; LOW	V_{LCD} programming range; HIGH	0
D, E	00	display blank		D = 0
	10	normal mode		
	01	all display segments on		E = 0
	11	inverse video mode		
TC1 to TC0	00	V_{LCD} temperature coefficient 0		TC1 to TC0 = 00
	01	V_{LCD} temperature coefficient 1		
	10	V_{LCD} temperature coefficient 2		
	11	V_{LCD} temperature coefficient 3		
S1 to S0	00	2 × voltage multiplier		S1 to S0 = 00
	01	3 × voltage multiplier		
	10	4 × voltage multiplier		
	11	5 × voltage multiplier		
V_{OP} 6 to V_{OP}0		V_{LCD} programming		V_{OP} 6 to V_{OP}0 = 0000000
BS2 to BS0		bias system		BS2 to BS0 = 000

10.1 Initialization

Immediately following power-on, all internal registers as well as the RAM content are undefined; a reset pulse must be applied.

Reset is accomplished by applying an external reset pulse (active LOW) at the pad $\overline{RES}$. When reset occurs within the specified time, all internal registers are reset, however the RAM is still undefined. The state after reset is described in Section 10.2.

The $\overline{RES}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches $V_{DD(min)}$ (or higher) within a maximal time t_{VHRL} after V_{DD} going HIGH (see Fig.16).

10.2 Reset function

After reset the LCD driver has the following state:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Display blank (E = D = 0)
- Address counter X6 to X0 = 0; Y3 to Y0 = 0
- Temperature control mode (TC1 to TC0 = 0)
- Bias system (BS2 to BS0 = 0)
- V_{LCD} is equal to 0; the HV-generator is switched off (V_{OP}6 to V_{OP}0 = 0 and PRS = 0)
- After power-on; RAM data is undefined; the reset signal doesn't change the content of the RAM
- All LCD outputs at V_{SS} (display off).

10.3 Function set

10.3.1 PD

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off; V_{LCD} can be disconnected
- Oscillator off (external clock possible)
- Serial bus; command; etc. function
- RAM contents not cleared; RAM data can be written
- V_{LCD} discharged to V_{SS} in Power-down mode.

10.3.2 V

When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig.5. When V = 1, the vertical addressing is selected. The data is written into the DDRAM as shown in Fig.6.

10.3.3 H

When H = 0 the commands ‘display control’, ‘set Y address’, ‘set X address’ and set the PRS bit (low or high range of the high voltage generator) can be performed, when H = 1 the others can be executed. The commands ‘write data’ and ‘function set’ can be executed in both cases.

10.4 Display control

10.4.1 D AND E

The bits D and E select the display mode (see Table 2).

10.5 Set Y address of RAM

Y3 to Y0 defines the Y address vector address of the display RAM (see Table 3).

Table 3 X/Y address range: note 1

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X RANGE
0	0	0	0	bank 0 (display RAM)	0 to 101
0	0	0	1	bank 1 (display RAM)	0 to 101
0	0	1	0	bank 2 (display RAM)	0 to 101
0	0	1	1	bank 3 (display RAM)	0 to 101
0	1	0	0	bank 4 (display RAM)	0 to 101
0	1	0	1	bank 5 (display RAM)	0 to 101
0	1	1	0	bank 6 (display RAM)	0 to 101
0	1	1	1	bank 7 (display RAM)	0 to 101
1	0	0	0	bank 8 (display RAM)	0 to 101

Note

1. In bank 8 only the LSB is accessed.

10.6 Set X address of RAM

The X address points to the columns. The range of X is 0 to 101 (65H).

10.7 Set HV-generator stages

The PCF8812 incorporates a software configurable voltage multiplier. After reset ($\overline{RES}$) the voltage multiplier is set to $2 \times V_{DD2}$. Other voltage multiplier factors are set via the command ‘Set HV-gen stages’ (see Tables 1 and 2).

10.8 Bias system

The bias voltage levels are set in the ratio of R - R - nR - R - R giving a $\frac{1}{(n+4)}$ bias system. Different multiplex rates require different factors 'n' (see Table 4). This is programmed by BS2 to BS0. For MUX1 to MUX65 the optimum bias value 'n' is given by: $n = \sqrt{65} - 3 = 5.062 = 5$ resulting in $^1/_9$ bias.

Table 4 Programming the required bias system

BS2	BS1	BS0	n	RECOMMEND MUX RATE
0	0	0	7	1 to 100
0	0	1	6	1 to 80
0	1	0	5	1 to 65 or 1 to 65
0	1	1	4	1 to 48
1	0	0	3	1 to 40 or 1 to 34
1	0	1	2	1 to 24
1	1	0	1	1 to 18 or 1 to 16
1	1	1	0	1 to 10 or 1 to 9 or 1 to 8

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES	BIAS VOLTAGES FOR n = 5 ($^1/_9$ BIAS)
V1	V_{LCD}	V_{LCD}
V2	$\frac{(n+3)}{(n+4)}$	$^8/_9 \times V_{LCD}$
V3	$\frac{(n+2)}{(n+4)}$	$^7/_9 \times V_{LCD}$
V4	$\frac{2}{(n+4)}$	$^2/_9 \times V_{LCD}$
V5	$\frac{1}{(n+4)}$	$^1/_9 \times V_{LCD}$
V6	V_{SS}	V_{SS}

10.9 Temperature control

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimum contrast. There are 4 different temperature coefficients available in the PCF8812 (see Fig.13). The coefficients are selected by bits TC1 to TC0. Table 6 shows the typical values of the different temperature coefficients. The coefficients are proportional to the programmed V_{LCD}.

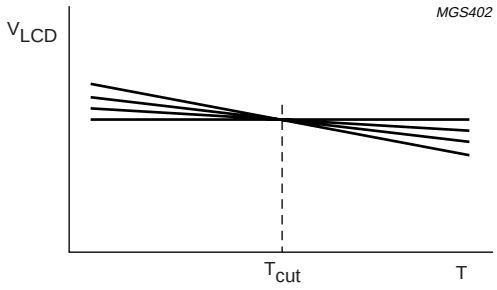


Fig.13 Temperature coefficients.

10.10 Set V_{OP} value

The operating voltage V_{LCD} can be set by software. The generated voltage is dependent on temperature, programmed Temperature Coefficient (TC) and the programmed voltage at reference temperature (T_{cut}).

$$V_{LCD(T)} = (a + V_{OP} \times b)(1 + (T - T_{cut}) \times TC) \quad (1)$$

The voltage at reference temperature [$V_{LCD}(T = T_{cut})$] can be calculated as follows:

$$V_{LCD(T = T_{cut})} = (a + V_{OP} \times b) \quad (2)$$

The parameters are explained in Table 6. The maximum voltage that can be generated is dependent on the V_{DD2} voltage and the display load current. Two overlapping V_{LCD} ranges are selectable via the command 'HV-gen control'. For the LOW (PRS = 0) range a = a_1 and for the HIGH (PRS = 1) range a = a_2 with steps equal to 'b' in both ranges. It should be noted that the charge pump is turned off if V_{OP} 6 to 0 and the bit PRS are all set to zero (see Fig.14).

For MUX 1 to 65 the optimum operating voltage of the liquid can be calculated as follows;

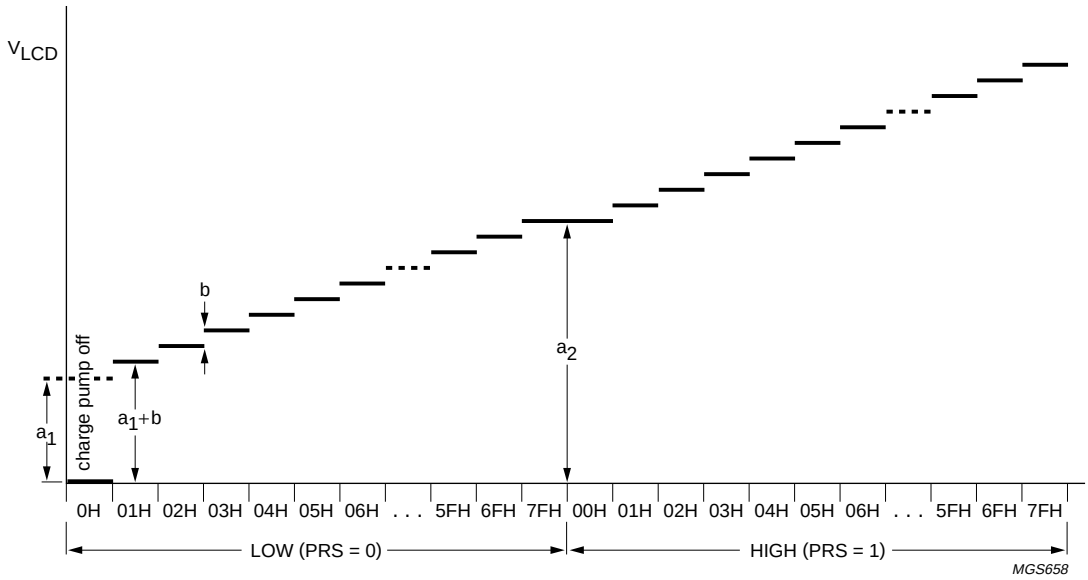
$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2} \times \left(1 - \frac{1}{\sqrt{65}}\right)} \times V_{th} = 6.85 \times V_{th} \quad (3)$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Table 6 Typical values for parameters for the HV-generator programming

SYMBOL	VALUE	UNIT
a1	2.94 (PRS = 0)	V
a2	6.75 (PRS = 1)	V
b	0.03	V
T_{cut}	27	°C

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9 V) the user has to ensure, while setting the V_{OP} register and selecting the Temperature Compensation (TC), that under all conditions and including all tolerances that V_{LCD} remains below 9 V.



V_{OP} 6 to 0 (programmed) [00H to 7FH; programming range LOW and HIGH].

Fig.14 V_{OP} programming of PCF8812 (at T = T_{cut}).

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); see notes 1 and 2

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD1}	supply voltage		–0.5	+6.5	V
V_{DD2}, V_{DD3}	supply voltage for internal voltage generator		–0.5	+4.5	V
V_{LCD}	supply voltage range LCD		–0.5	+9.0	V
V_i	all input voltages		–0.5	V_{DD} + 0.5	V
I_{SS}	ground supply current		–50	+50	mA
I_i, I_o	DC input or output current		–10	+10	mA
P_{tot}	total power dissipation		–	300	mW
P_O	power dissipation per output		–	30	mW
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling voltage	note 3	–	±1900	V
		note 4	–	±200	V

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are referenced to V_{SS} unless otherwise specified.
3. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
4. Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH series inductor.

12 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS devices”*).

13 DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage		+2.5	–	+5.5	V
V_{DD2},V_{DD3}	supply voltage for internal voltage generator	LCD voltage internally generated (voltage generator enabled)	+2.5	–	+4.5	V
V_{LCDIN}	LCD input supply voltage	LCD voltage externally supplied (voltage generator disabled)	+4.5	–	+9.0	V
V_{LCDOUT}	LCD output supply voltage	LCD voltage internally generated (voltage generator enabled); note 1	+4.5	–	+9.0	V
$I_{DD(tot)}$	total supply current	normal mode; V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{SCLK} = 0; T_{amb} = 25 °C; no display load; 4 × charge pump; notes 2 and 3	–	220	350	µA
		Power-down mode; with internal or external V_{LCD} supply voltage; note 4	–	1.5	–	µA
I_{LCDIN}	supply current from external V_{LCD}	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{SCLK} = 0; T = 25 °C; no display load; notes 2, 3 and 5	–	30	–	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	V_I = V_{DD1} or V_{SS1}	–1	–	+1	µA
Column and row outputs						
R_{col}	column output resistance COL 0 to COL 101	I_L = 10 µA outputs tested one at a time	–	12	20	kΩ
R_{row}	row output resistance ROW 0 to ROW 64	I_L = 10 µA outputs tested one at a time	–	12	20	kΩ
$V_{bias(col)}$	column bias tolerance COL 0 to COL 101		–100	0	+100	mV
$V_{bias(row)}$	row bias tolerance ROW 0 to ROW 64		–100	0	+100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LCD supply voltage generator						
V_{LCD}	V_{LCD} tolerance internally generated	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{SCLK} = 0; T_{amb} = 25 °C; display-load = 10 μA; notes 3, 6 and 7	–300	0	+300	mV
TC	V_{LCD} temperature coefficient	V_{DD1} = 2.8 V; f_{SCLK} = 0; T_{amb} = –20 to +70 °C; display load = 10 μA; note 3				
		coefficient 0	–	0×10^{-3}	–	1/°C
		coefficient 1	–	-0.76×10^{-3}	–	1/°C
		coefficient 2	–	-1.05×10^{-3}	–	1/°C
		coefficient 3	–	-2.10×10^{-3}	–	1/°C

Notes

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. f_{SCLK} = 0 means no serial clock.
4. During power-down all static currents are switched off.
5. If external V_{LCD}; the display load current is not transmitted to I_{DD}.
6. Tolerance depend on the temperature; (typical null at T_{amb} = 27 °C, maximum tolerance values are measured at the temperate range limit, maximum tolerance is proportional to V_{LCD}).
7. For TC1 to TC3.

14 AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency	V_{DD1} = 2.8 V; T_{amb} = –20 to +70 °C	22	38	67	kHz
$f_{clk(ext)}$	external clock frequency		20	38	67	kHz
f_{frame}	frame frequency	f_{OSC} or $f_{clk(ext)}$ = 38 kHz; note 1	–	73	–	Hz
t_{VHRL}	V_{DD} to $\overline{RES}$ LOW	see Fig.16	0	–	1	μs
t_{RW}	$\overline{RES}$ LOW pulse width	see Fig.16	500	–	–	ns
Serial bus timing characteristics						
f_{SCLK}	clock frequency	V_{DD1} = 3.0 V ±10%; all signal timing is based on 20% to 80% of V_{DD} and a maximum rise and fall time of 10 ns	0	–	4.00	MHz
t_{cyc}	clock cycle time		250	–	–	ns
t_{PWH1}	SCLK pulse width HIGH		100	–	–	ns
t_{PWL1}	SCLK pulse width LOW		100	–	–	ns
t_{S2}	$\overline{SCE}$ set-up time		60	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{H2}	$\overline{SCE}$ hold time		100	–	–	ns
t_{PWH2}	$\overline{SCE}$ minimum HIGH time		100	–	–	ns
t_{H5}	$\overline{SCE}$ start hold time	note 2	100	–	–	ns
t_{S3}	D/$\overline{C}$ set-up time		100	–	–	ns
t_{H3}	D/$\overline{C}$ hold time		100	–	–	ns
t_{S4}	SDIN set-up time		100	–	–	ns
t_{H4}	SDIN hold time		100	–	–	ns

Notes

1. $f_{frame} = \frac{f_{clk(ext)}}{520}$
2. t_{H5} is the time from the previous SCLK positive edge (irrespective of the state of $\overline{SCE}$) to the negative edge of $\overline{SCE}$ (see Fig.15).

15 SERIAL INTERFACE

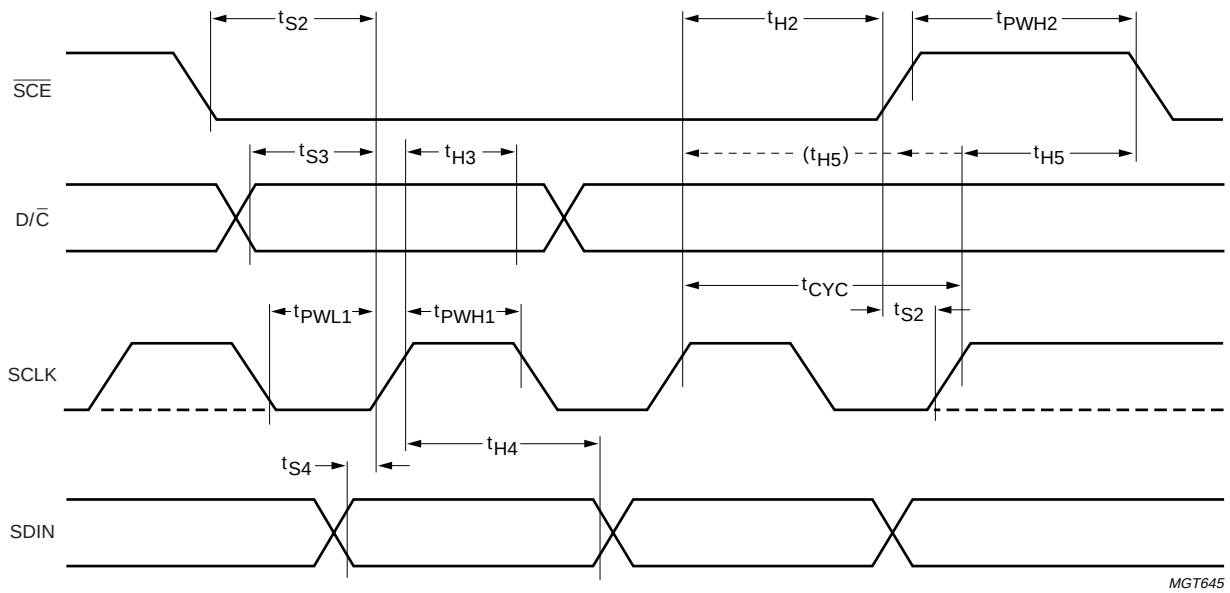


Fig.15 Serial interface timing.

16 RESET

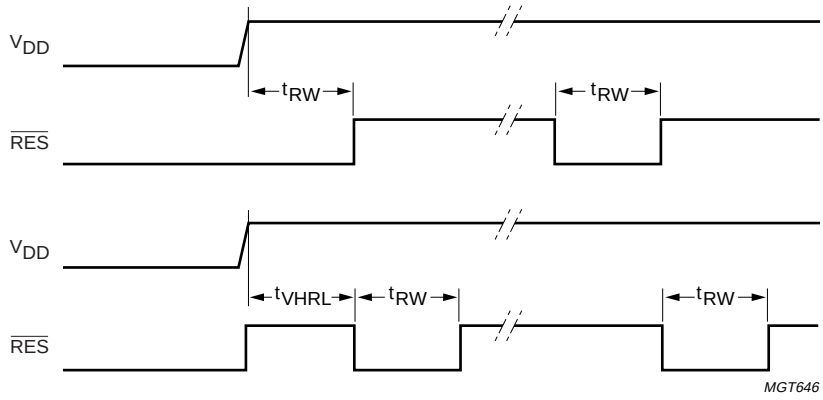
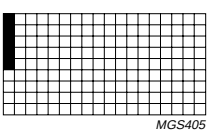
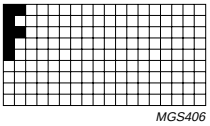
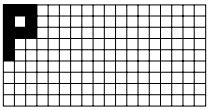
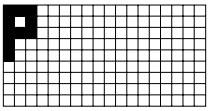
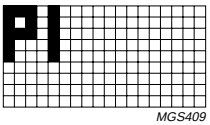
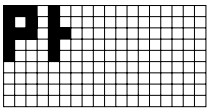
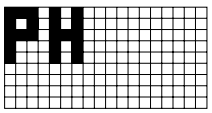


Fig.16 Reset timing.

17 APPLICATION INFORMATION

Table 7 Programming example for PCF8812

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	start										$\overline{SCE}$ is going low
2	0	0	0	1	0	0	0	0	1		function set; PD = 0, V = 0; select extended instruction set (H = 1 mode)
3	0	0	0	0	1	0	0	0	1		set charge pump range HIGH PRS = 1
4	0	1	0	0	1	1	1	0	0		set V_{OP}; V_{OP} is set to 7.6 V
5	0	0	0	1	0	0	0	0	0		function set; PD = 0; V = 0; select normal instruction set (H = 0 mode)
6	0	0	0	0	0	1	1	0	0		display control; set normal mode (D = 1; E = 0).
7	1	1	1	1	1	1	0	0	0	 MGS405	data write; Y and X are initialized to 0 by default, so they aren't set here

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
8	1	1	0	1	0	0	0	0	0	 MGS406	data write
9	1	1	1	1	0	0	0	0	0	 MGS407	data write
10	1	0	0	0	0	0	0	0	0	 MGS407	data write
11	1	1	1	1	1	1	0	0	0	 MGS409	data write
12	1	0	0	1	0	0	0	0	0	 MGS410	data write
13	1	1	1	1	1	1	0	0	0	 MGS411	data write

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
14	0	0	0	0	0	1	1	0	1	 MGS412	display control; set inverse video mode (D = 1; E = 1)
15	0	1	0	0	0	0	0	0	0	 MGS412	set X-address of RAM; set address to 0000000
16	1	0	0	0	0	0	0	0	0	 MGS414	data write

The pinning of the PCF8812 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 65 × 102 pixels.

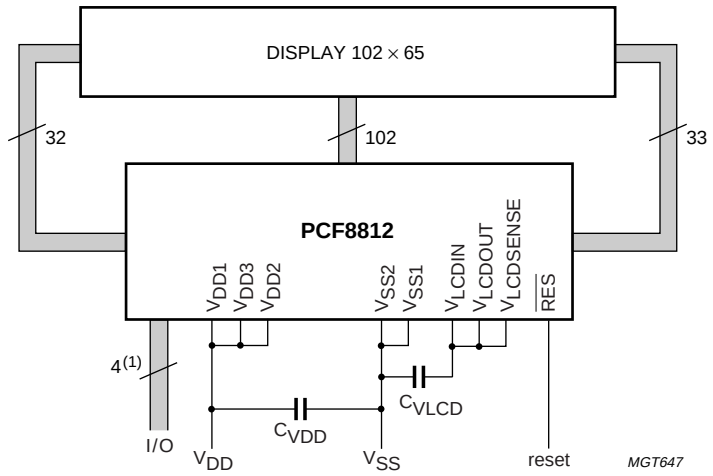


Fig.17 Application diagram; internal charge pump is used and a single V_{DD}.

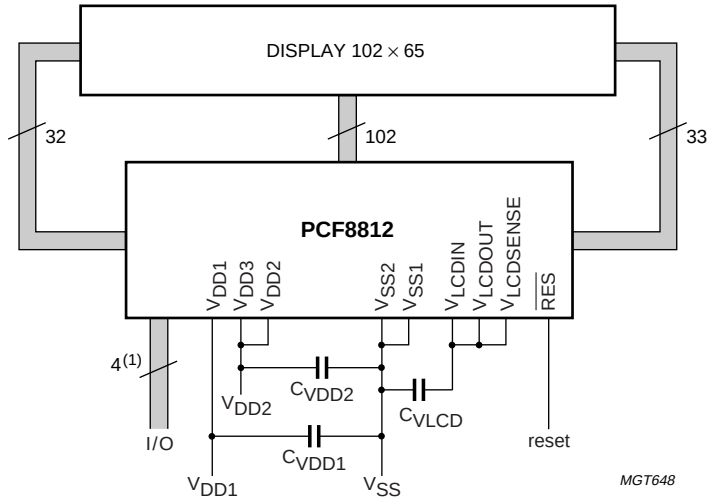


Fig.18 Application diagram; internal charge pump is used and two separate V_{DD} (V_{DD1} and V_{DD2}).

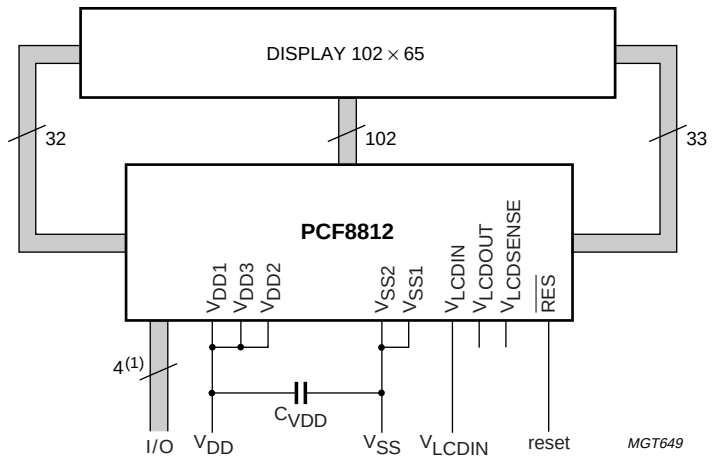


Fig.19 Application diagram; external high voltage generation is used.

The required minimum value for the external capacitors in an application with the PCF8812 are as follows:

C_{VLCD} = 100 nF (minimum)

C_{VDD}; C_{VDD1}; C_{VDD2} = 1 µF (minimum).

Higher capacitor values are recommended for ripple reduction.

18 CHIP INFORMATION

The PCF8812 is manufactured in n-well CMOS technology. The substrate is at V_{SS} potential.

19 PAD INFORMATION

Table 8 Bonding pad dimensions

NAME	DIMENSION
Pad pitch	70 µm
Pad size; aluminium	62 × 100 µm
Bump dimensions	50 × 90 × 17.5 µm (±5)
Wafer thickness; including bumps	maximum 430 µm
Wafer thickness; without bumps	381 µm typ.

20 BONDING PAD LOCATION

Table 9 Bonding pad location

All x and y coordinates are referenced to the centre of the chip (dimensions in μm; see Fig.20).

SYMBOL	PAD	COORDINATES	
		x	y
$\overline{RES}$	1	+3870	+934.6
ROW 32	2	+4270	+934.6
ROW 31	3	+4340	+934.6
ROW 30	4	+4410	+934.6
ROW 29	5	+4480	+934.6
ROW 28	6	+4550	+934.6
ROW 27	7	+4620	+934.6
ROW 26	8	+4690	+934.6
ROW 25	9	+4760	+934.6
ROW 24	10	+4830	+934.6
ROW 23	11	+4900	+934.6
ROW 22	12	+4970	+934.6
ROW 21	13	+5040	+934.6
ROW 20	14	+5110	+934.6
ROW 19	15	+5180	+934.6
dummy pad	16	+5320	+934.6
dummy pad	17	+5355	−934.6
ROW 0	18	+5005	−934.6
ROW 1	19	+4935	−934.6
ROW 2	20	+4865	−934.6
ROW 3	21	+4795	−934.6
ROW 4	22	+4725	−934.6
ROW 5	23	+4655	−934.6
ROW 6	24	+4585	−934.6
ROW 7	25	+4515	−934.6
ROW 8	26	+4445	−934.6
ROW 9	27	+4375	−934.6
ROW 10	28	+4305	−934.6
ROW 11	29	+4235	−934.6
ROW 12	30	+4165	−934.6
ROW 13	31	+4095	−934.6
ROW 14	32	+4025	−934.6
ROW 15	33	+3955	−934.6
ROW 16	34	+3885	−934.6
ROW 17	35	+3815	−934.6
ROW 18	36	+3745	−934.6
COL 0	37	+3605	−934.6
COL 1	38	+3535	−934.6
COL 2	39	+3465	−934.6
COL 3	40	+3395	−934.6
COL 4	41	+3325	−934.6
COL 5	42	+3255	−934.6
COL 6	43	+3185	−934.6
COL 7	44	+3115	−934.6
COL 8	45	+3045	−934.6
COL 9	46	+2975	−934.6
COL 10	47	+2905	−934.6
COL 11	48	+2835	−934.6
COL 12	49	+2765	−934.6
COL 13	50	+2695	−934.6
COL 14	51	+2625	−934.6
COL 15	52	+2555	−934.6
COL 16	53	+2485	−934.6
COL 17	54	+2415	−934.6
COL 18	55	+2345	−934.6
COL 19	56	+2275	−934.6
COL 20	57	+2205	−934.6
COL 21	58	+2135	−934.6
COL 22	59	+2065	−934.6
COL 23	60	+1995	−934.6
COL 24	61	+1925	−934.6
COL 25	62	+1785	−934.6
COL 26	63	+1715	−934.6
COL 27	64	+1645	−934.6
COL 28	65	+1575	−934.6
COL 29	66	+1505	−934.6
COL 30	67	+1435	−934.6
COL 31	68	+1365	−934.6
COL 32	69	+1295	−934.6
COL 33	70	+1225	−934.6
COL 34	71	+1155	−934.6
COL 35	72	+1085	−934.6
COL 36	73	+1015	−934.6
COL 37	74	+945	−934.6
COL 38	75	+875	−934.6

SYMBOL	PAD	COORDINATES	
		x	y
COL 39	76	+805	–934.6
COL 40	77	+735	–934.6
COL 41	78	+665	–934.6
COL 42	79	+595	–934.6
COL 43	80	+525	–934.6
COL 44	81	+455	–934.6
COL 45	82	+385	–934.6
COL 46	83	+315	–934.6
COL 47	84	+245	–934.6
COL 48	85	+175	–934.6
COL 49	86	+105	–934.6
COL 50	87	–35	–934.6
COL 51	88	–105	–934.6
COL 52	89	–175	–934.6
COL 53	90	–245	–934.6
COL 54	91	–315	–934.6
COL 55	92	–385	–934.6
COL 56	93	–455	–934.6
COL 57	94	–525	–934.6
COL 58	95	–595	–934.6
COL 59	96	–665	–934.6
COL 60	97	–735	–934.6
COL 61	98	–805	–934.6
COL 62	99	–875	–934.6
COL 63	100	–945	–934.6
COL 64	101	–1015	–934.6
COL 65	102	–1085	–934.6
COL 66	103	–1155	–934.6
COL 67	104	–1225	–934.6
COL 68	105	–1295	–934.6
COL 69	106	–1365	–934.6
COL 70	107	–1435	–934.6
COL 71	108	–1505	–934.6
COL 72	109	–1575	–934.6
COL 73	110	–1645	–934.6
COL 74	111	–1715	–934.6
COL 75	112	–1785	–934.6
COL 76	113	–1925	–934.6
COL 77	114	–1995	–934.6

SYMBOL	PAD	COORDINATES	
		x	y
COL 78	115	–2065	–934.6
COL 79	116	–2135	–934.6
COL 80	117	–2205	–934.6
COL 81	118	–2275	–934.6
COL 82	119	–2345	–934.6
COL 83	120	–2415	–934.6
COL 84	121	–2485	–934.6
COL 85	122	–2555	–934.6
COL 86	123	–2625	–934.6
COL 87	124	–2695	–934.6
COL 88	125	–2765	–934.6
COL 89	126	–2835	–934.6
COL 90	127	–2905	–934.6
COL 91	128	–2975	–934.6
COL 92	129	–3045	–934.6
COL 93	130	–3115	–934.6
COL 94	131	–3185	–934.6
COL 95	132	–3255	–934.6
COL 96	133	–3325	–934.6
COL 97	134	–3395	–934.6
COL 98	135	–3465	–934.6
COL 99	136	–3535	–934.6
COL 100	137	–3605	–934.6
COL 101	138	–3675	–934.6
ROW 50	139	–3815	–934.6
ROW 49	140	–3885	–934.6
ROW 48	141	–3955	–934.6
ROW 47	142	–4025	–934.6
ROW 46	143	–4095	–934.6
ROW 45	144	–4165	–934.6
ROW 44	145	–4235	–934.6
ROW 43	146	–4305	–934.6
ROW 42	147	–4375	–934.6
ROW 41	148	–4445	–934.6
ROW 40	149	–4515	–934.6
ROW 39	150	–4585	–934.6
ROW 38	151	–4655	–934.6
ROW 37	152	–4725	–934.6
ROW 36	153	–4795	–934.6

SYMBOL	PAD	COORDINATES	
		x	y
ROW 35	154	−4865	−934.6
ROW 34	155	−4935	−934.6
ROW 33	156	−5005	−934.6
dummy pad	157	−5355	−934.6
dummy pad	158	−5320	+934.6
ROW 51	159	−5180	+934.6
ROW 52	160	−5110	+934.6
ROW 53	161	−5040	+934.6
ROW 54	162	−4970	+934.6
ROW 55	163	−4900	+934.6
ROW 56	164	−4830	+934.6
ROW 57	165	−4760	+934.6
ROW 58	166	−4690	+934.6
ROW 59	167	−4620	+934.6
ROW 60	168	−4550	+934.6
ROW 61	169	−4480	+934.6
ROW 62	170	−4410	+934.6
ROW 63	171	−4340	+934.6
ROW 64	172	−4270	+934.6
dummy pad	173	−4050	+934.6
V_{DD1}	174	−3890	+934.6
V_{DD1}	175	−3810	+934.6
V_{DD1}	176	−3730	+934.6
V_{DD1}	177	−3650	+934.6
V_{DD1}	178	−3570	+934.6
V_{DD1}	179	−3490	+934.6
V_{DD3}	180	−3250	+934.6
V_{DD2}	181	−3090	+934.6
V_{DD2}	182	−3010	+934.6
V_{DD2}	183	−2930	+934.6
V_{DD2}	184	−2850	+934.6
V_{DD2}	185	−2770	+934.6
V_{DD2}	186	−2690	+934.6
V_{DD2}	187	−2610	+934.6
V_{DD2}	188	−2530	+934.6
V_{DD2}	189	−2450	+934.6
V_{DD2}	190	−2370	+934.6
V_{DD2}	191	−2290	+934.6
V_{DD2}	192	−2210	+934.6

SYMBOL	PAD	COORDINATES	
		x	y
V_{DD2}	193	−2130	+934.6
OSC	194	−1890	+934.6
SDIN	195	−1650	+934.6
D/$\overline{C}$	196	−1410	+934.6
$\overline{SCE}$	197	−1170	+934.6
T2	198	−930	+934.6
SCLK	199	−690	+934.6
V_{SS2}	200	−530	+934.6
V_{SS2}	201	−450	+934.6
V_{SS2}	202	−370	+934.6
V_{SS2}	203	−290	+934.6
V_{SS2}	204	−210	+934.6
V_{SS2}	205	−130	+934.6
V_{SS2}	206	−50	+934.6
V_{SS2}	207	+30	+934.6
V_{SS2}	208	+110	+934.6
V_{SS2}	209	+190	+934.6
V_{SS2}	210	+270	+934.6
V_{SS2}	211	+350	+934.6
V_{SS2}	212	+430	+934.6
V_{SS2}	213	+510	+934.6
V_{SS1}	214	+670	+934.6
V_{SS1}	215	+750	+934.6
V_{SS1}	216	+830	+934.6
V_{SS1}	217	+910	+934.6
T1	218	+1150	+934.6
T5	219	+1630	+934.6
T4	220	+2030	+934.6
V_{SS1}	221	+2110	+934.6
V_{SS1}	222	+2190	+934.6
T3	223	+2270	+934.6
V_{LCDIN}	224	+2510	+934.6
V_{LCDIN}	225	+2590	+934.6
V_{LCDIN}	226	+2670	+934.6
V_{LCDIN}	227	+2750	+934.6
V_{LCDIN}	228	+2830	+934.6
V_{LCDIN}	229	+2910	+934.6
V_{LCDOUT}	230	+3070	+934.6
V_{LCDOUT}	231	+3150	+934.6

SYMBOL	PAD	COORDINATES	
		x	y
V_{LCDOUT}	232	+3230	+934.6
V_{LCDOUT}	233	+3310	+934.6
V_{LCDOUT}	234	+3390	+934.6
V_{LCDOUT}	235	+3470	+934.6
V_{LCDOUT}	236	+3550	+934.6
$V_{LCDSENSE}$	237	+3630	+934.6
Alignment marks			
Circle 1		+5185	–910.8
Circle 2		–5185	–910.8
Circle 3		–4160	+909.7
Circle 4		+4160	+909.7

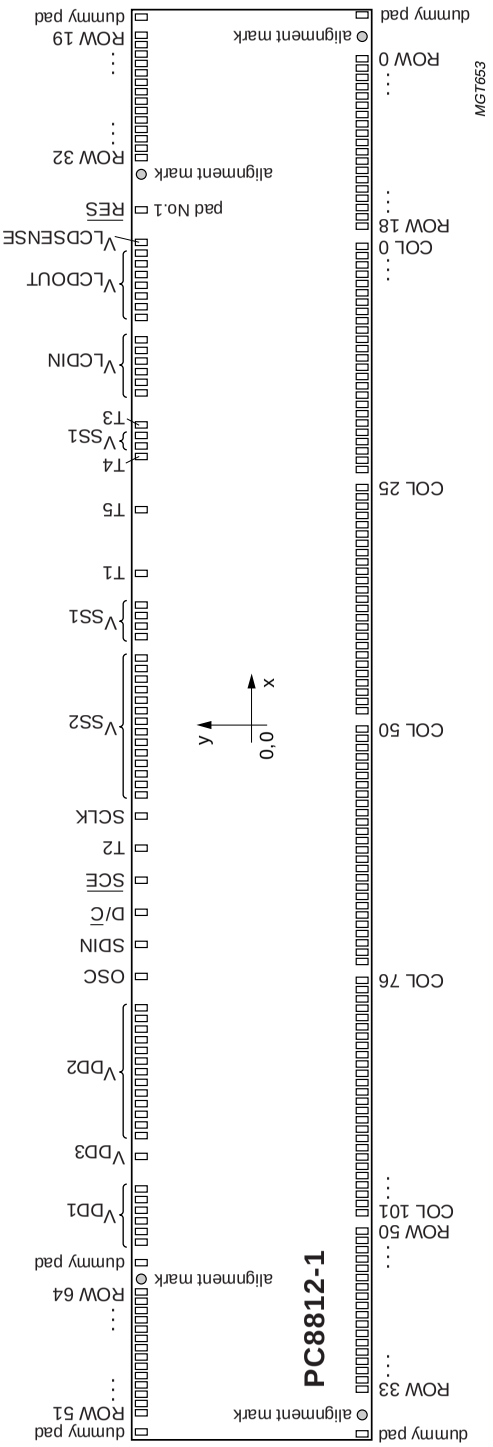


Fig.20 Bonding pad locations.

(1) The alignment marks are circular with a diameter of 100 µm.
(2) Maximum chip size: 2.1 × 10.9 mm.

21 DEVICE PROTECTION DIAGRAM

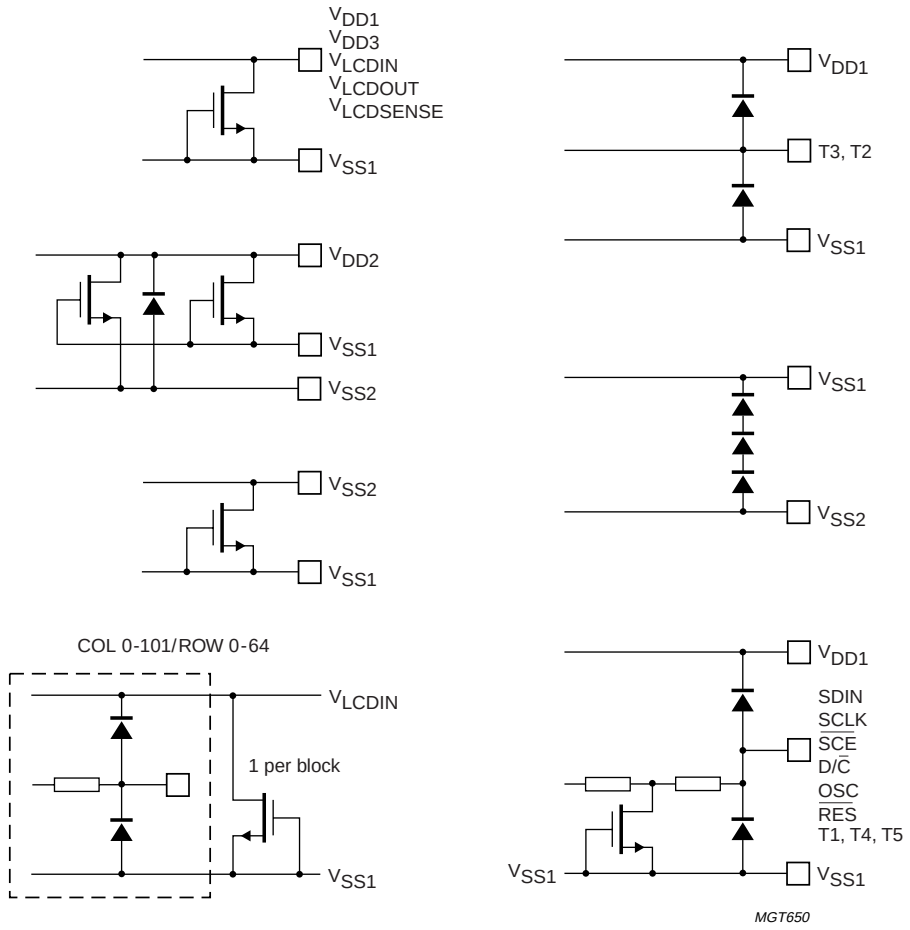


Fig.21 Device protection diagram.

22 TRAY INFORMATION

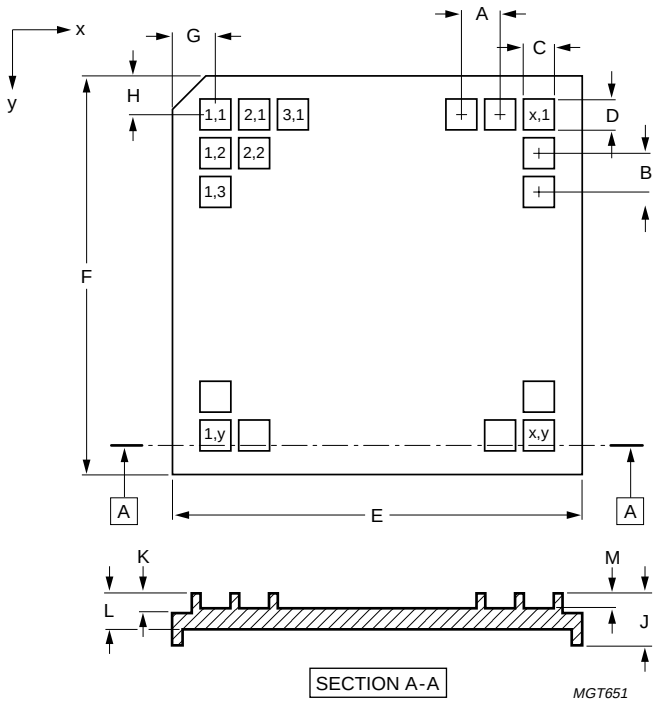
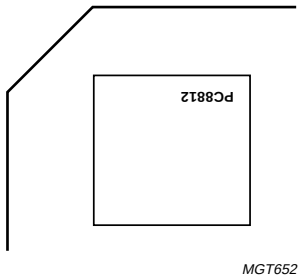


Fig.22 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.23 Tray alignment.

Table 10 Tray dimensions

DIMENSION	DESCRIPTION	VALUE
A	pocket pitch; x direction	13.77 mm
B	pocket pitch; y direction	4.37 mm
C	pocket width; x direction	11.04 mm
D	pocket width; y direction	2.24 mm
E	tray width; x direction	50.8 mm
F	tray width; y direction	50.8 mm
G	distance from cut corner to pocket (1 and 1) centre	11.68 mm
H	distance from cut corner to pocket (1 and 1) centre	5.74 mm
J	tray thickness	3.96 mm
K	tray cross section	1.78 mm
L	tray cross section	2.49 mm
M	pocket depth	0.89 mm
x	no. pockets in x direction	3
y	no. pockets in y direction	10

23 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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