CONTENTS

1 FEATURES

- Low power CMOS:
  - maximum operating current:
    2.0 mA (PCF8582C-2)
    2.5 mA (PCF8594C-2)
    4.0 mA (PCF8598C-2)
  - maximum standby current 10 μA (at 6.0 V), typical 4 μA
- Non-volatile storage of:
  - 2 kbits organized as 256 × 8-bit (PCF8582C-2)
  - 4 kbits organized as 512 × 8-bit (PCF8594C-2)
  - 8 kbits organized as 1024 × 8-bit (PCF8598C-2)
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations:
  - byte write mode
  - 8-byte page write mode
    (minimizes total write time per byte)
- Read operations:
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on-reset
- High reliability by using a redundant storage code
- Endurance: 1000000 Erase/Write (E/W) cycles at T_{amb} = 22 °C
- 10 years non-volatile data retention time
- Pin and address compatible to: PCF8570, PCF8571, PCF8572 and PCF8581.

2 GENERAL DESCRIPTION

The PCF85xxC-2 is a family of floating gate Electrically Erasable Programmable Read Only Memories (EEPROMs) with 2, 4 and 8 kbits (256, 512 and 1024 × 8-bit). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases the reliability compared to conventional EEPROMs. Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCF85xxC-2 devices may be connected to the I²C-bus. Chip select is accomplished by three address inputs (A0, A1 and A2).

Timing of the E/W cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit. There is an option of using an external clock for timing the length of an E/W cycle.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current read	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	–	60	μA
		V_{DD} = 6 V	–	200	μA
I_{DDW}	supply current E/W	f_{SCL} = 100 kHz			
	PCF8582C-2	V_{DD} = 2.5 V	–	0.6	mA
		V_{DD} = 6 V	–	2.0	mA
	PCF8594C-2	V_{DD} = 2.5 V	–	0.8	mA
		V_{DD} = 6 V	–	2.5	mA
	PCF8598C-2	V_{DD} = 2.5 V	–	1.0	mA
		V_{DD} = 6 V	–	4.0	mA
$I_{DD(stb)}$	standby supply current	V_{DD} = 2.5 V	–	3.5	μA
		V_{DD} = 6 V	–	10	μA

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8582C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8594C-2P			
PCF8598C-2P			
PCF8582C-2T	SO8	plastic small outline package; 8 leads (straight); body width 3.9 mm	SOT96-1
PCF8594C-2T			
PCF8598C-2T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Note

1. The Most Significant Bit (MSB) ‘b7’ is sent first.

6 BLOCK DIAGRAM

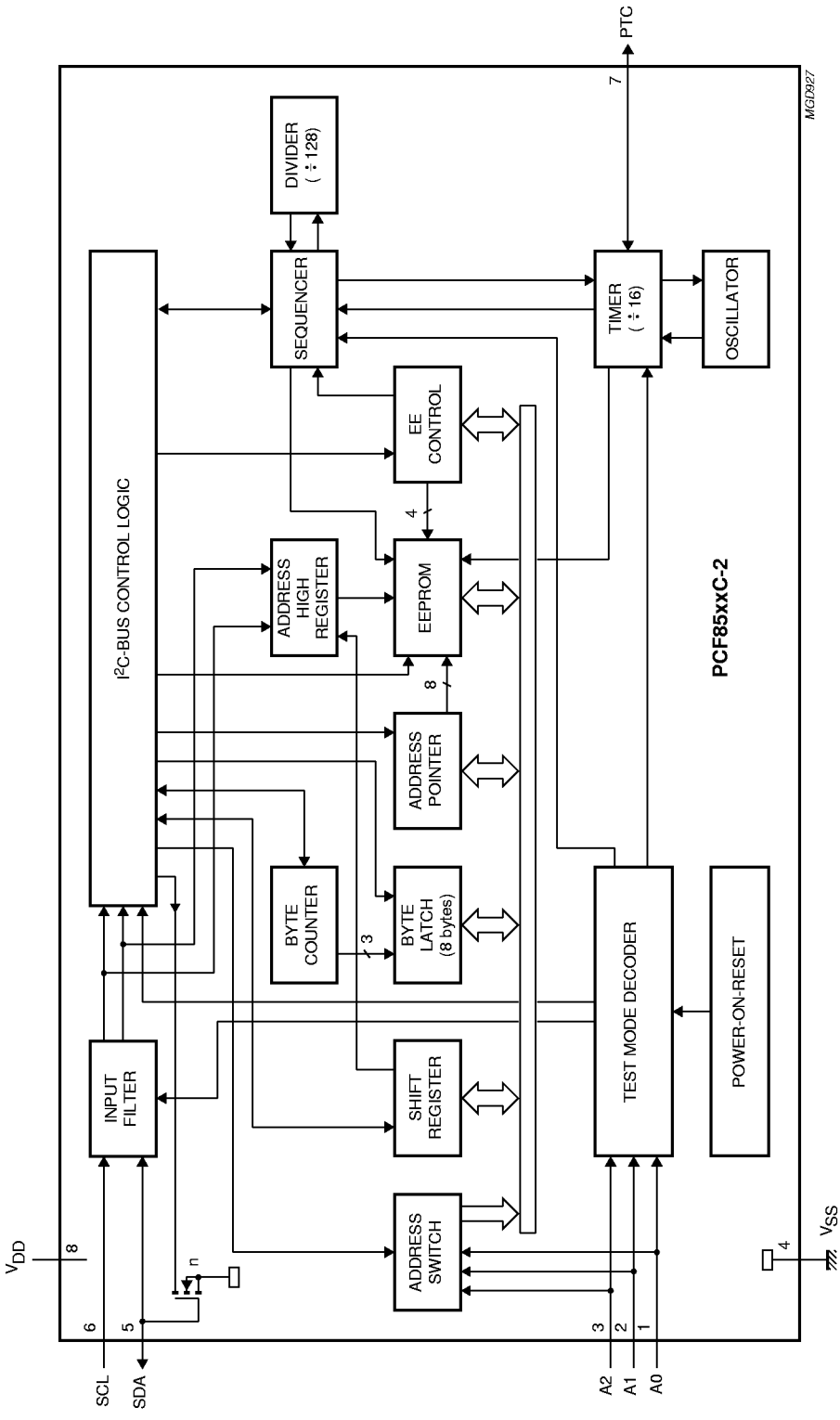


Fig.1 Block diagram.

The pin numbers in this block diagram refer to the PCF8582C-2.
For PCF8594C-2 and PCF8598C-2 please see Chapter 7.

7 PINNING

7.1 Pin description PCF8582C-2

SYMBOL	PIN	DESCRIPTION
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

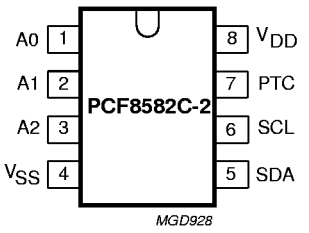


Fig.2 Pin configuration PCF8582C-2.

7.2 Pin description PCF8594C-2

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

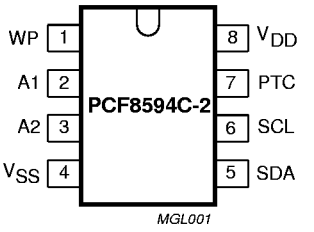


Fig.3 Pin configuration PCF8594C-2.

7.3 Pin description PCF8598C-2

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
n.c.	2	not connected
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

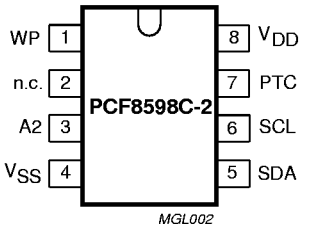


Fig.4 Pin configuration PCF8598C-2.

8 I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

8.1 Bus conditions

The following bus conditions have been defined:

- **Bus not busy**: both data and clock lines remain HIGH.
- **Start data transfer**: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the START condition.
- **Stop data transfer**: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the STOP condition.
- **Data valid**: the state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

8.2 Data transfer

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes, transferred between the START and STOP conditions is limited to 7 bytes in the E/W mode and 8 bytes in the page E/W mode.

Data transfer is unlimited in the read mode.
The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF85xxC-2 operates in both modes.

By definition a device that sends a signal is called a 'transmitter', and the device which receives the signal is called a 'receiver'. The device which controls the signal is called the 'master'. The devices that are controlled by the master are called 'slaves'.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account.
A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

8.3 Device addressing

Following a START condition the bus master must output the address of the slave it is accessing. The 4 MSBs of the slave address are the device type identifier (see Fig.5). For the PCF85xxC-2 this is fixed to '1010'.

The next three significant bits address a particular device or memory page (page = 256 bytes of memory). A system could have up to eight PCF8582C-2 (or four PCF8594C-2 containing two memory pages each or two PCF8598C-2 containing four memory pages each, respectively) devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

Address bits must be connected to either V_{DD} or V_{SS}.

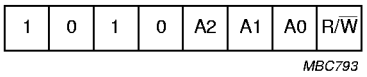


Fig.5 Slave address.

8.4 Write operations

8.4.1 BYTE/WORD WRITE

For a write operation the PCF85xxC-2 requires a second address field. This address field is a word address providing access to the 256 words of memory. Upon receipt of the word address the PCF85xxC-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a STOP condition or transmit up to six more bytes of data and then terminate by generating a STOP condition.

After this STOP condition the E/W cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte.

During the E/W cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

8.4.2 PAGE WRITE

The PCF85xxC-2 is capable of an eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCF85xxC-2 will respond with an acknowledge.
The typical E/W time in this mode is 9 × 3.5 ms = 31.5 ms. Erasing a block of 8 bytes in page mode takes typical 3.5 ms and sequential writing of these 8 bytes another typical 28 ms.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. The slave acknowledges the reception of each data byte with an ACK. The I²C-bus data transfer is terminated by the master after the 8th byte with a STOP condition. If the master transmits more than eight bytes prior to generating the STOP condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored and no programming will be done. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

8.4.3 REMARK

A write to the EEPROM is always performed if the pin WP is LOW (not on PCF8582C-2). If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCF85xxC-2 when one of the upper 256 EEPROM bytes (PCF8594C-2) or 512 EEPROM bytes (PCF8598C-2) is addressed. However, an acknowledge will be given after the slave address and the word address.

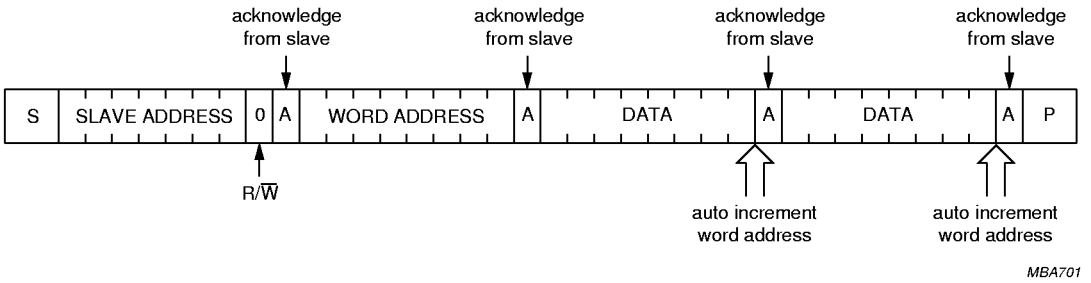


Fig.6 Auto increment memory word address; two byte write.

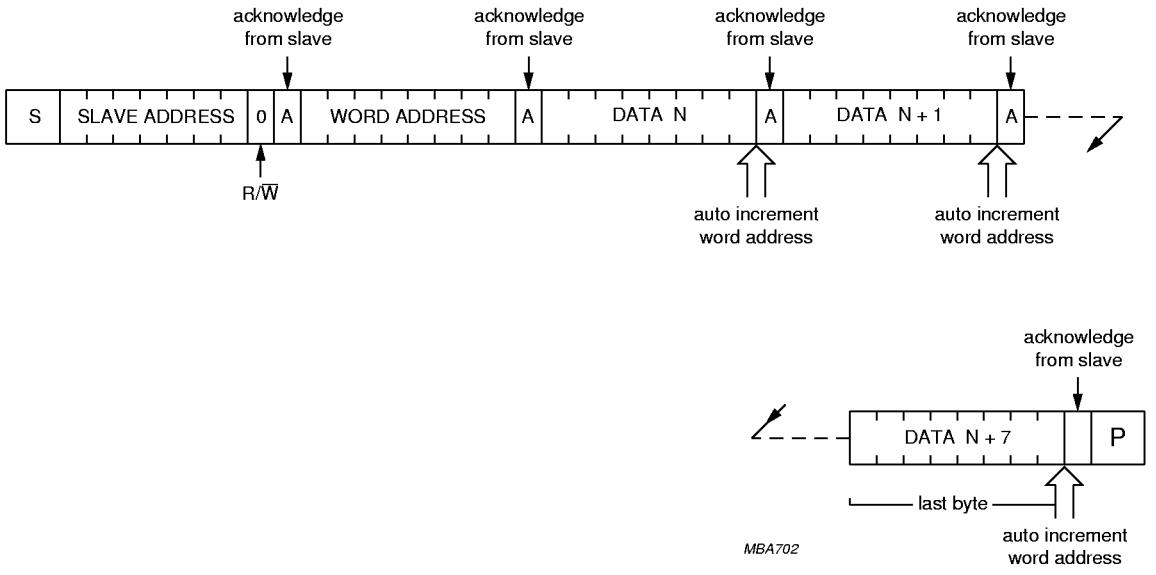


Fig.7 Page write operation; eight bytes.

8.5 Read operations

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1.

There are three basic read operations; current address read, random read and sequential read sequential read.

8.5.1 REMARK

The lower 8 bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0 and from 511 to 256.

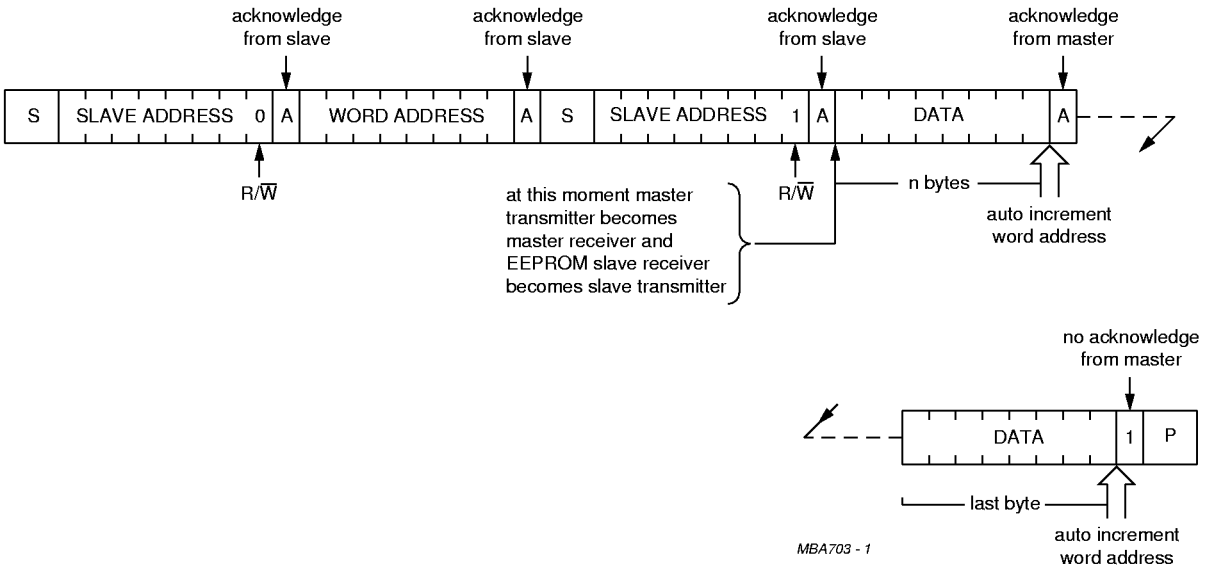


Fig.8 Master reads PCF85xxC-2 slave after setting word address (write word address; read data).

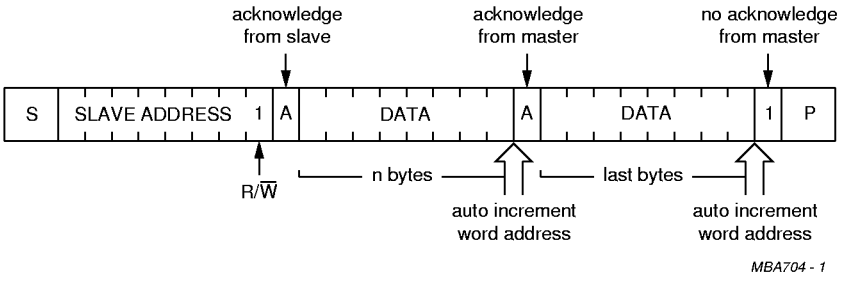


Fig.9 Master reads PCF85xxC-2 immediately after first byte (read mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+6.5	V
V_I	input voltage on any input pin	$\|Z_i\| > 500\ \Omega$	$V_{SS} - 0.8$	+6.5	V
I_I	input current on any input pin		−	1	mA
I_O	output current		−	10	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C

10 CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current read	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	−	60	μA
		V_{DD} = 6.0 V	−	200	μA
I_{DDW}	supply current E/W	f_{SCL} = 100 kHz			
	PCF8582C-2	V_{DD} = 2.5 V	−	0.6	mA
		V_{DD} = 6.0 V	−	2.0	mA
	PCF8594C-2	V_{DD} = 2.5 V	−	0.8	mA
		V_{DD} = 6.0 V	−	2.5	mA
	PCF8598C-2	V_{DD} = 2.5 V	−	1.0	mA
		V_{DD} = 6.0 V	−	4.0	mA
$I_{DD(stb)}$	standby supply current	V_{DD} = 2.5 V	−	3.5	μA
		V_{DD} = 6.0 V	−	10	μA
PTC output (pin 7)					
V_{IL}	LOW level input voltage		−0.8	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	V_{DD} + 0.8	V
SCL input (pin 6)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	+6.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−	±1	μA
f_{SCL}	clock input frequency		0	100	kHz
C_I	input capacitance	$V_I = V_{SS}$	−	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		–0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	+6.5	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	μA
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	–	years

11 I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}; see Fig.10.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	μs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		4.0	–	μs
t_{LOW}	LOW level clock period		4.7	–	μs
t_{HIGH}	HIGH level clock period		4.0	–	μs
$t_{SU;STA}$	set-up time for STARt condition	repeated start	4.7	–	μs
$t_{HD;DAT}$	data hold time				
	for bus compatible masters		5	–	μs
	for bus devices	note 1	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	ns
t_r	SDA and SCL rise time		–	1	μs
t_f	SDA and SCL fall time		–	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	μs

Note

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

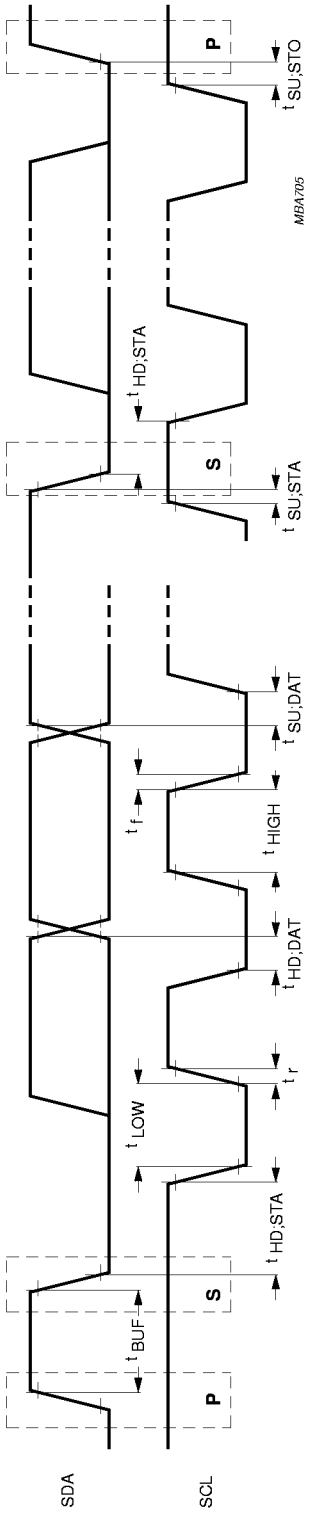


Fig.10 Timing requirements for the I²C-bus.

P = STOP condition; **S** = START condition.

12 WRITE CYCLE LIMITS

Selection of the chip address is achieved by connecting the A0, A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
E/W cycle timing						
$t_{E/W}$	E/W cycle time	internal oscillator	–	7	–	ms
		external clock	4	–	10	ms
Endurance						
$N_{E/W}$	E/W cycle per byte	T_{amb} = –40 to +85 °C	100000	–	–	cycles
		T_{amb} = 22 °C	–	1000000	–	cycles

13 EXTERNAL CLOCK TIMING

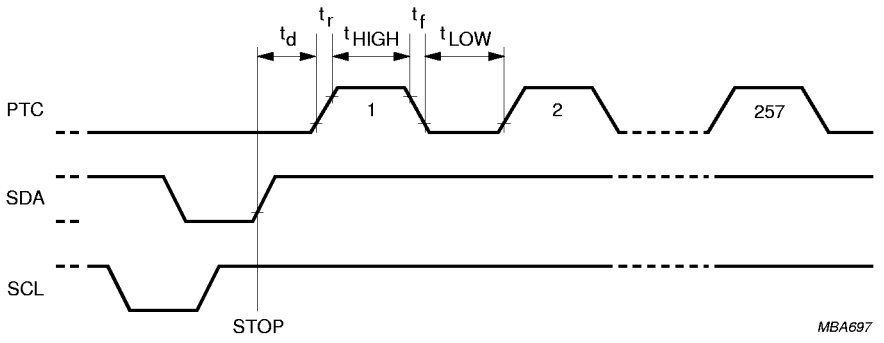


Fig.11 One byte E/W cycle.

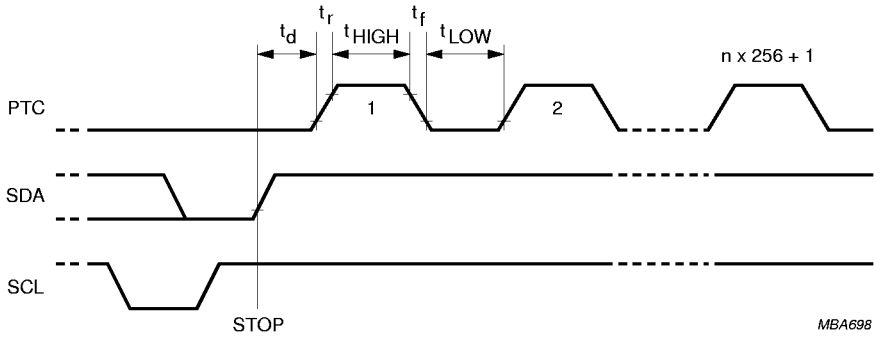


Fig.12 n bytes E/W cycle (n = 2 to 7).

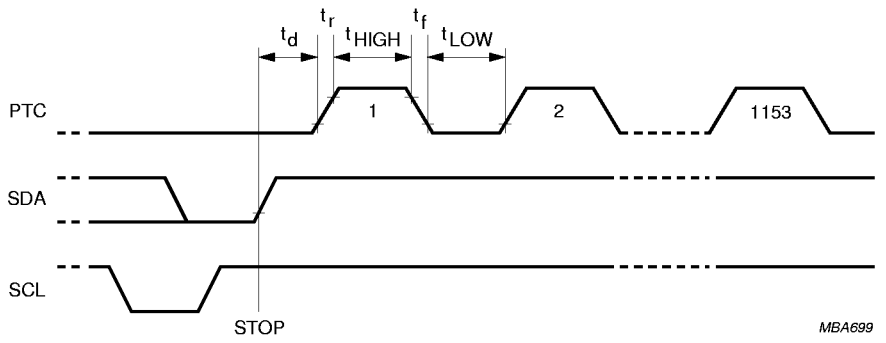
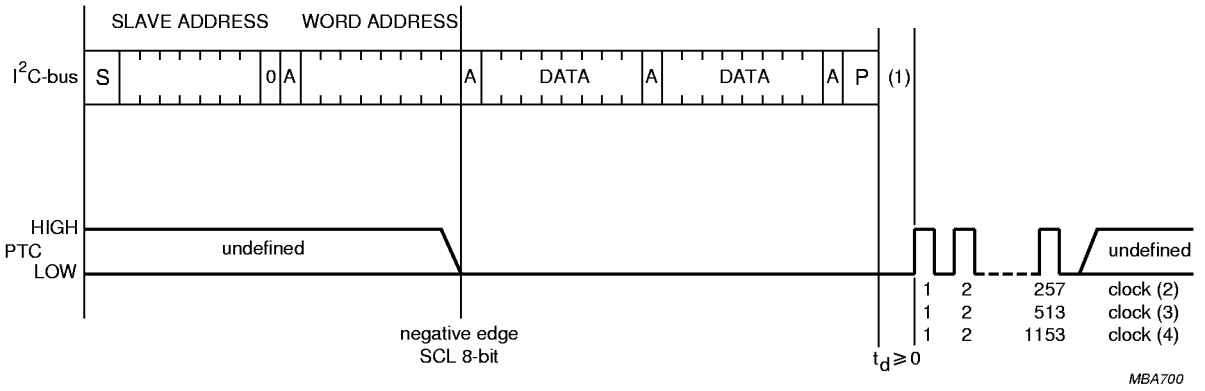


Fig.13 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eighth bits of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

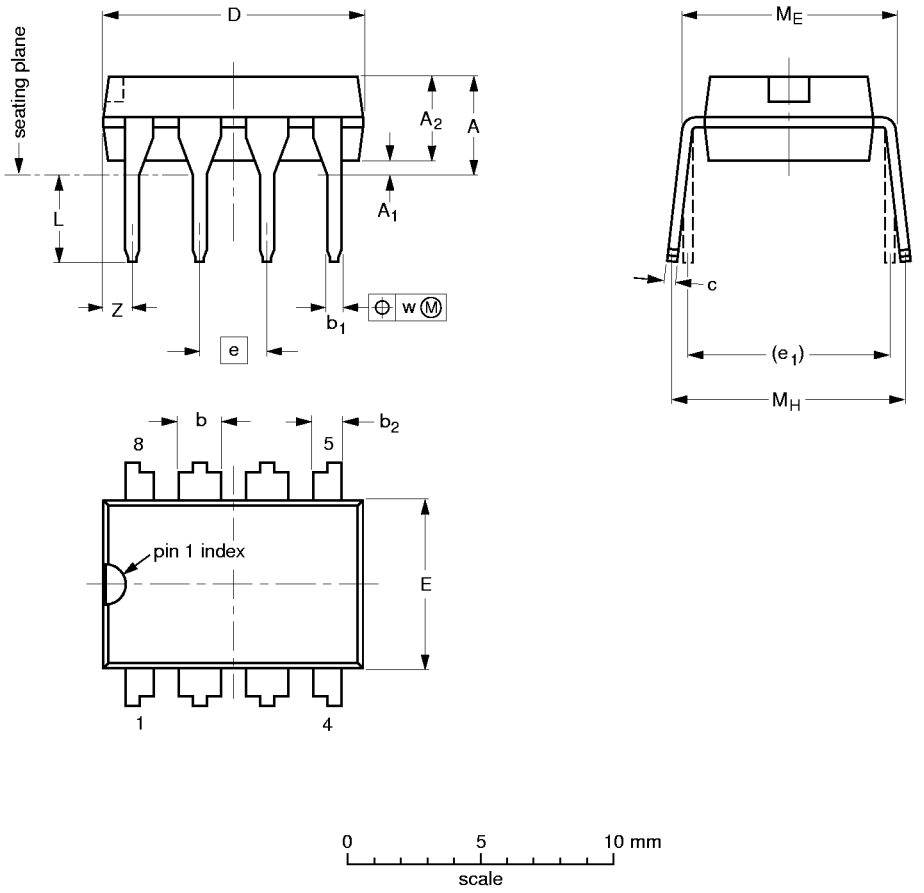
(3) 2-byte programming.

(4) One page (8 bytes) programming.

Fig.14 External clock.

14 PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

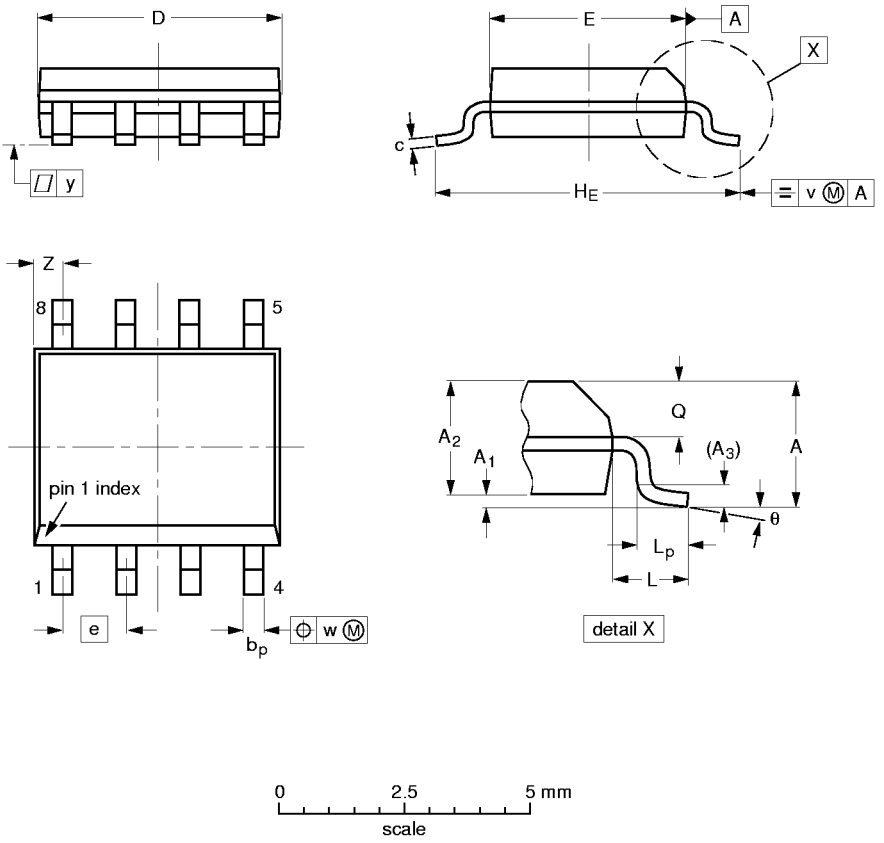
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

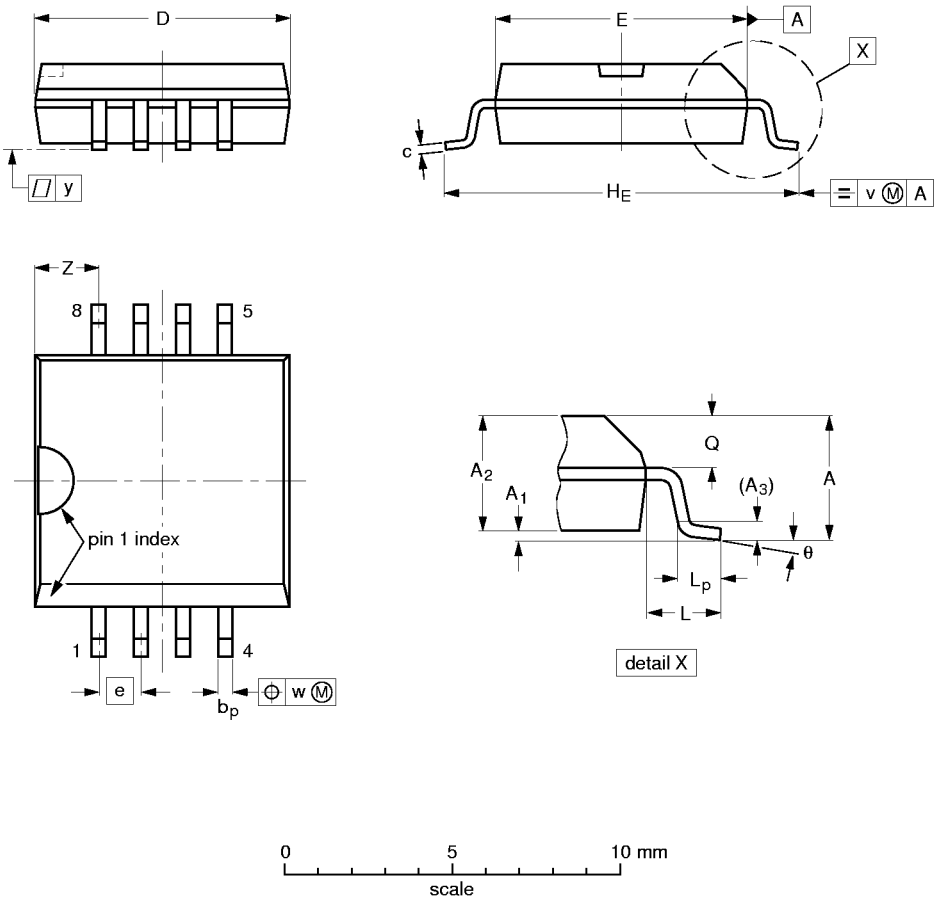
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.42 0.39	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~91-08-13~~ 95-02-25

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 DIP

15.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15.3 SO

15.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.