DATA SHEET

PCF85116-3

2048 × 8-bit CMOS EEPROM with I²C-bus interface

Product specification
Supersedes data of 1997 Feb 24
File under Integrated Circuits, IC12

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Philips Semiconductors

PHILIPS

2048 × 8-bit CMOS EEPROM with I²C-bus interface

PCF85116-3

CONTENTS

1 FEATURES

- Low power CMOS:
  - maximum operating current 1.0 mA
  - maximum standby current 10 μA (at 5.5 V), typical 4 μA
- Non-volatile storage of 16 kbits organized as eight blocks of 256 × 8-bit each
- Single supply with full operation down to 2.7 V
- On-chip voltage multiplier
- Serial input/output I²C-bus (100 kbits/s standard-mode and 400 kbits/s fast-mode)
- Write operations: multi byte write mode up to 32 bytes
- Write-protection input
- Read operations:
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on-reset
- High reliability by using redundant EEPROM cells
- Endurance: 1000000 Erase/Write (E/W) cycles at T_{amb} = 22 °C
- 20 years non-volatile data retention time (minimum)
- Pin and address compatible to the PCx85xxC-2 family (see also Section 2.1)
- 2 kV ESD protection (Human Body model).

2 DESCRIPTION

The PCF85116-3 is an 16 kbits (2048 × 8-bit) floating gate Electrically Erasable Programmable Read Only Memory (EEPROM). By using redundant EEPROM cells it is fault tolerant to single bit errors. In most cases multi bit errors are also covered. This feature dramatically increases reliability compared to conventional EEPROM memories. Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Only one PCF85116-3 device is required to support all eight blocks of 256 × 8-bit each.

Timing of the E/W cycle is carried out internally, thus no external components are required. A write-protection input at pin 7 (WP) allows disabling of write-commands from the master by a hardware signal. When pin 7 is HIGH the data bytes received will not be acknowledged by the PCF85116-3 and the EEPROM contents are not changed.

2.1 Remark

The PCF85116-3 is pin and address compatible to the PCx85xxC-2 family. The PCF85116-3 covers the whole address space of 16 kbits; address inputs are no longer needed. Therefore, pins 1 to 3 are not connected.
The write-protection input is at pin 7.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.7	5.5	V
I_{DDR}	supply current read	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	–	1.0	mA
I_{DDW}	supply current E/W	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	–	1.0	mA
I_{stb}	standby supply current	V_{DD} = 2.7 V	–	6	μA
		V_{DD} = 5.5 V	–	10	μA

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF85116-3P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF85116-3T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	MEM SEL	MEM SEL	MEM SEL	R/$\overline{W}$

Note

1. The Most Significant Bit (MSB) ‘b7’ is sent first.

6 BLOCK DIAGRAM

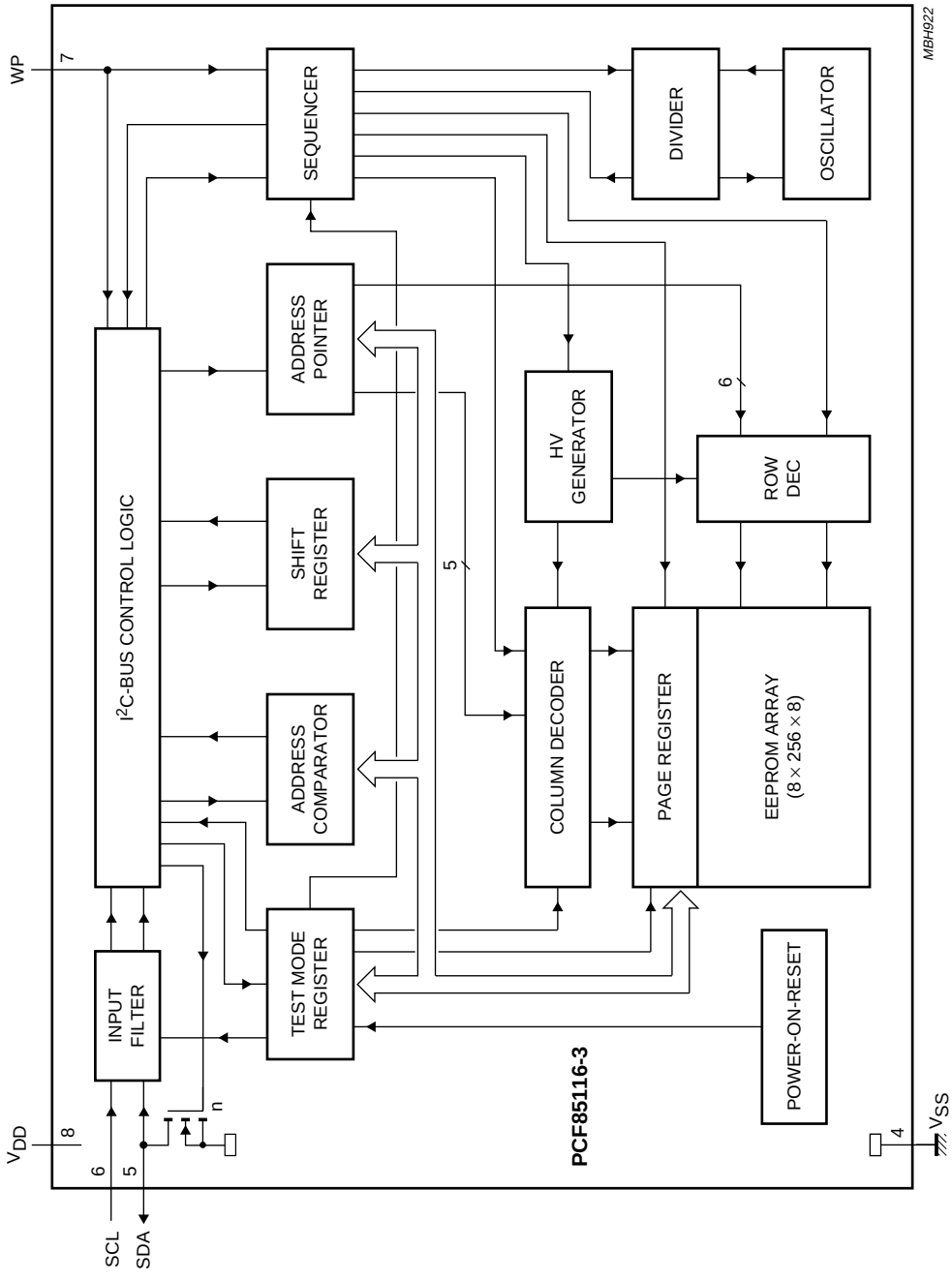


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
n.c.	3	not connected
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
WP	7	write-protection input
V_{DD}	8	positive supply voltage

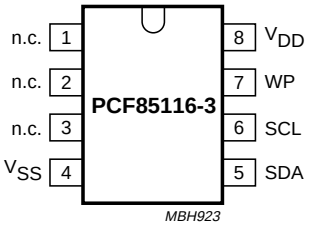


Fig.2 Pin configuration.

8 I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

8.1 Bus conditions

The following bus conditions have been defined:

- Bus not busy: both data and clock lines remain HIGH.
- Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the START condition
- Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the STOP condition
- Data valid: the state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

8.2 Data transfer

Each data transfer is initiated with a START condition and terminated with a STOP condition; the number of the data bytes, transferred between the START and STOP conditions is limited to 32 bytes in the E/W mode.

Data transfer is unlimited in the read mode.
The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate), a high speed mode (100 kHz clock rate) and a fast speed mode (400 kHz clock rate) are defined.
The PCF85116-3 operates in all three modes.

By definition a device that sends a signal is called a ‘transmitter’, and the device which receives the signal is called a ‘receiver’. The device which controls the signal is called the ‘master’. The devices that are controlled by the master are called ‘slaves’.

Each byte is followed by one acknowledge bit.
This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account.
A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

8.3 Device addressing

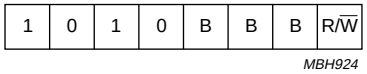


Fig.3 Slave address.

Following a START condition the bus master must output the address of the slave it is accessing. The 4 MSBs of the slave address are the device type identifier (see Fig.3). For the PCF85116-3 this is fixed to '1010'.

The next three significant bits of the slave address field are the block selection bits. It is used by the host to select one out of eight blocks (1 block = 256 bytes of memory). These are, in effect, the three most significant bits of the word address.

The last bit of the slave address defines the operation to be performed. When R/$\overline{W}$ is set to logic 1 a read operation is selected.

8.4 Write operations

8.4.1 BYTE/WORD WRITE

For a write operation the PCF85116-3 requires a second address field. This address field is a word address providing access to any one of the eight blocks of memory. Upon receipt of the word address the PCF85116-3 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master terminates the transfer by generating a STOP condition.

After this stop condition the E/W cycle starts and the bus is free for another transmission. Its duration is maximum 10 ms.

During the E/W cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

8.4.2 PAGE WRITE

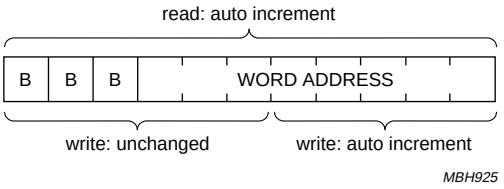


Fig.4 Auto increment of memory address.

The PCF85116-3 is capable of an 32-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit up to 32 data bytes within one transmission. After receipt of each byte the PCF85116-3 will respond with an acknowledge. The master terminates the transfer by generating a STOP condition. The maximum total E/W time in this mode is 10 ms.

After the receipt of each data byte the six high order bits of the memory address providing access to one of the 64 pages of the memory remain unchanged. The five low order bits of the memory address will be incremented only (see Fig.3). By these five bits a single byte within the page in access is selected. By an increment the memory address may change from 31 to 0, from 63 to 32, etc. If the master transmits more than 32 bytes prior to generating the STOP condition, data within the addressed page may be overwritten and unpredictable results may occur. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

8.4.3 REMARK

Write accesses to the EEPROM are enabled if the pin WP is LOW. When WP is HIGH the EEPROM is write-protected and no acknowledge will be given by the PCF85116-3 when data is sent. However, an acknowledge will be given after the slave address and the word address.

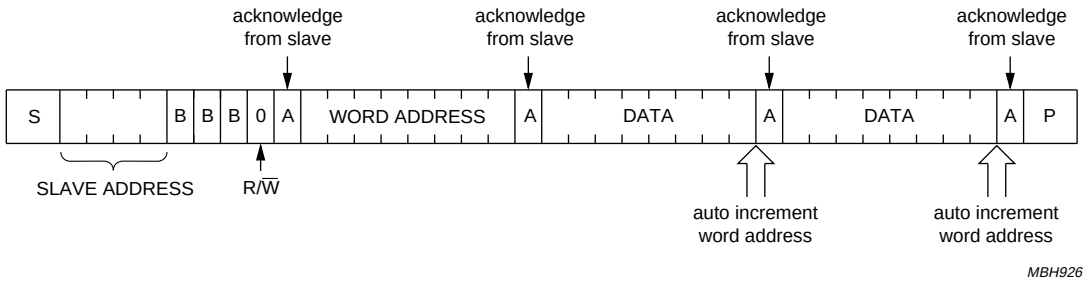


Fig.5 Auto increment memory address; two byte write.

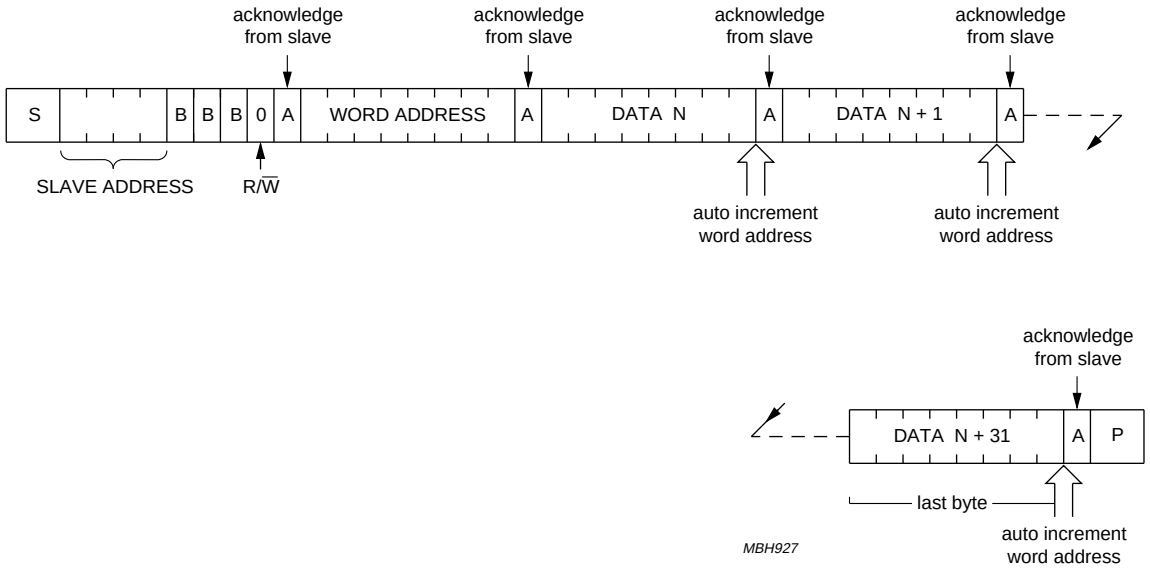


Fig.6 Page write operation; 32 bytes.

8.5 Read operations

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address (R/$\overline{W}$) is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

8.5.1 REMARK

During read operations all bits of the memory address are incremented after each transmission of a data byte. Contrary to write operations an overflow of the memory address occurs from 2047 to 0 (see Fig.3).

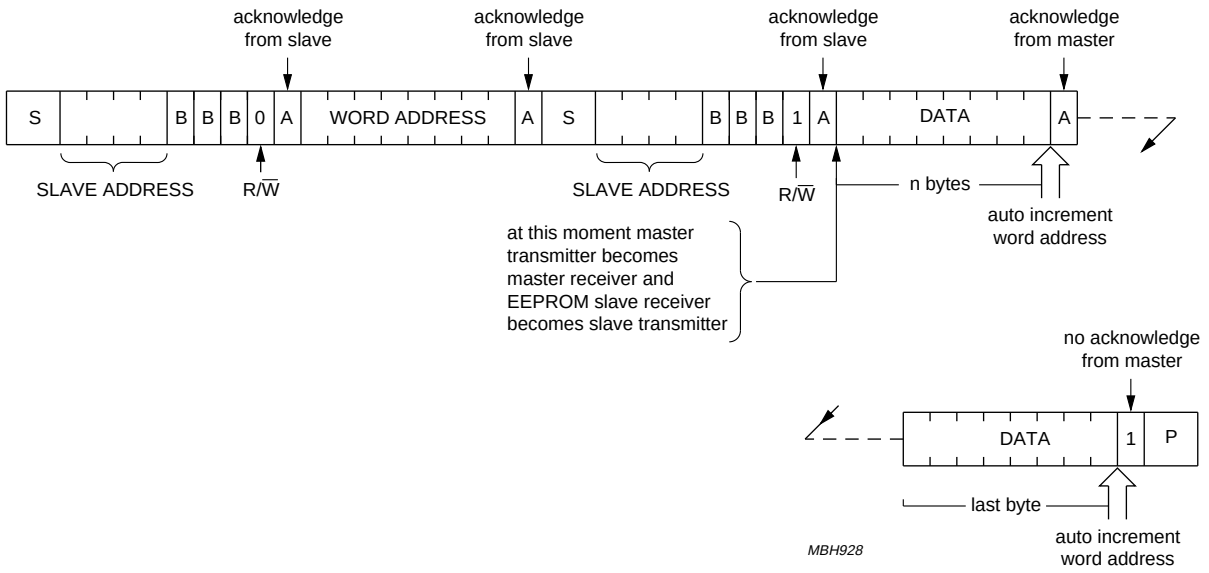


Fig.7 Master reads PCx85116-3 slave after setting word address (write word address; read data).

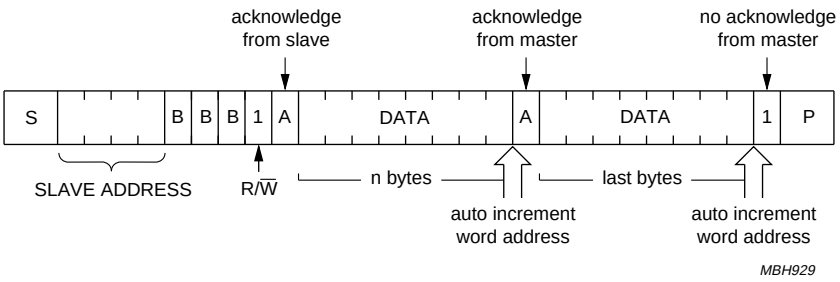


Fig.8 Master reads PCx85116-3 immediately after first byte (read mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.3	+6.5	V
V_I	input voltage on any pin	$\|Z_i\| > 500\ \Omega$	$V_{SS} - 0.8$	+6.5	V
I_I	input current on any pin		–	1	mA
I_O	output current		–	10	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{esd}	electrostatic discharge voltage	note 1	2	–	kV

Note

1. ESD Human Body model Q22 at T_{amb} = 22 °C; discharge procedure according to MIL-STD-883C Method 3015.

10 CHARACTERISTICS

V_{DD} = 2.7 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage		2.7	5.5	V
I_{DDR}	supply current read	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	–	1.0	mA
I_{DDW}	supply current E/W	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	–	1.0	mA
$I_{DD(stb)}$	standby supply current	V_{DD} = 2.7 V	–	6	µA
		V_{DD} = 5.5 V	–	10	µA
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		–0.8	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	6.5	V
V_{OL1}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	–	0.4	V
V_{OL2}		I_{OL} = 6 mA; $V_{DD(min)}$	–	0.6	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	µA
$t_{o(f)}$	output fall time from V_{IHmin} to V_{ILmax}	note 1			
	with up to 3 mA sink current at V_{OL1}		$20 + 0.1C_b$	250	ns
	with up to 6 mA sink current at V_{OL2}		$20 + 0.1C_b$	250	ns
t_{SP}	pulse width of spikes suppressed by filter		0	100	ns
C_I	input capacitance	$V_I = V_{SS}$	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
SCL input (pin 6)					
V_{IL}	LOW level input voltage		–0.8	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	6.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	±1	µA
f_{SCL}	clock input frequency		0	400	kHz
t_{SP}	pulse width of spikes suppressed by filter		0	100	ns
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
WP input (pin 7)					
V_{IL}	LOW level input voltage		–0.8	$+0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	$V_{DD} + 0.8$	V
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	20	–	years

Note

1. The bus capacitance ranges from 10 to 400 pF (C_b = total capacitance of one bus line in pF).

11 I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN.	MAX.	MIN.	MAX.	
f_{SCL}	clock frequency		0	100	0	400	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	1.3	–	µs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW level clock period		4.7	–	1.3	–	µs
t_{HIGH}	HIGH level clock period		4.0	–	0.6	–	µs
$t_{SU;STA}$	set-up time for START condition	repeated start	4.7	–	0.6	–	µs
$t_{HD;DAT}$	data hold time						
	for CBUS compatible masters		5	–	–	–	µs
	for I²C-bus devices	note 1	0	–	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	100	–	ns
t_r	SDA and SCL rise time		–	1000	$20 + 0.1C_b$(2)	300	ns
t_f	SDA and SCL fall time		–	300	$20 + 0.1C_b$(2)	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	0.6	–	µs

Notes

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.
2. C_b = total capacitance of one bus line in pF.

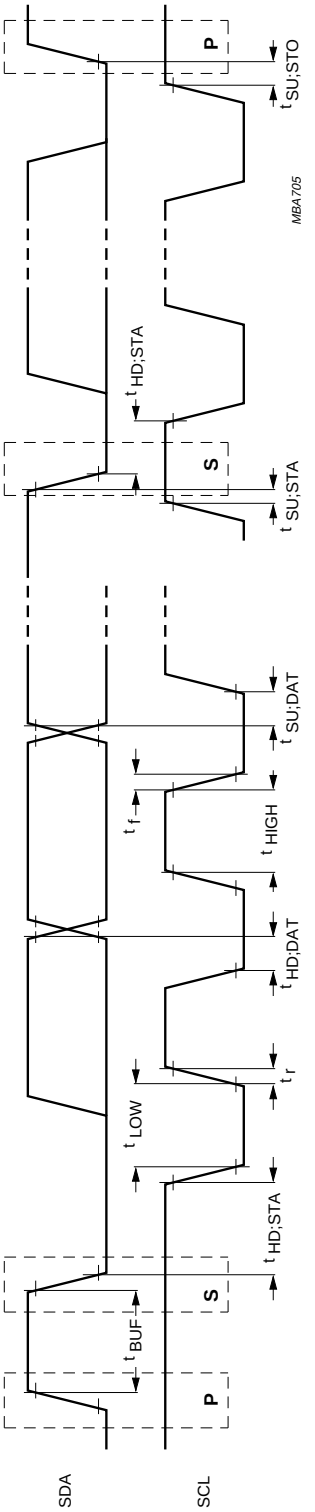


Fig.9 Timing requirements for the I²C-bus.

P = STOP condition; **S** = START condition.

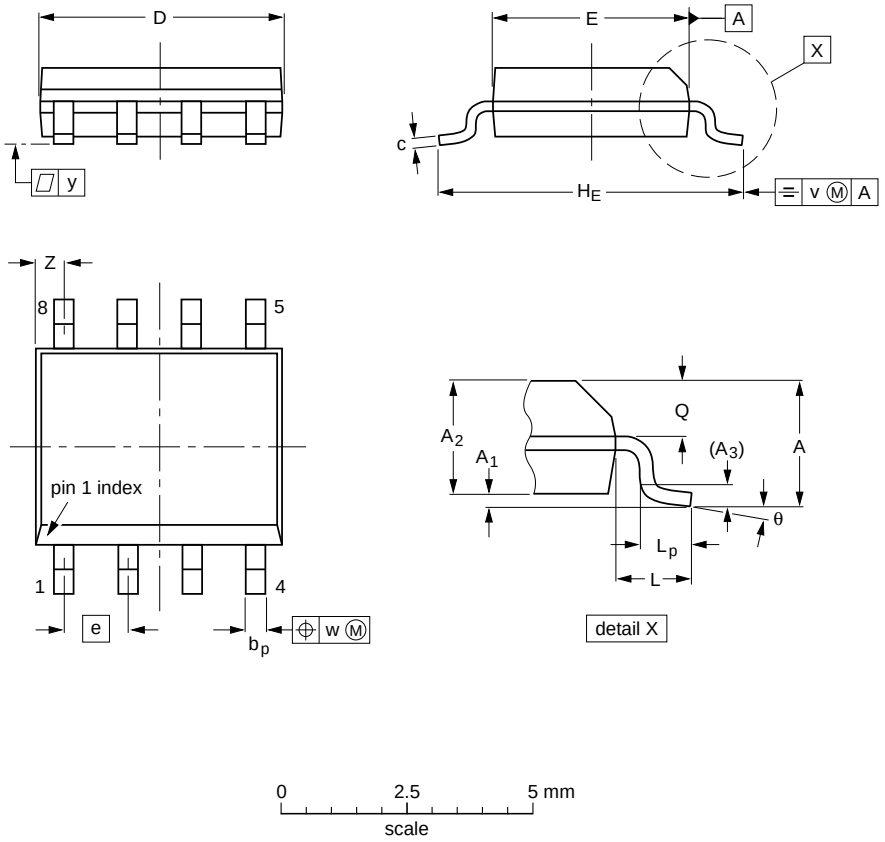
12 WRITE CYCLE LIMITS

The Power-on-reset circuit resets the I²C-bus logic with a set-up time of ≤10 µs.Enabling the chip is achieved by connecting the WP input to V_{SS}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
E/W cycle timing						
$t_{E/W}$	E/W cycle time		–	–	10	ms
Endurance						
$N_{E/W}$	E/W cycle per byte	T_{amb} = –40 to +85 °C	100000	–	–	cycles
		T_{amb} = 22 °C	1000000	–	–	cycles

13 PACKAGE OUTLINES

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

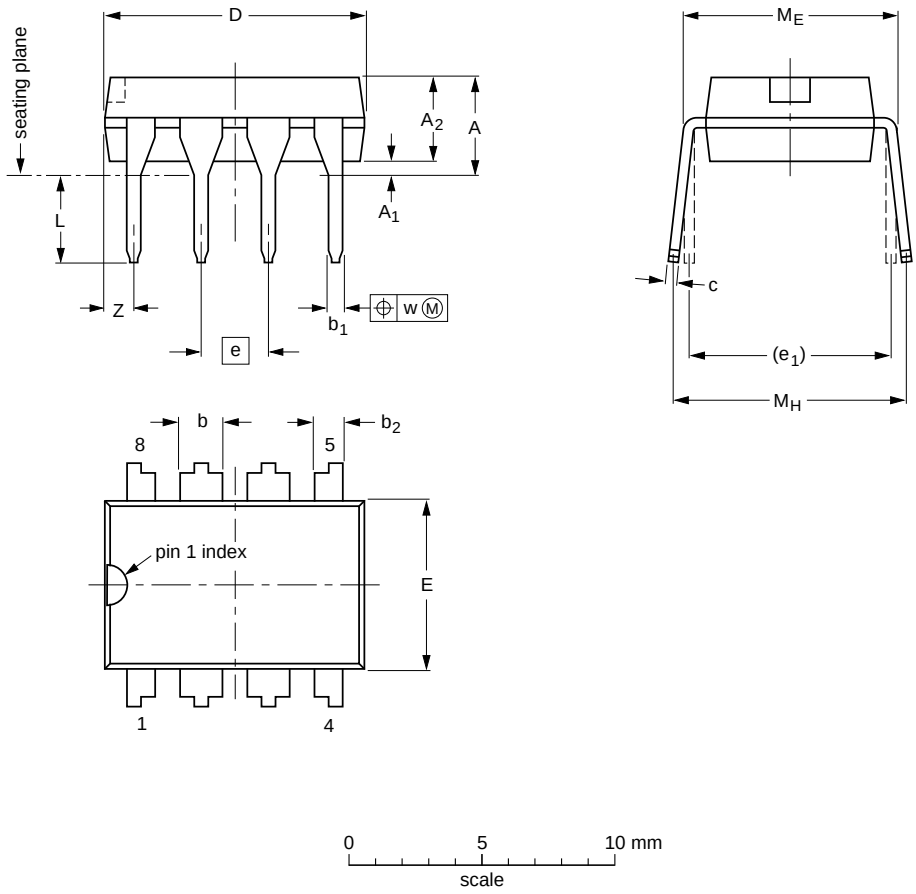
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

14.2 DIP

14.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 SO

14.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

17 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

Philips Semiconductors – a worldwide company

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