DATA SHEET

PCD509x2/zuu/v family
Low cost; low power DECT baseband controllers (ABC-PRO)

Objective specification
File under Integrated Circuits, IC17

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Philips
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CONTENTS

1 FEATURES

- The PCD50912 is designed for GAP compatible DECT handsets
- The PCD50922 is designed for GAP compatible DECT base stations serving up to six handsets
- Fully static 80C51 microcontroller
- Emulation supported for 80C51 program development
- Four 8-bit ports (P0, P1, P2 and P3), 32 I/O lines
- Dedicated port pins for keyboard, I^2C-bus, interrupt sources and/or external memory
- Fifteen interrupt sources (including those from TICB, BML and DSP) with two priority levels
- I^2C-bus interface
- UART with IrDA-compatible Data Transmission Mode
- 256 bytes of microcontroller main RAM
- 3 kbytes of microcontroller AUX RAM
- 1 kbyte of shared System Data RAM
- 64 kbytes of mask programmable ROM
- 128 kbyte address space for external ROM access, maximum 192 kbytes together with internal ROM
- 128 kbytes of external RAM addressable
- Embedded DSP with 6.912, 13.824 or 27.648 Mips
- Speech and IOM-2 interface
- BML for TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation, protected B-fields
- Local call and B-field loop-back
- Automatic receiver delay adjustment programmable per slot to correct for terminal mobility
- Phase error measurement and phase error correction by hardware
- Serial interface to synthesizer for frequency programming
- Programmable timing and polarity of radio-control signals
- Easy interfacing with radio circuits, operating at different supply voltages
- GMSK pulse shaper with two different pulse shapes (BT = 0.5 and BT = 0.8)
- Comparator for use as bit-slicer
- 3 channel time-multiplexed 8-bit ADC for RSSI, battery and general input voltage measurement
- Battery management supported by programmable current source for temperature or charge current measurement
- On-chip 8-bit DAC for various purposes
- Low power crystal oscillator at 13.824 MHz
- Programmable on-chip capacitors for frequency adjustment to 13.824 MHz with large pulling range
- High performance DAC and ADC for dynamic earpiece and dynamic or electret microphone
- Analog-to-digital path switchable sensitivity for microphone or line interface input
- On-chip reference voltage and supply for electret microphone
- Very low ohmic buzzer output
- Pulse density modulated or pulse width modulated buzzer output signal
- Power-on-reset
- Low power operation optimized for 2 battery cells in handset
- Long standby time due to reduced digital supply voltage and reduced activity in idle-locked mode
- Flexible supply voltage concept due to use of level shifters between each supply voltage domain
- Eight independent supply voltage domains:
  - 1.8 to 3.6 V for digital core, microcontroller ports P0 and P2, and also P1 and P3
  - 1.8 to 3.6 V for buzzer, oscillator and battery
  - 2.7 to 3.6 V for RF interface and analog circuits
- CMOS technology
- Small and flat LQFP80 package.

2 GENERAL DESCRIPTION

The PCD509x2 family is designed for low power GAP compatible DECT handset (PP) and base station (FP) applications. The circuit includes the audio interface, the DSP, the microcontroller and the Burst Mode Logic, and contains all functionality to convert speech and data signals from/to the analog side (microphone and earpiece or line interface circuit) to/from the radio side (1.152 Mbits/s data).

This circuit is a member of the ABC family, where A stands for ‘ADPCM codec’, B for ‘Burst Mode Logic’ and C for ‘microController’. The name ABC-PRO stands for PROfessional ABC.

The PCD509x2/zuu/v contains on-chip ROM for the embedded DSP code and on-chip ROM for the embedded microcontroller code. It is these ROM codes that differentiate between various chip derivatives. For each DSP code a separate DSP user manual is published. Please contact Philips Semiconductors for more information.

This family specification contains the hardware description that is independent of the used ROM codes.

The numerical digit ‘x’ in PCD509x2 determines the intended application area (e.g. PCD50912 for use in handsets or PCD50922 for use in simple base stations, etc.). The last numerical digit ‘2’ is used to denote hardware derivatives. The extension digits ‘z’ (A to Z) and ‘uu’ (00 to 99) denote the DSP and the microcontroller software version, respectively. The extension ‘v’ denotes the hardware version updates of the circuit.

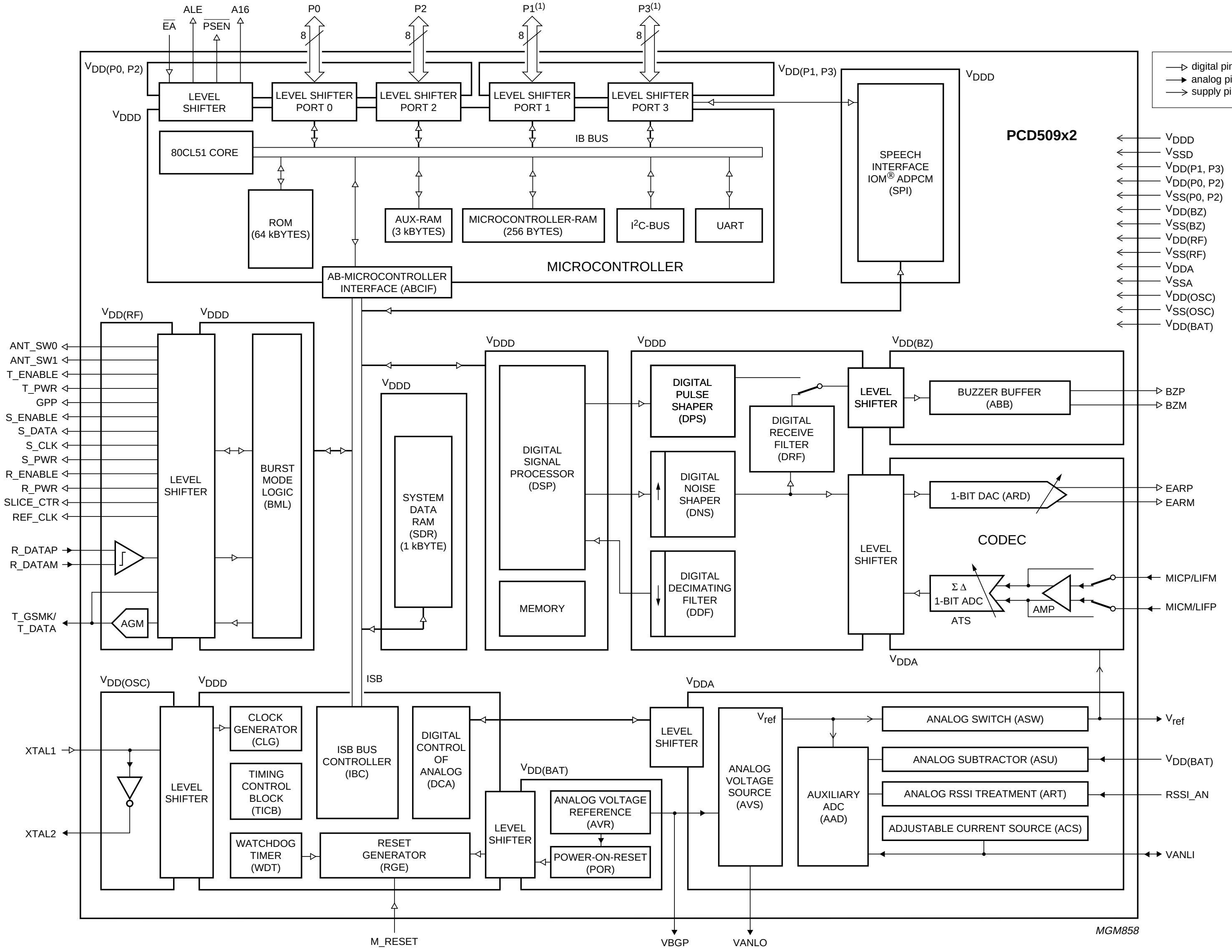
Although the microcontroller ROM code is present on-chip, an external program memory for the microcontroller code can be used. This is not the case for the DSP ROM code which is fixed by the chip version.

Throughout this family specification the term PCD509x2 is used to cover all sub types and versions. If any specific feature or parameter is connected to a certain sub type or version this will be specifically written. Until otherwise stated this family specification is valid for hardware version 1 (v = 1).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD50912H	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
PCD50922H			

4 BLOCK DIAGRAM



(1) Ports 1 and 3 are shared with alternative functions.

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

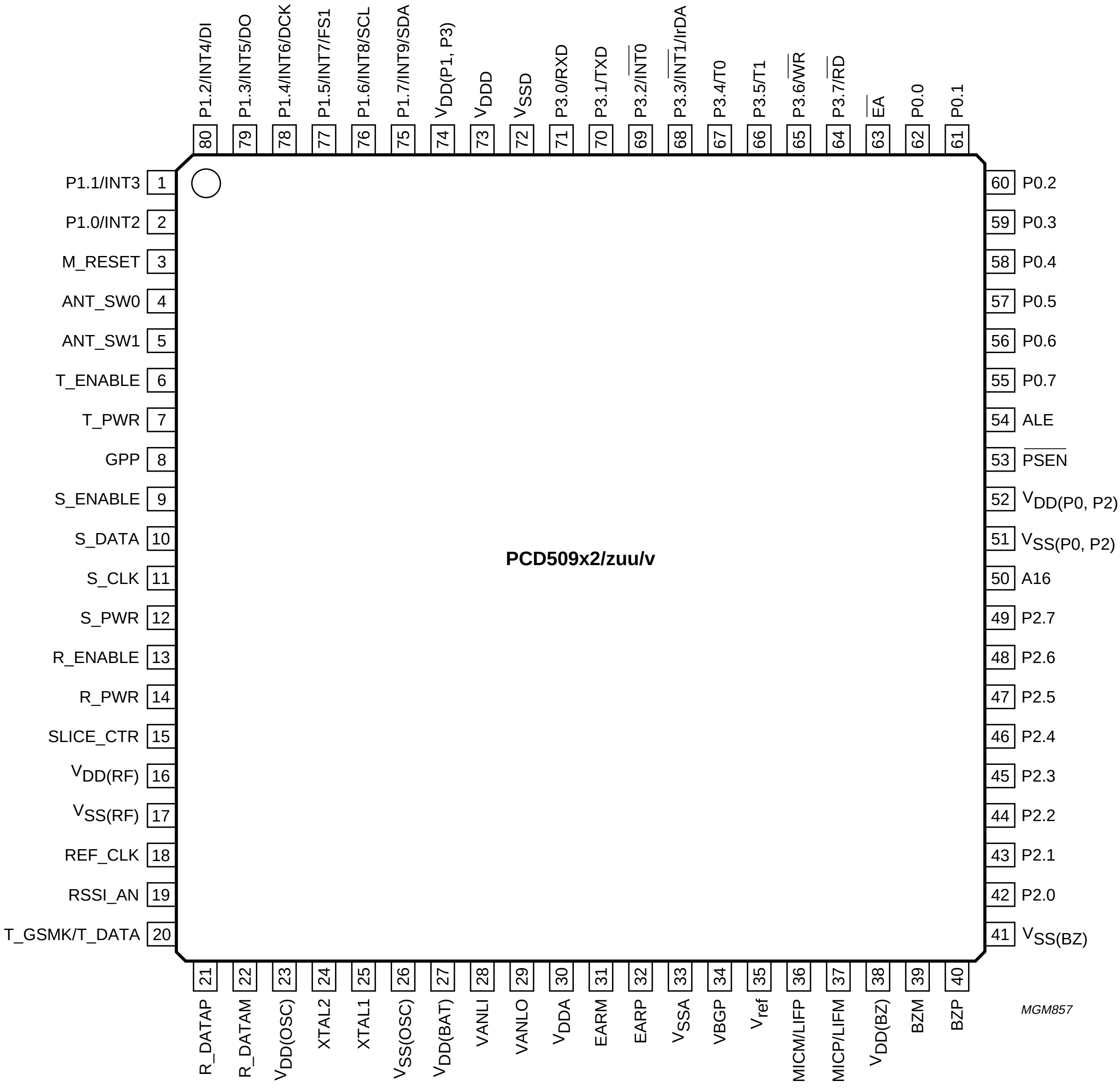


Fig.2 Pin configuration (LQPF80).

5.2 Pin description

Table 1 LQFP80 package

SYMBOL	PIN	I/O	STATE AFTER RESET(1)	SUPPLY DOMAIN	DESCRIPTION
P1.1/INT3	1	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 3
P1.0/INT2	2	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 2
M_RESET	3	I	–	V_{DDD}	master reset input (Schmitt trigger)
ANT_SW0	4	O	HIGH	$V_{DD(RF)}$	antenna switch 0
ANT_SW1	5	O	HIGH	$V_{DD(RF)}$	antenna switch 1
T_ENABLE	6	O	HIGH	$V_{DD(RF)}$	enable transmitter
T_PWR	7	O	LOW	$V_{DD(RF)}$	switch transmitter power
GPP CLK100 VCO_BND_SW GP_CLK7 GP_CLK3 GP_CLK05 R_SLICED on/of	8	O	LOW	$V_{DD(RF)}$	general purpose pin used for the following: 100 Hz signal related to DECT frame timing VCO band switch 6.912 MHz general purpose clock 3.456 MHz general purpose clock 576 kHz general purpose clock ABS bitslice comparator output static high/low.
S_ENABLE	9	O	LOW	$V_{DD(RF)}$	synthesizer enable
S_DATA	10	O	LOW	$V_{DD(RF)}$	serial synthesizer data
S_CLK	11	O	LOW	$V_{DD(RF)}$	clock for serial synthesizer interface
S_PWR	12	O	LOW	$V_{DD(RF)}$	switch synthesizer power
R_ENABLE	13	O	HIGH	$V_{DD(RF)}$	enable receiver
R_PWR	14	O	HIGH	$V_{DD(RF)}$	switch receiver power
SLICE_CTR	15	O	LOW	$V_{DD(RF)}$	switch slicer time constant
$V_{DD(RF)}$	16	–	–	–	positive supply voltage for RF interface pins
$V_{SS(RF)}$	17	–	–	–	negative supply voltage for RF interface pins
REF_CLK	18	O	running	$V_{DD(RF)}$	programmable reference clock for synthesizer
RSSI_AN	19	I	–	$V_{DD(RF)}$	analog input for RSSI measurement
T_GMSK/T_DATA	20	O	off	$V_{DD(RF)}$	transmitter data output, filtered/digital
R_DATAP	21	I	–	$V_{DD(RF)}$	positive input for receiver data
R_DATAM	22	I	–	$V_{DD(RF)}$	negative input for receiver data
$V_{DD(OSC)}$	23	–	–	–	positive supply for crystal oscillator
XTAL2	24	O	running	$V_{DD(OSC)}$	crystal oscillator output
XTAL1	25	I	–	$V_{DD(OSC)}$	crystal oscillator input

SYMBOL	PIN	I/O	STATE AFTER RESET(1)	SUPPLY DOMAIN	DESCRIPTION
$V_{SS(OSC)}$	26	–	–	–	negative supply for crystal oscillator
$V_{DD(BAT)}$	27	I	–	–	positive battery supply voltage
VANLI	28	I/O	–	V_{DDA}	analog input to ADC, current output
VANLO	29	O	off	V_{DDA}	analog output from DAC
V_{DDA}	30	–	–	–	positive supply voltage for analog circuits
EARM	31	O	off	V_{DDA}	negative output to earpiece
EARP	32	O	off	V_{DDA}	positive output to earpiece
V_{SSA}	33	–	–	–	negative supply voltage for analog circuits
VBGP	34	O	1.2 V	$V_{DD(BAT)}$	bandgap output voltage (+1.2 V)
V_{ref}	35	O	off	V_{DDA}	reference voltage, microphone supply (+2 V)
MICM/LIFP	36	I	off	V_{DDA}	negative/positive input from microphone/line
MICP/LIFM	37	I	off	V_{DDA}	positive/negative input from microphone/line
$V_{DD(BZ)}$	38	–	–	–	positive supply voltage for buzzer
BZM	39	O	LOW	$V_{DD(BZ)}$	negative buzzer output
BZP	40	O	LOW	$V_{DD(BZ)}$	positive buzzer output
$V_{SS(BZ)}$	41	–	–	–	negative supply voltage for buzzer
P2.0	42	I/O	HIGH	$V_{DD(P0,P2)}$	bidirectional Port 3 pins (80C51)
P2.1	43	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.2	44	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.3	45	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.4	46	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.5	47	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.6	48	I/O	HIGH	$V_{DD(P0,P2)}$	
P2.7	49	I/O	HIGH	$V_{DD(P0,P2)}$	
A16	50	O	LOW	$V_{DD(P0,P2)}$	A16 address select
$V_{SS(P0,P2)}$	51	–	–	–	negative supply voltage
$V_{DD(P0,P2)}$	52	–	–	–	positive supply voltage for periphery pins
$\overline{PSEN}$	53	O	HIGH	$V_{DD(P0,P2)}$	program store enable (80C51), active LOW
ALE	54	O	HIGH	$V_{DD(P0,P2)}$	address latch enable (80C51)
P0.7	55	I/O	HIGH	$V_{DD(P0,P2)}$	bidirectional Port 0 pins (80C51)
P0.6	56	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.5	57	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.4	58	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.3	59	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.2	60	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.1	61	I/O	HIGH	$V_{DD(P0,P2)}$	
P0.0	62	I/O	HIGH	$V_{DD(P0,P2)}$	

SYMBOL	PIN	I/O	STATE AFTER RESET(1)	SUPPLY DOMAIN	DESCRIPTION
$\overline{EA}$	63	I	–	$V_{DD(P0,P2)}$	external access (80C51), active LOW
P3.7/$\overline{RD}$	64	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Read data, active LOW
P3.6/$\overline{WR}$	65	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Write data, active LOW
P3.5/T1	66	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Timer 1 input
P3.4/T0	67	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/Timer 0 input
P3.3/$\overline{INT1}$/IrDA	68	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 1/IrDA clock
P3.2/$\overline{INT0}$	69	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 0
P3.1/TXD	70	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/UART transmit data
P3.0/RXD	71	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/UART receive data
V_{SSD}	72	–	–	–	negative supply voltage for digital core
V_{DDD}	73	–	–	–	positive supply voltage for digital core
$V_{DD(P1,P3)}$	74	–	–	–	positive supply voltage for periphery pins
P1.7/INT9/SDA	75	I/O	off	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 9/I^2C-bus data
P1.6/INT8/SCL	76	I/O	off	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 8/I^2C-bus clock
P1.5/INT7/FS1	77	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 7/SPI Frame Sync
P1.4/INT6/DCK	78	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 6/SPI Data Clock
P1.3/INT5/DO	79	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 5/SPI Data Out
P1.2/INT4/DI	80	I/O	HIGH	$V_{DD(P1,P3)}$	80C51 port pin/external interrupt 4/SPI Data In

Note

1. In the ‘State After Reset’ column the following symbols are used:
   a) HIGH means active HIGH, for BUPxSW pin types this means weak pull-up
   b) LOW means active LOW
   c) ‘running’ means the clock signal is active
   d) ‘off’ means the high-impedance state.

6 FUNCTIONAL DESCRIPTION

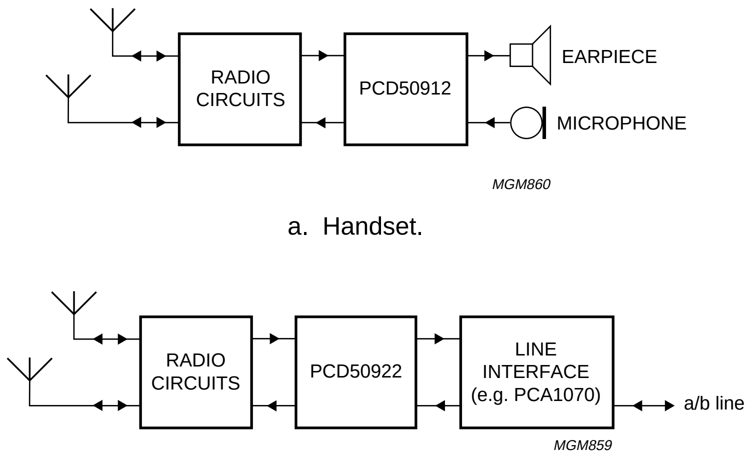
6.1 DECT baseband controller system

The PCD509x2 is a family of baseband controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimal component-count and minimal power consumption for very long standby times. All baseband controllers include an embedded 80C51 microcontroller with on-chip memory, including an IrDA (Infrared Data Association) compatible UART and I^{2}C-bus. The Burst Mode Logic performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The implemented RF Interface is compatible with the Philips Burst Mode Controller PCD504x. The ADPCM transcoding is in compliance with the CCITT Recommendation G.726. Also included is an on-chip codec with receive and transmit filters, complying with CCITT Recommendation G.712. Power-on-reset logic and power management functions further reduce power consumption and external components.

The chip is intended to support stand-alone systems only (see Fig.3). There are no provisions to build clusters of base stations. There are no provisions for external controllers to exert control over the embedded 80C51. There are no provisions for external controllers to have direct access to the on-chip data memories. There are no provisions to allow handsets to receive from two unsynchronised base stations simultaneously, but a handset can operate in a multi base station environment as long as they are synchronous base stations.

Refer to the block diagram in Fig.1. The DECT Controller consists of a number of functional blocks that operate more or less autonomously and communicate with each other via the System Data RAM (SDR). Blocks have access to SDR via the Internal System Bus (ISB). The ISB consists of an 8-bit data bus, a 10-bit address bus and a number of bus-request/bus-grant signals. Access to the ISB is controlled by ISB Bus Controller (IBC). The IBC acknowledges bus requests on the basis of a priority scheme. The embedded 80C51 controller is to be programmed by the user. It must contain DECT software from Man-Machine Interface (MMI) to the DECT protocols TBC, CBC and DBC (refer to *“Figures 10 to 13, in Section 6 of prETS 300 175-3: June* 1996”). Software is available from Philips Semiconductors.

Hardware state machines in the Burst Mode Logic (BML) and the Speech Interface (SPI) execute the lower blocks in the TBC, CBC and DBC. The 80C51 has control over the BML and the SPI via tables in SDR. The BML saves serial data, received via R_DATAP/M, in buffer areas in SDR. The position of the buffers in SDR is fixed by the 80C51 software by means of the tables previously mentioned. A-fields and B-fields are stored in separate buffers. In this way, two traffic bearers, each with their private A-fields, can share the same B-field buffer as is required in case of bearer hand-over or local call. The DSP and Codec support speech processing functions like analog-to-digital and digital-to-analog conversion, filtering, ADPCM encoding and decoding, 8-bit µ-law PCM to 14-bit linear PCM conversion and its reverse, echo cancelling, tone generation etc.



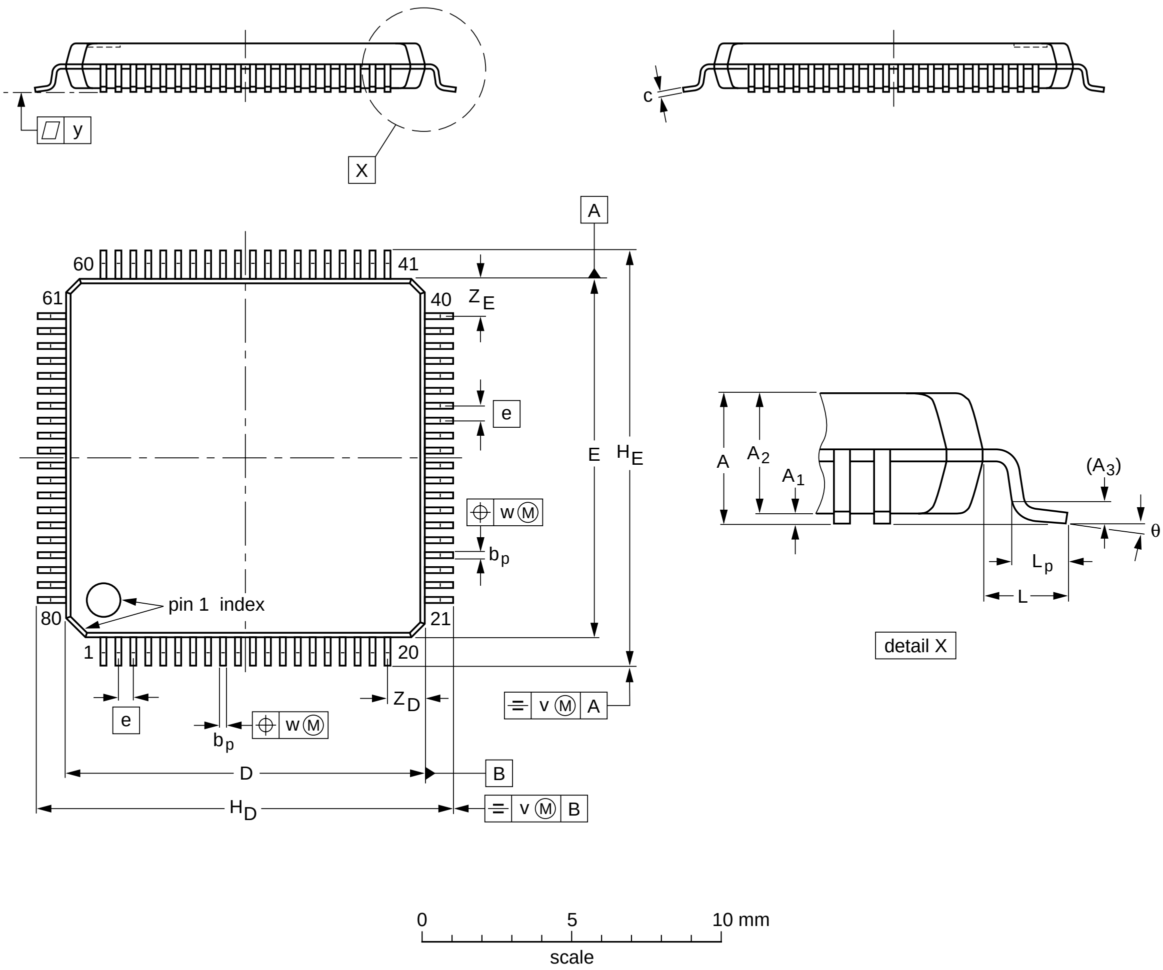
a. Handset.

b. Base station.

Fig.3 Block diagram examples of DECT systems with PCD509xy.

7 PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~95-12-19~~ 97-07-15

8 SOLDERING

8.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (order code 9398 652 90011).

8.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

8.3 Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

8.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

9 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

10 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

11 PURCHASE OF PHILIPS I^{2}C COMPONENTS

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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