FEATURES

- An embedded RISC controller (PCC) with 4 k byte (RAM/ROM) program memory for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning and the general control of the BMC hardware
- PP and FP modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control
- Switches up to 12 simultaneous active speech channels from speech interface to 1152 kbs radio interface, and vice versa
- RSSI measurement with on-chip peak/hold detector and 4-bit ADC
- Local call switching for up to 6 internal calls
- Quality control report
- Digital Phase-Locked Loop
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless hand over procedure
- Fast (hardware) and slow (software) mute function
- 1.5 k byte extended RAM memory for the handset
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Low power consumption in standby mode
- Low supply voltage (2.7 to 6 V)
- SACMOS technology.

Interfaces to:

- 1 ADPCM codec in the handset mode of operation
- Up to 2 ADPCM codecs in a simple base station (with up to 2 analog lines)
- 2048 kb/s highway interface for systems requiring more than 2 connections to the network
- Radio head
- 80C51-type microcontroller, or a 68000-type microcontroller
- Programmable synthesizer interface (8, 16, 24 bits).

GENERAL DESCRIPTION

The PCD5040/PCD5041 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT physical layer and Medium Access Control layer (MAC) time critical functions for application in DECT handset and base station products which comply with the following standards (plus updates):

- DECT CI part 2; physical layer (DE/RES 3001-2)
- DECT CI part 3; medium access control layer (DE/RES 3001-3)
- DECT CI part 7; security features for DECT (DE/RES 3001-7)
- DECT CI part 9; public access profile (DE/RES 3001-9).

The BMC is designed to be connected to an ADPCM codec (PCD5032) and an 8051-type microcontroller without glue logic. Other codecs and microcontrollers (e.g. 68000-family) are also supported. Two versions of the BMC will become available. The PCD5040 will have a RAM supported memory containing the BMC firmware, while the PCD5041 has a ROM instead. Both versions have the same pinning.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5040	QFP64	plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm	SOT208-1
PCD5041			

BLOCK DIAGRAM

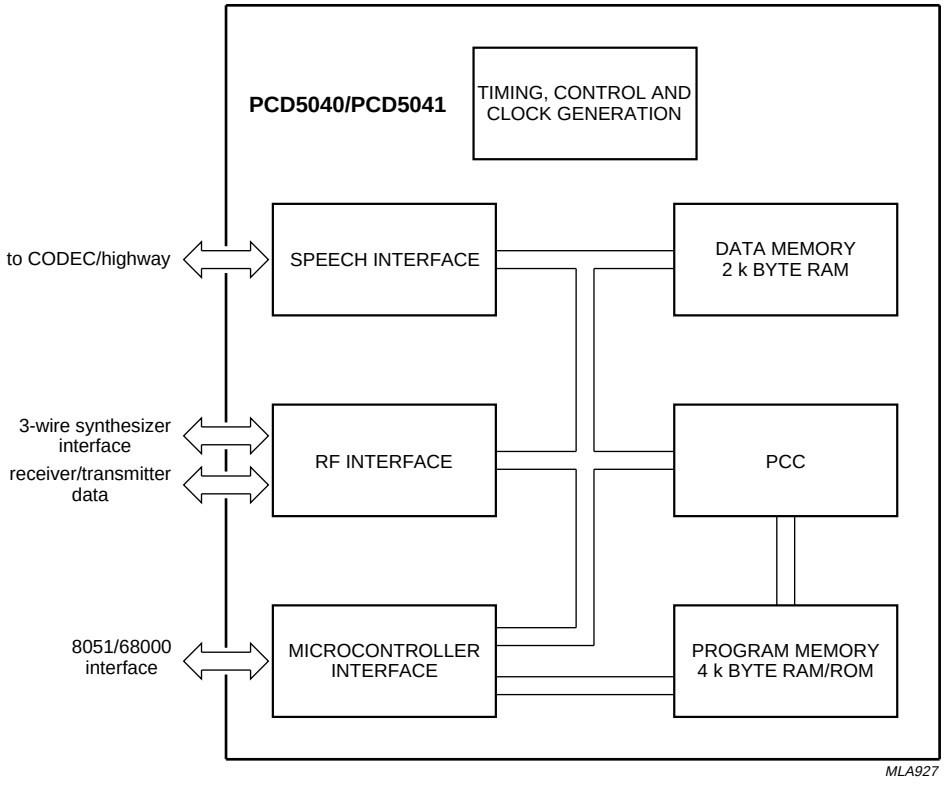

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AD0 to AD7	1 to 8	address/data bus input/output lines
ALE	9	address latch enable input
$\overline{CS}$	10	chip select input; active LOW
A10 to A8	11 to 13	address bus input lines
V_{DD}	14	positive supply voltage
PROC_CLK	15	microcontroller clock output; programmable from $f_{CLK/96}$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS}	16	negative supply voltage
XTAL1	17	crystal oscillator input
XTAL2	18	crystal oscillator output
V_{SS}	19	negative supply voltage
RESERVED	20	reserved
$\overline{RD}$	21	read input; active LOW
$\overline{WR}$	22	write input; active LOW
$\overline{RDY}$	23	ready signal output; active LOW, to initiate wait states in the microcontroller
$\overline{INT}$	24	interrupt output; active LOW
CLK100	25	100 Hz frame timer output
V_{SS}	26	negative supply voltage
DO	27	3-state data output on the speech interface
FS1	28	8 kHz framing signal output to ADPCM codec 1 for simple base plus handset, otherwise 8 kHz framing input
FS2	29	8 kHz framing signal output to ADPCM codec 2 in the base station mode
DI	30	data input on the speech interface
DCLK	31	1152 kHz data clock output for simple base plus handset, otherwise 2048 kHz data clock input signal
CLK3	32	3.456 MHz clock output; nominal value, used to adjust system timing
ANT_SW	33	switch output; selects one of two antennas
$\overline{T\_ENABLE}$	34	transmitter enable input; active LOW
T_POWER_RMP	35	transmitter power ramp control output
REM_STATUS	36	8-bit serial data input; can be read in for each s-lot
SYNTH_LOCK	37	lock indication input from synthesizer
V_{SS}	38	negative supply voltage
REF_CLK	39	reference frequency output for the synthesizer; i.e. the crystal oscillator clock f_{CLK}
V_{DD}	40	positive supply voltage
S_ENABLE	41	synthesizer enable output
S_CLK	42	clock signal output; to be used with S_DATA
S_DATA	43	serial data output to the synthesizer
S_POWER_DWN	44	synthesizer power down control output
VCO_BND_SW	45	VCO bandswitch control signal output

SYMBOL	PIN	DESCRIPTION
1200_Hz	46	control signal output for dual synthesizer schemes
T_DATA	47	serial data output to transmitter
TEST0	48	input to select test mode 0; normal operation set to logic 0
TEST1	49	input to select test mode 1; normal operation set to logic 0
RSSI_AN	50	analog input signal for basic DECT systems; peak signal strength measured after a low-pass filter
TEST2	51	input to select test mode 2; normal operation set to logic 0
TEST3	52	input to select test mode 3; normal operation set to logic 0
R_DATA	53	receive data input
$\overline{\text{R\_ENABLE}}$	54	receiver enable output; active LOW
R_POWER_DWN	55	receiver power down output
SLICE_CTR	56	slice time constant control output
V_{DD}	57	positive supply voltage
V_{SS}	58	negative supply voltage
V_{REF}	59	reference input for the ADC
V_{DD}_RAM	60	positive supply voltage for data RAM
SYNCPORT	61	this signal is the SYNCPORT input/output in the base station; it is an output in a master base station, input in a slave base station, in accordance with Annex C, DECT CI specification part 2. SYNCPORT is not active in the handset
M_RESET	62	BMC master reset input signal
MEM_SEL	63	input to select PCC program memory at the microcontroller interface
TEST4	64	input to select test mode 4; normal operation set to logic 0

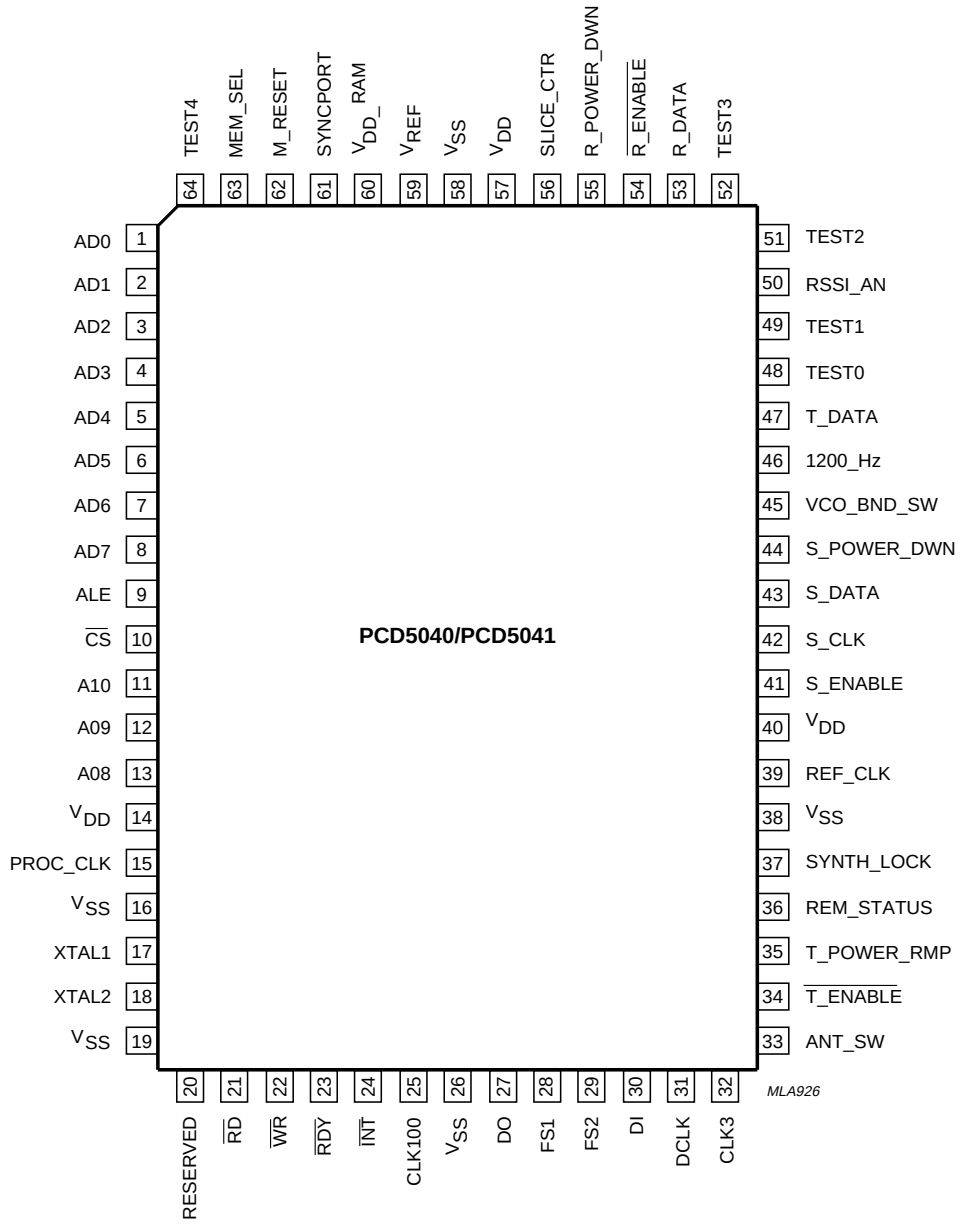

Fig.2 Pin configuration.