DATA SHEET

PCA9504A
Glue chip 4

Product specification
Supersedes data of 2000 Jul 25

2000 Aug 16

Philips
Semiconductors

PHILIPS

Glue chip 4 PCA9504A

FEATURES

- Dual, Strapping, Selectable Feature Sets
- Audio-disable Circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RMSRST# generation
- Voltage translation for DDC to VGA monitor
- HSYNCH / VSYNCH voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP Logic gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

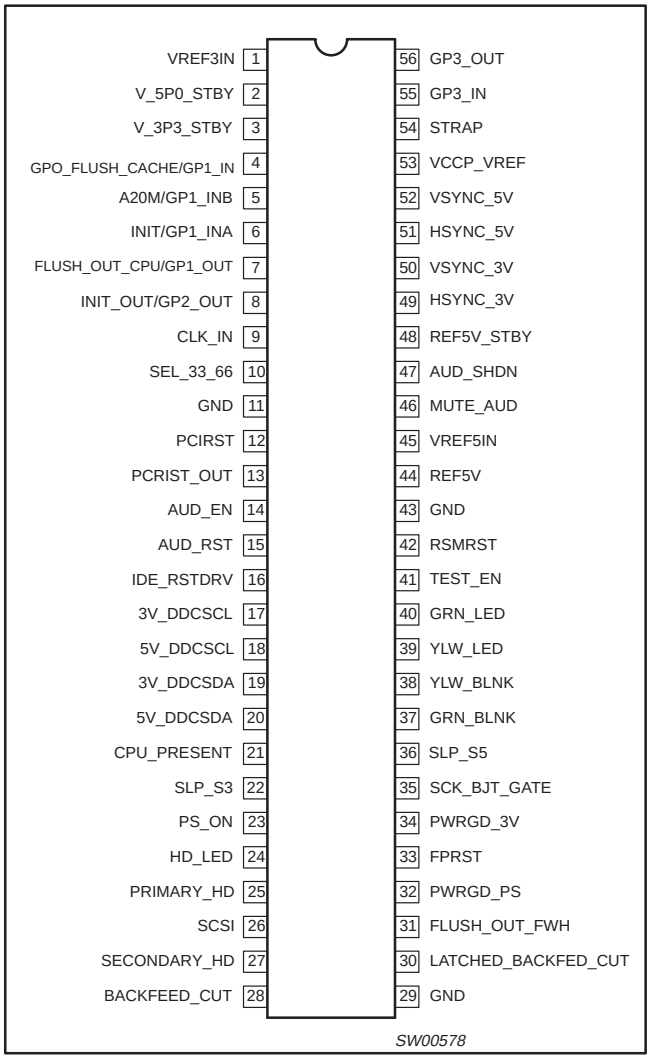
DESCRIPTION

The Glue 4 is a combinational part, integrating miscellaneous logic functions into a single chip.

The Glue 4 has two V_{CC} references (3 V and 5 V) and three Ground pins. There are two sets of I^2C interface pins (3 V and 5 V). The part has a Strap Selection pin used to select from FLUSH mode or General-Purpose mode.

Design optimized for the Intel 82801BA I/O controller hub (ICH2).

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic TSSOP	0°C to +70°C	PCA9504ADGG	SOT364-1

PIN DESCRIPTION

PIN(S)		SYMBOL	FUNCTION
1	3I	VREF3IN	3.3 V input
2	P	V_5P0_STBY	5 V system standby power supply
3	P	V_3P3_STBY	3 V system standby power supply
4	3IU	GPO_FLUSH_CACHE / GP2_IN	GPO from SIO / ICH2 / Buffer 2 input
5	REF	A20M / GP1_INB	A20M signal from ICH2 / NAND 1 input B
6	REF	INIT / GP1_INA	INIT signal from the ICH2 / Buffer 1 input A
7	5V OD	FLUSH_OUT_CPU / GP1_OUT	Open drain signal, goes to the CPU / NAND 1 output
8	5V OD	INIT_OUT / GP2_OUT	Delayed INIT signal into the CPU / Buffer 2 output
9	3I	CLK_IN	Either 33MHz or 66MHz clock, based on SEL_33_66 pin
10	3IU	SEL_33_66	Strapping option for 33MHz or 66MHz CLK_IN
11, 29, 43	G	GND	Ground
12	3I	PCRIST	PCI reset signal
13	3O	PCRIST_OUT	Copy of PCRIST, increased drive-strength
14	3IU	AUD_EN	Audio enable input (GPO from ICH2 / SIO)
15	3O	AUD_RST	Audio reset output
16	5O	IDE_RSTDRV	IDE reset output, 5 V push/pull
17	3IOD	3V_DDCSCL	DDCSCL input/output 3.3 V side
18	5IOD	5V_DDCSCL	DDCSCL input/output 5 V side
19	3IOD	3V_DDCSDA	DDCSDA input/output 3.3 V side
20	5IOD	5V_DDCSDA	DDCSDA input/output 5 V side
21	3IU	CPU_PRESENT	CPU present signal from the processor
22	3I	SLP_S3	Signal from ICH2 for transitioning to the S3 power state
23	5V OD	PS_ON	Power supply turn-on signal
24	5V OD	HD_LED	Hard drive front panel LED output
25	5IU	PRIMARY_HD	IDE primary drive active input
26	5IU	SCSI	SCSI drive active input
27	5IU	SECONDARY_HD	IDE secondary drive active input
28	5V OD	BACKFEED_CUT	Signal used for STR circuitry
30	5O	LATCHED_BACKFEED_CUT	Signal used for STR circuitry
31	5V OD	FLUSH_OUT_FWH	Open drain signal, goes to the FWH
32	5IU	PWRGD_PS	Power good signal from power supply
33	5IU	FPRST	Reset signal from the front panel
34	3O	PWRGD_3V	3.3 V power good output
35	5V OD	SCK_BJT_GATE	Gate signal from the SCK BJT in suspend to RAM
36	3I	SLP_S5	Signal from the ICH2 for transitioning to the S5 power state
37	3IU	GRN_BLNK	Power LED input, from SIO GPIO
38	3IU	YLW_BLNK	Power LED input, from SIO GPIO
39	5V OD	YLW_LED	Power LED output
40	5V OD	GRN_LED	Power LED output
41	5ID	TEST_EN	Test enable, 100K internal pull-down to GND
42	3O	RSMRST	Reset for the ICH2 resume well
44	AO	REF5V	Highest system supply reference voltage
45	5I	VREF5IN	5V system primary supply input
46	3IU	MUTE_AUD	Signal from SIO to mute audio on power up/down
47	5O	AUD_SHDN	Signal to audio amp to signal shutdown
48	AO	REF5V_STBY	Highest system standby voltage
49	3I	HSYNC_3V	HSYNCH input from chipset video

PIN DESCRIPTION CONTINUED

PIN(S)		SYMBOL	FUNCTION
50	3I	VSYNC_3V	VSYNCH input from chipset video
51	5O	HSYNC_5V	HSYNCH output to monitor
52	5O	VSYNC_5V	VSYNCH output to monitor
53	AI	V_{CCP}_VREF	Analog voltage reference for determining INIT/A20M input thresholds
54	3IV/3O	STRAP	Strapping option for GP or FLUSH mode
55	5I	GP3_IN	Generic logic gate 3 input
56	5V OD	GP3_OUT	Generic logic gate 3 output

TYPE	DESCRIPTION
3I	3.3 V input signal
3IU	3.3 V input signal with internal pull-up
5I	5 V input signal
5IU	5 V input signal with internal pull-up
5ID	5 V input signal with internal pull-down
P	Power (input)
G	Ground (input)
3O	3.3 V output signal
5O	5 V output signal
3V OD	3.3 V open-drain output signal
5V OD	5 v open-drain output signal
AO	Analog output
AI	Analog input
3IOD	3.3 V input/output open-drain
5IOD	5 V input/output open-drain
REFL	Input voltage levels referenced to V_{CCP}_VREF

FUNCTION TABLES

Strapping Selection Pin

STRAP (pin 54)	MODE[1]	PIN NAME & (PIN NUMBER)
0	FLUSH	GPO_FLUSH_CACHE (4)
0	FLUSH	A20M (5)
0	FLUSH	INIT (6)
0	FLUSH	FLUSH_OUT_CPU (7)
0	FLUSH	INIT_OUT (8)
1	GP	GP2_IN (4)
1	GP	GP1_INB (5)
1	GP	GP1_INA (6)
1	GP	GP1_OUT (7)
1	GP	GP2_OUT (8)

NOTE:

1. The pin is internally pulled up to default to FLUSH mode.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_5P0_STBY	DC 5.0V supply		–0.5	+6.0	V
V_3P3_STBY	DC 3.3V supply		–0.5	+6.0	V
$V_{I\ (5V)}$	DC input voltage (5 V pins)	Note 2	–0.5	V_5P0_STBY+0.5	V
$V_{O\ (5V)}$	Output voltage range (5 V pins)	Note 2	–0.5	V_5P0_STBY+0.5	V
$V_{I\ (3.3V)}$	DC input voltage (3.3 V pins)	Note 2	–0.5	V_3P3_STBY+0.5	V
$V_{O\ (3.3V)}$	Output voltage range (3.3 V pins)	Note 2	–0.5	V_3P3_STBY+0.5	V
SPD	Supply power dissipation			100	MW
ESD	Static Discharge voltage		2000		V
T_{STG}	Storage temperature range		–55	+150	°C
T_{OTR}	Operating Temperature Range		0	70	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under “recommended operating condition” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage rating may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3 V supply voltage		3.0	3.6	V
V_{DDL}	DC 2.5 V supply voltage		4.75	5.25	V
V_I	DC input voltage		0	V_{DD3}	V
V_O	DC output voltage		0	V_{DDL} V_{DD3}	V
T_A	Operating ambient temperature range in free air		0	+70	°C

DC CHARACTERISTICS

V_5P0_STBY = 5V ± 5%; V_3P3_STBY = 3.3V ± 10%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T_A = 0°C to +70°C			
			MIN	TYP	MAX	
STRAP						
V_{IH}	HIGH level input voltage		2.0			V
V_{IL}	LOW level input voltage				0.8	V
I_{IH}	Input leakage high		–1		1	µA
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –3 mA	2.4			V
I_{IL}	Input leakage low		–88		–26	µA
AUD_EN						
V_{IH}	HIGH level input voltage		2.0			V
V_{IL}	LOW level input voltage				0.8	V
I_{IL}	Input leakage high	V_{IL} = 0 V	–88		–26	µA
I_{IH}	Input leakage low		–1		1	µA
PCIRST						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_L	Input leakage		–1		1	µA
Hys	Input hysteresis		400			mV
MUTE_AUD						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_{IH}	Input leakage high		–1		1	µA
I_{IL}	Input leakage low	V_{IL} = 0 V	–88		–26	µA
VREF5IN						
V_{IH}	HIGH level input voltage		0.85*V5P 0_STBY			V
V_{IL}	LOW level input voltage				0.2*V5P 0_STBY	V
I_L	Input leakage		–1		1	µA
VREF3IN						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_L	Input leakage		–1		1	µA
PRIMARY_HD						
V_{IH}	HIGH level input voltage		0.7*5VSB			V
V_{IL}	LOW level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I_{IL}	Input leakage low	V_{IL} = 0 V	–88		–26	µA
I_{IH}	Input leakage high	V_{IH} = 5VSB	–1		1	µA
SECONDARY_HD						
V_{IH}	HIGH level input voltage		0.7*5VSB			V
V_{IL}	LOW level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I_{IL}	Input leakage low	V_{IL} = 0 V	–88		–26	µA

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T_A = 0°C to +70°C			
			MIN	TYP	MAX	
I_{IH}	Input leakage high	V_{IH} = 5VSB	–1		1	µA
SCSI						
V_{IH}	HIGH level input voltage		0.7*5VSB			V
V_{IL}	LOW level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I_{IL}	Input leakage low	V_{IL} = 0 V	–88		–26	µA
I_{IH}	Input leakage high	V_{IH} = 5VSB	–1		1	µA
FPRST						
V_{IH}	HIGH level input voltage		0.7*5VSB			V
V_{IL}	LOW level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I_{IL}	Input leakage low	V_{IL} = 0 V	–88		–26	µA
I_{IH}	Input leakage high	V_{IH} = 5VSB	–1		1	µA
PWRGD_PS						
V_{IH}	HIGH level input voltage		0.7*5VSB			V
V_{IL}	LOW level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I_{IL}	Input leakage low	V_{IL} = 0 V	–88		–26	µA
I_{IH}	Input leakage high	V_{IH} = 5VSB	–1		1	µA
GPO_FLUSH_CACHE/GP2_IN						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_L	Input leakage	V_{IL} = 0 V	–88		–26	µA
I_{IH}	Input leakage	V_{IH} = 5 V	–1		1	µA
INIT / GP1_INA (GP Mode)						
V_{IH}	HIGH level input voltage	Part is strapped for GP mode	2.4			V
V_{IL}	LOW level input voltage	Part is strapped for GP mode			0.8	V
I_L	Input leakage	Part is strapped for GP mode	–1		1	µA
VCCP_V_{ref}	Bias voltage	GP mode	1.95		2.1	V
INIT / GP1_INA (Flush Mode)						
V_{IH}	HIGH level input voltage	FLUSH mode	1.5			V
V_{IL}	LOW level input voltage	FLUSH mode			0.4	V
I_{IL}	Input leakage	FLUSH mode	–1		1	µA
VCCP_V_{ref}	Bias voltage	FLUSH mode	0.95		1.1	V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T_A = 0°C to +70°C			
			MIN	TYP	MAX	
A20M / GP1_INB						
V_{IH}	HIGH level input voltage	FLUSH mode	1.5			V
V_{IL}	LOW level input voltage	FLUSH mode			0.4	V
I_{IL}	Input leakage	FLUSH mode	–1		1	µA
VCCP_V_{ref}	Bias voltage	FLUSH mode	0.95		1.1	V
V_{IH}	HIGH level input voltage	GP mode	2.4			V
V_{IL}	LOW level input voltage	GP mode			0.8	V
I_L	Input leakage	GP mode	–1		1	µA
VCCP_V_{ref}	Bias voltage	GP mode	1.95		2.1	V
CLK_IN						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
Hys	Input hysteresis		250			mV
I_L	Input leakage		–1		1	µA
SEL_33_66						
V_{IH}	HIGH level input voltage		2.0			V
V_{IL}	LOW level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I_{IH}	Input leakage		–1		1	µA
I_{IL}	Input leakage	V_{IL} = 0 V	–88		–26	µA
SLP_S3						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I_L	Input leakage		–1		1	µA
SLP_S5						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I_L	Input leakage		–1		1	µA
CPU_PRESENT						
V_{IH}	HIGH level input voltage		2.0			V
V_{IL}	LOW level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I_{IH}	Input leakage	V_{IH} = 3VSB	–1		1	µA
I_{IL}	Input leakage	V_{IL} = 0 V	–88		–26	µA
TEST_EN						
V_{IH}	HIGH level input voltage		0.7*5VSB			V
V_{IL}	LOW level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I_{IH}	Input leakage	V_{IL} = 0 V	–1		1	µA
I_{IL}	Input leakage	V_{IH} = 5VSB	20		88	µA

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T_A = 0°C to +70°C			
			MIN	TYP	MAX	
HSYNC_3V						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_L	Input leakage		–1		1	µA
VSYNC_3V						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_L	Input leakage		–1		1	µA
GRN_BLNK						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_{IH}	Input leakage		–1		1	µA
I_{IL}	Input leakage	V_{IL} = 0 V	–88		–26	µA
YLW_BLNK						
V_{IH}	HIGH level input voltage		2.0			V
V_{IL}	LOW level input voltage				0.8	V
I_{IH}	Input leakage		–1		1	µA
I_{IL}	Input leakage	V_{IL} = 0 V	–88		–26	µA
GP3_IN						
V_{IH}	HIGH level input voltage		2.2			V
V_{IL}	LOW level input voltage				0.8	V
I_L	Input leakage		–1		1	µA
AUD_RST						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –3 mA	2.4			V
I_{OZ}	Off state output current		–1		1	µA
AUD_SHDN						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	2.4			V
I_{OZ}	Off state output current		–1		1	µA
REF5V						
V_{OUT5}	LOW level output voltage	V_{REF5in} > 1.5 V	V_{REF5in} – 0.05		V_{REF5in} + 0.05	V
V_{OUT3}	HIGH level output voltage	V_{REF3in} > 1.5 V	V_{REF3in} – 0.05		V_{REF3in} + 0.05	V
I_{OUTL}	Off state output current		–20		20	µA
REF5V_STBY						
V_{OUT5}	LOW level output voltage	V_5P0_STBY > 1.5 V	V_5P0_STBY – 0.05		V_5P0_STBY + 0.05	V
V_{OUT3}	HIGH level output voltage	V_5P0_STBY > 1.5 V	V_5P0_STBY – 0.05		V_5P0_STBY + 0.05	V
I_{OUTL}	Off state output current		–20		20	µA
HD_LED						
V_{OL}	LOW level output voltage	I_{OL} = 12 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T_A = 0°C to +70°C			
			MIN	TYP	MAX	
IDE_RSTDRV						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	2.4			V
I_{OZ}	Off state output current		–1		1	µA
PCIRST_OUT						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –3 mA	2.4			V
I_{OZ}	Off state output current		–1		1	µA
PRWGD_3V						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –3 mA	2.4			V
I_{OZ}	Off state output current		–1		1	µA
INIT_OUT / GP2_OUT						
V_{OL}	LOW level output voltage	I_{OL} = 12 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA
FLUSH_OUT_CPU / GP1_OUT						
V_{OL}	LOW level output voltage	I_{OL} = 12 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA
BACKFEED_CUT						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA
FLUSH_OUT_FWH						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA
LATCHED_BACKFEED_CUT						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	2.4			V
I_{OZ}	Off state output current		–1		1	µA
PS_ON						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA
RSMRST						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –3 mA	2.4			V
I_{OZ}	Off state output current		–1		1	µA
VTRIP	5VSB LOW trip voltage		1.8		3.5	V
SCK_BJT_GATE						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA

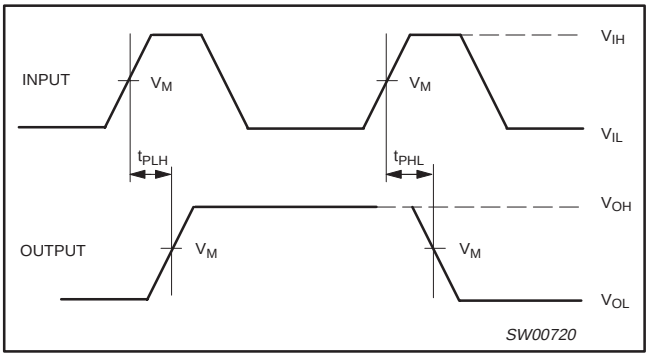
SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T_A = 0°C to +70°C			
			MIN	TYP	MAX	
3V_DDCSDA						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_H	Input leakage	5V_DDCSDA = V_{DD}	–1		2.5	µA
I_{OZ}	Off state output current		–1		1	µA
5V_DDCSDA						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_H	Input leakage	3V_DDCSDA = V_{DD}	–1		2.5	µA
I_{OZ}	Off state output current		–1		1	µA
3V_DDCSCL						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_H	Input leakage	5V_DDCSCL = V_{DD}	–1		2.5	µA
I_{OZ}	Off state output current		–1		1	µA
5V_DDCSCL						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
I_H	Input leakage	3V_DDCSCL = V_{DD}	–1		2.5	µA
I_{OZ}	Off state output current		–1		1	µA
HSYNC_5V						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	3.8			V
I_{OZ}	Off state output current		–1		1	µA
VSYNC_5V						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA			0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	3.8			V
I_{OZ}	Off state output current		–1		1	µA
GRN_LED / YLW_LED						
V_{OL}	LOW level output voltage	I_{OL} = 24 mA			0.4	V
I_{OZ}	Off state output current		–1		1	µA
GP3_OUT						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA				
I_{OZ}	Off state output current		–1		1	µA

AC CHARACTERISTICS

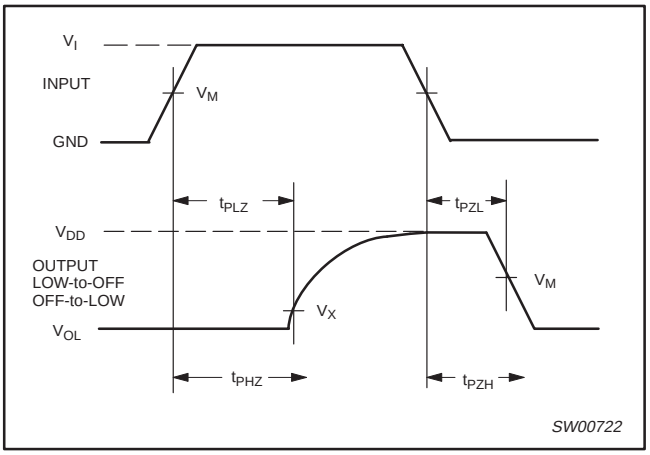
V_{CC1} = 3.3 V; V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	NOTES
		T_A = 0°C to +70°C				
		MIN	TYP	MAX		
t_{RESET}	RSMRST	4.0		100	ms	
t_{RESET_FALL}	RSMRST			100	ns	
t_{PHL}/t_{PLH}	Propagation Delay AUD_EN to AUD_RST PCIRST to AUD_RST PCIRST to IDE_RSTDRV PCIRST to PCIRST_OUT	1.0		11.0	ns	
t_{PLH}/t_{PHL}	Proparation Delay MUTE_AUD to MUTE_SHDN	2.5		6.0	ns	
t_{PLH}/t_{PHL}	Propagation Delay PWRGD_PS to PWRGD_3V FPRST to PWRGD_3V	4.5		11.0	ns	
t_{PLH}/t_{PHL}	Propagation Delay HSYNC_3V to HSYNC_5V VSYNC_3V to VSYNC_5V	2.0		5.0	ns	
t_{PLH}/t_{PHL}	Propagation Delay PWRGD_PS to SCK_BJT_GATE FPRST to SCK_BJT_GATE	1.0		6.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay PRIMARY_HD to HD_LED PRIMARY_HD to HD_LED PRIMARY_HD to HD_LED	1.0		5.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay GP1_INA to GP1_OUT GP2_INA to GP1_OUT	3.0		25.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay GP2_IN to GP2_OUT	3.0		7.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay GP3_IN to GP3_OUT	1.0		4.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay SLP_S3 to BACKFEED_OUT PRWGD_PS to BACKFEED_OUT	1.0		6.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay CPU_PRESENT to PS_ON	2.0		10.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay SLP_S3 to PS_ON	2.0		10.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay BACHFEED_OUT to LATCHED_BACKFEED_OUT	2.0		11.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay SLP_S5 to YLW_LED SLP_S5 to GRN_LED YLW_BLNK to YLW_LED GRN_BLNK to GRN_LED	1.0		5.0	ns	
t_{PLZ}/t_{PZL}	Open Drain Prop Delay 3V_DDOSDA to 5V_DDOSDA 3V_DDOSDA to 5V_DDOSDA	1.0		5.0	ns	
t_r, t_f	Rise and Fall Times HSYNC_5V VSYNC_5V	3.5			ns	
t_r, t_f	Rise and Fall Times LATCHED_BACKFEED_OUT			1.0	µs	

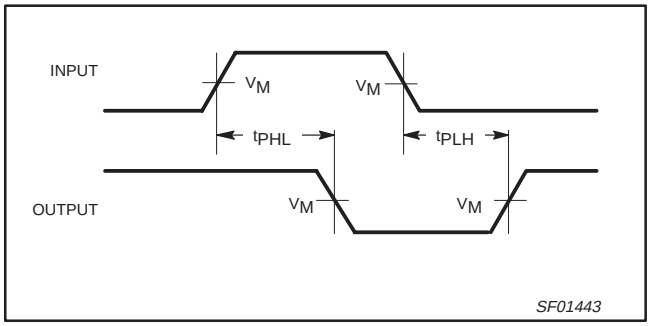
WAVEFORMS



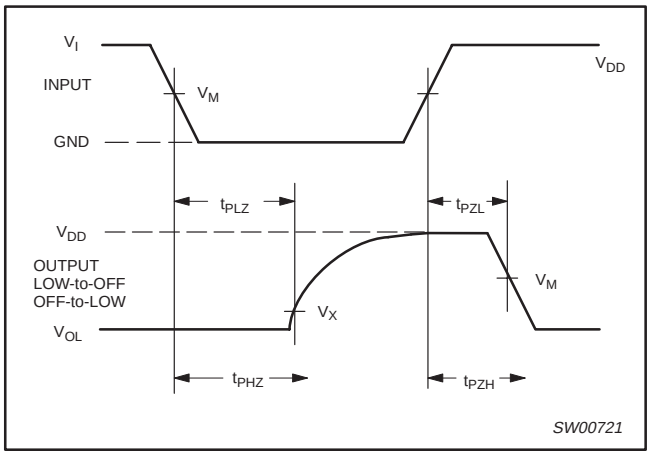
Waveform 1.



Waveform 2.



Waveform 3.



Waveform 4.

5V REFERENCE GENERATION

Supply	REF5V
VREF5IN < VREF3IN	VREF3IN
VREF5IN > VREF3IN	VREF5IN

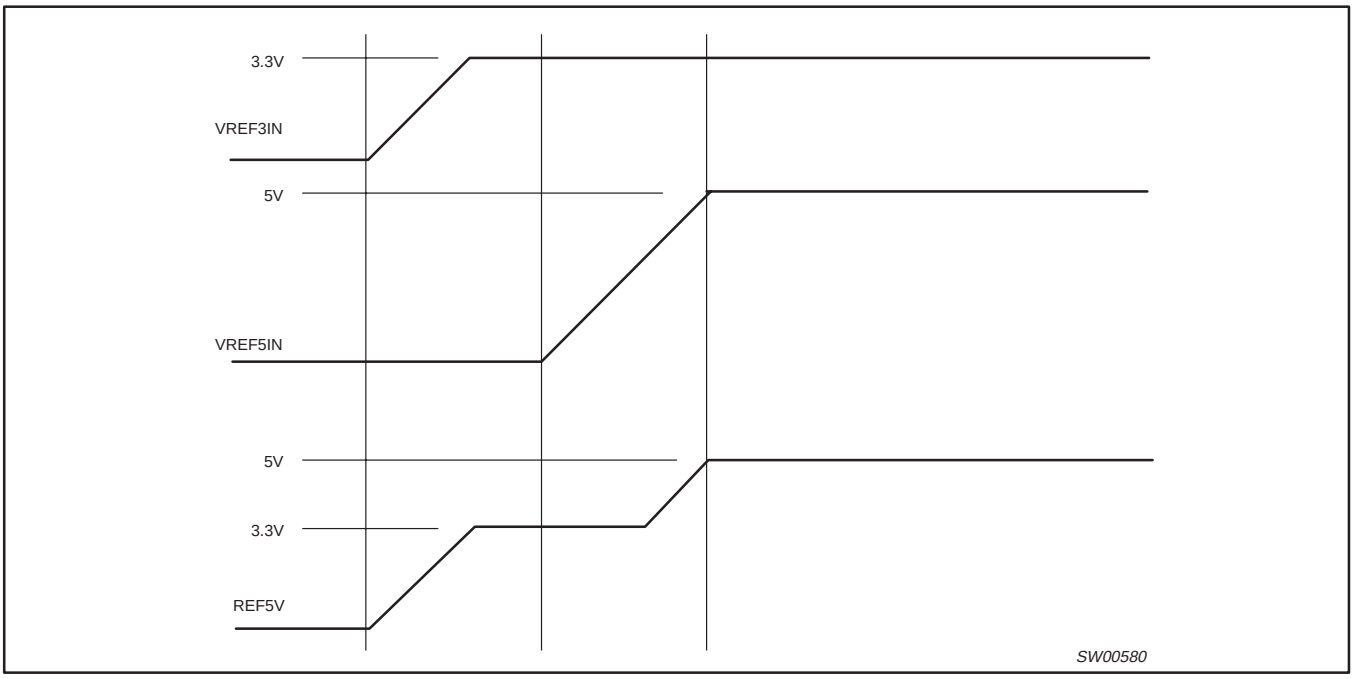


Figure 1. REF5V when VREF3IN ramps before VREF5IN

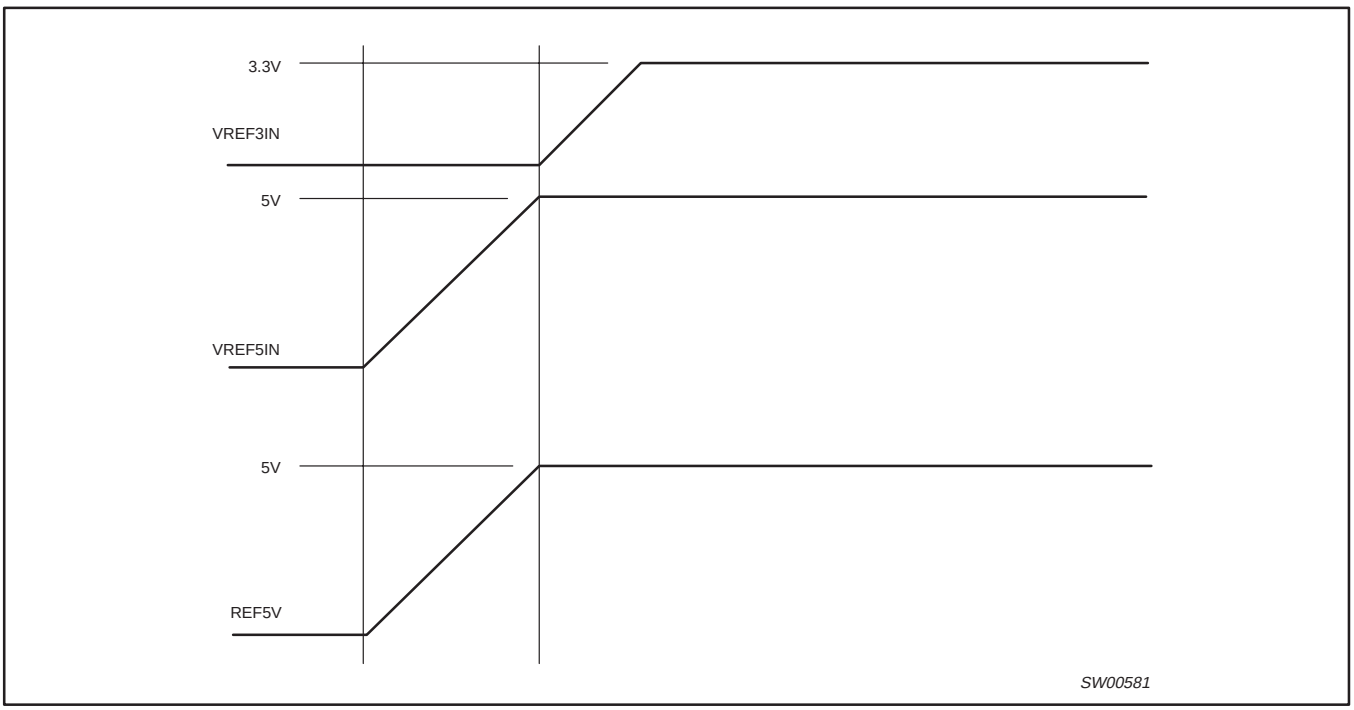


Figure 2. REF5V when VREF5IN ramps before VREF3IN

5V STANDBY REFERENCE GENERATION

Standby Supply	REF5V_STBY
V_5PO_STBY < V_3P3_STBY	V_3P3_STBY
V_5PO_STBY ÷ V_3P3_STBY	V_5PO_STBY

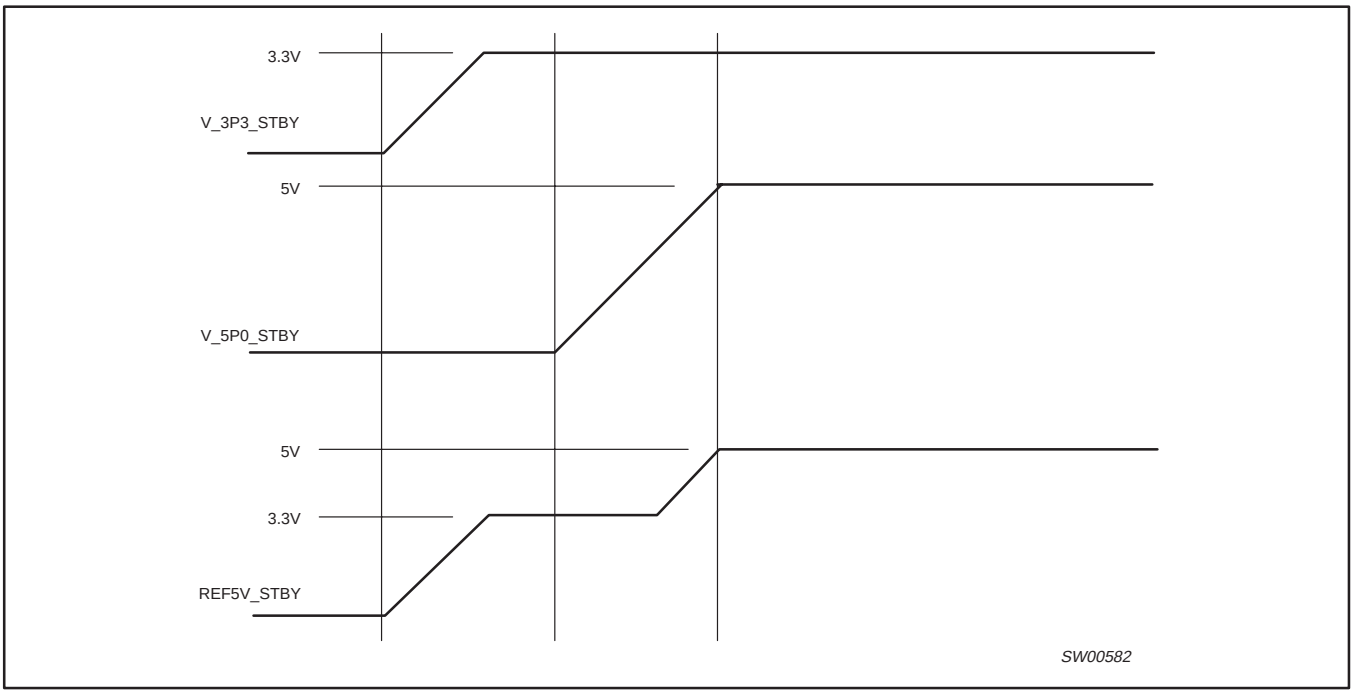


Figure 3. REF5V_STBY when V_3P3_STBY ramps before V_5PO_STBY

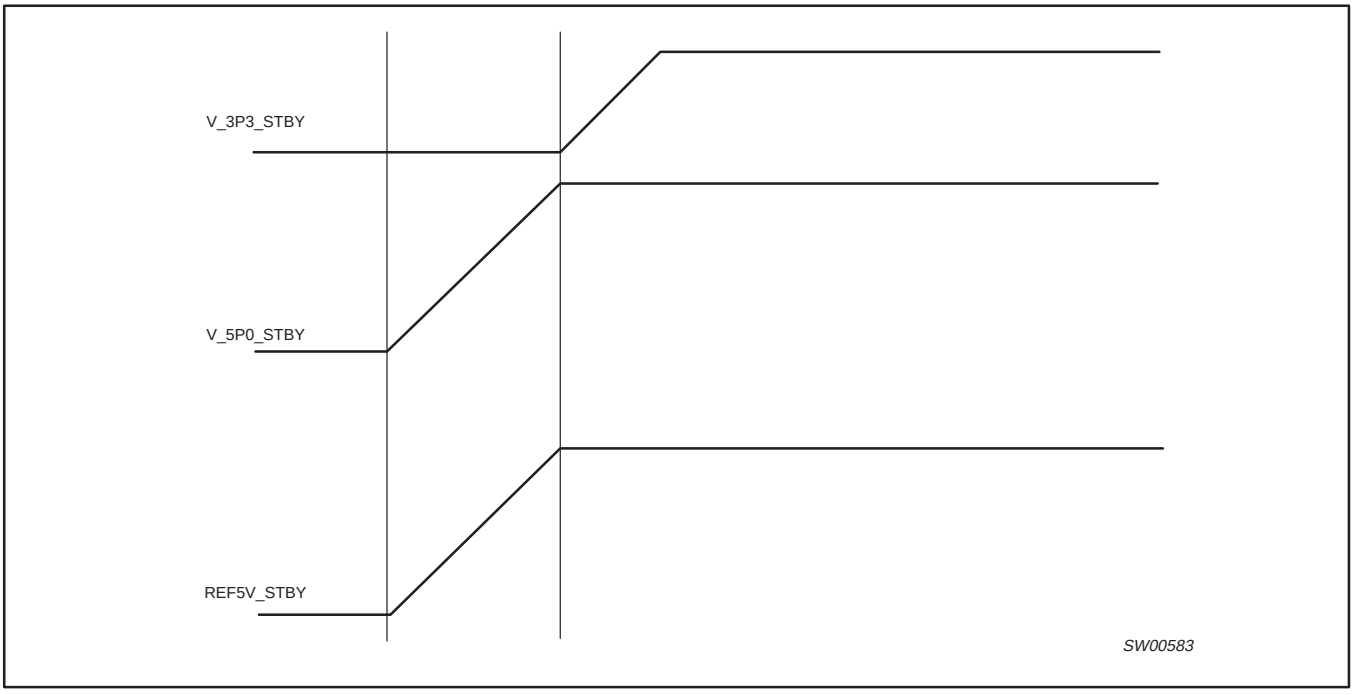


Figure 4. REF5V_STBY when V_5PO_STBY ramps before V_3P3_STBY

FLUSH OUT* / INIT OUT* CIRCUIT

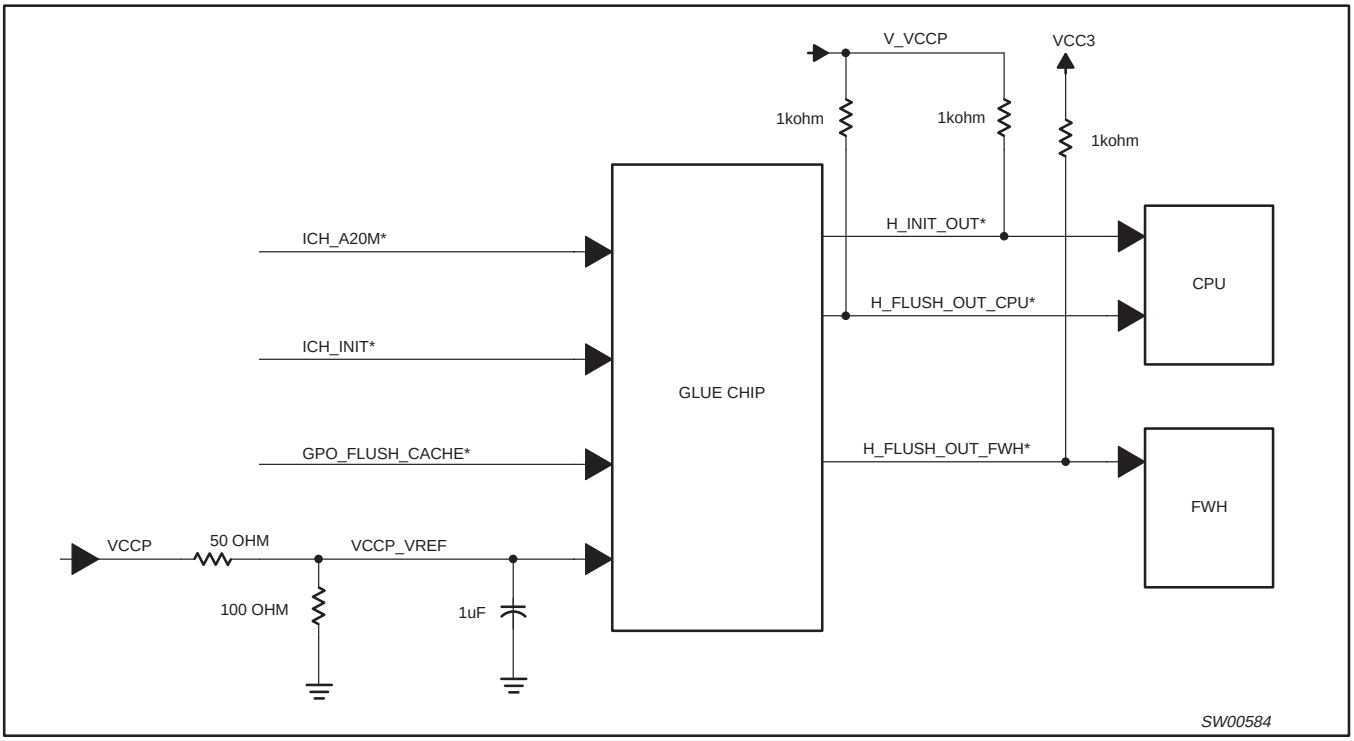


Figure 5. Block diagram for FLUSH_OUT*/INIT_OUT* circuit

Case	A20M*	GPO FLUSH CACHE*	INIT*	FLUSH OUT CPU*	FLUSH OUT FWH*	INIT OUT*
1	1	falling edge	0	0 (for t1)	0 (for t1)	0, Hi-Z, then 0 (delayed by t1-t, then active for 2*t)
2	1	falling edge	1	0 (for t1)	0 (for t1)	Hi-Z, 0 (delayed by t1-t, then active for 2*t)
3	X	1	0	Hi-Z	Hi-Z	0
4	X	1	1	Hi-Z	Hi-Z	Hi-Z
5	0	falling edge	1	Hi-Z	Hi-Z	Hi-Z
6	0	falling edge	0	Hi-Z	Hi-Z	0

NOTE:
1. Nominal value timings with tolerances are listed in the DC Characteristics table for t and t1. All Hi-Z outputs are shown as 1's or High in the following diagrams.

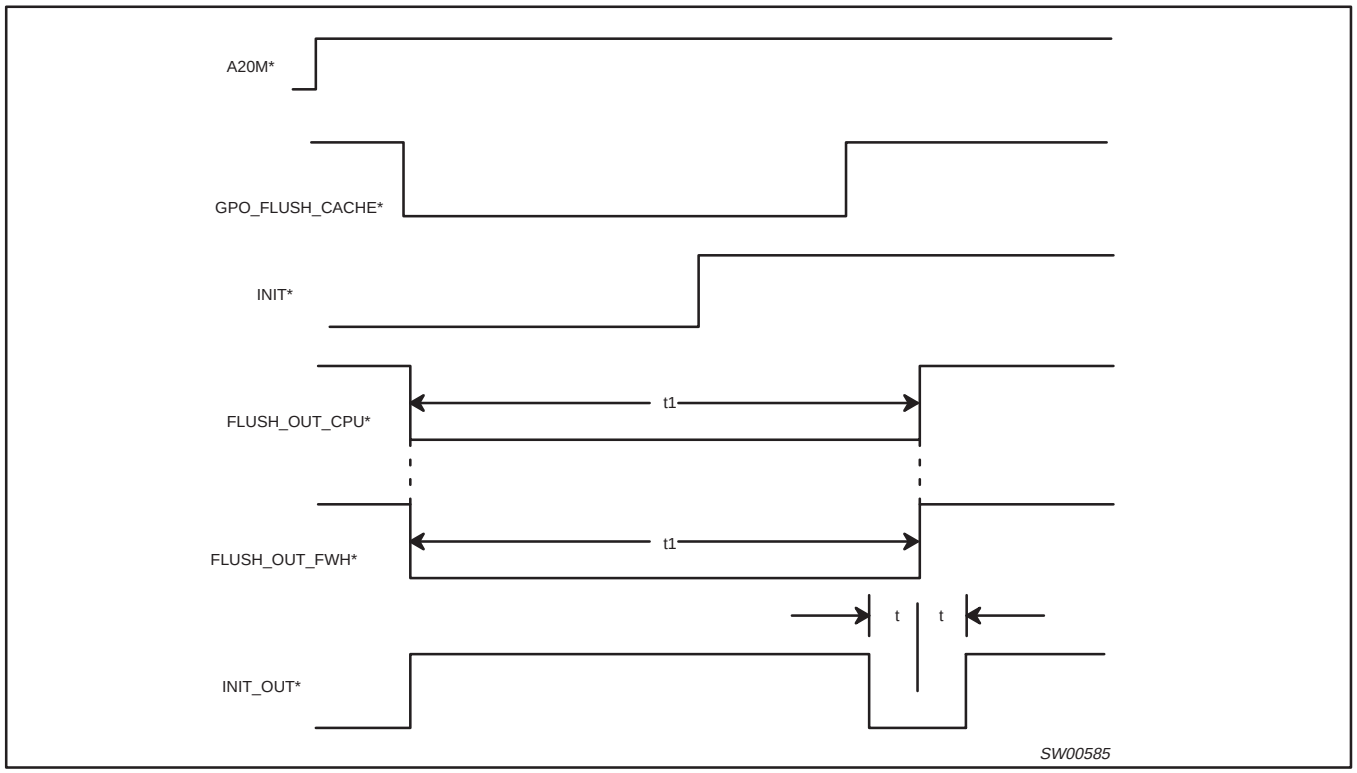


Figure 6. Waveforms for Case 1

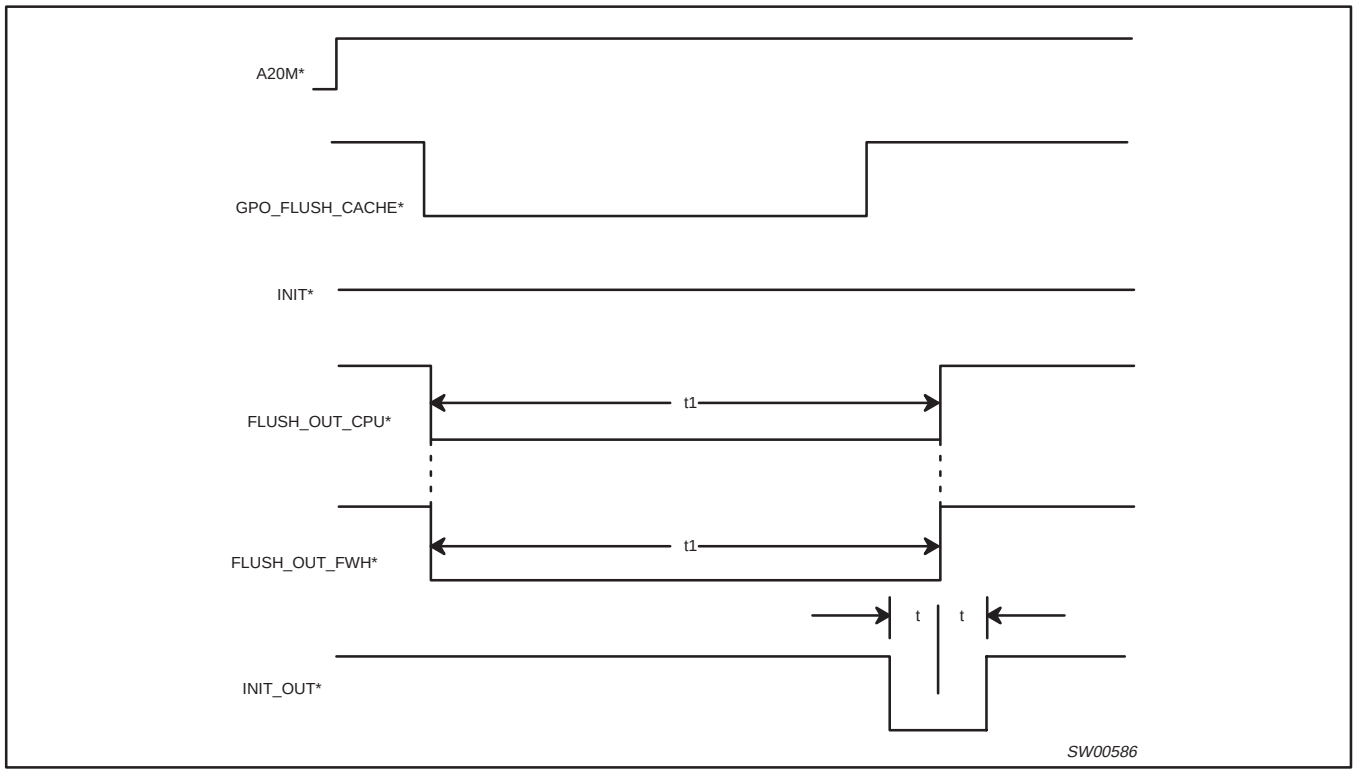


Figure 7. Waveforms for Case 2

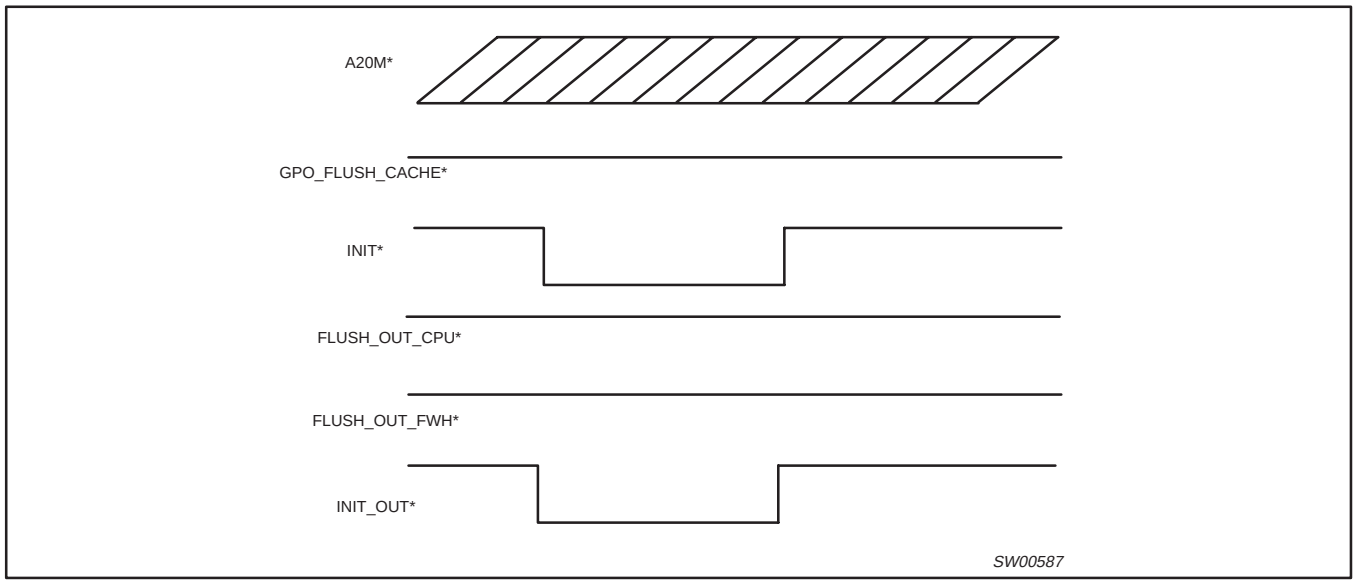


Figure 8. Waveforms for Case 3

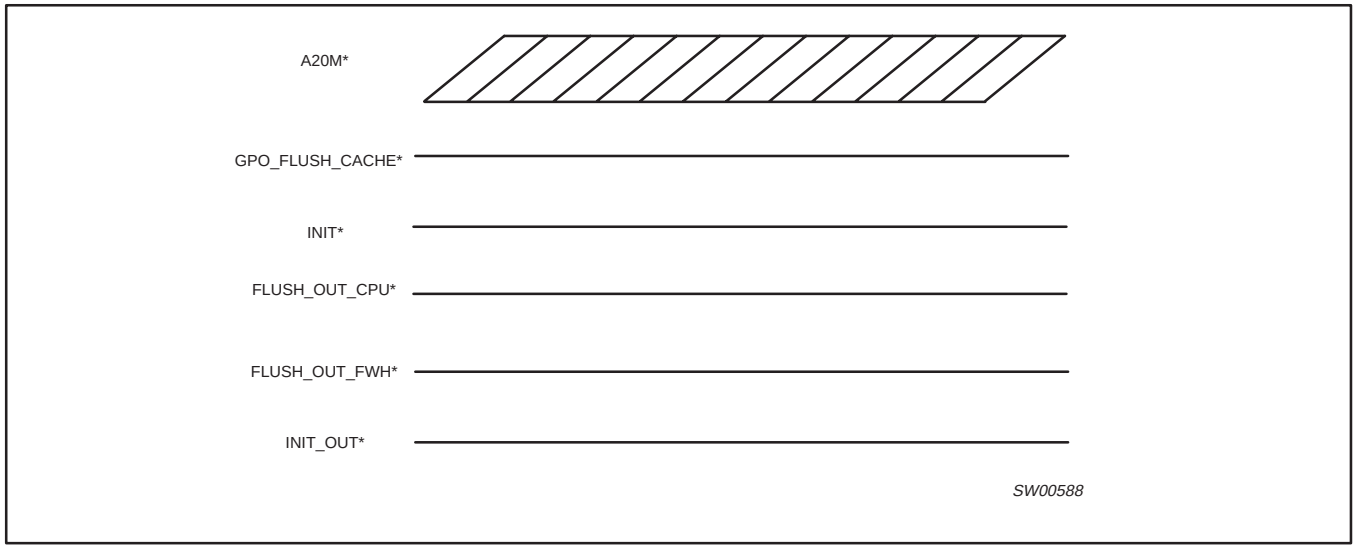


Figure 9. Waveforms for Case 4

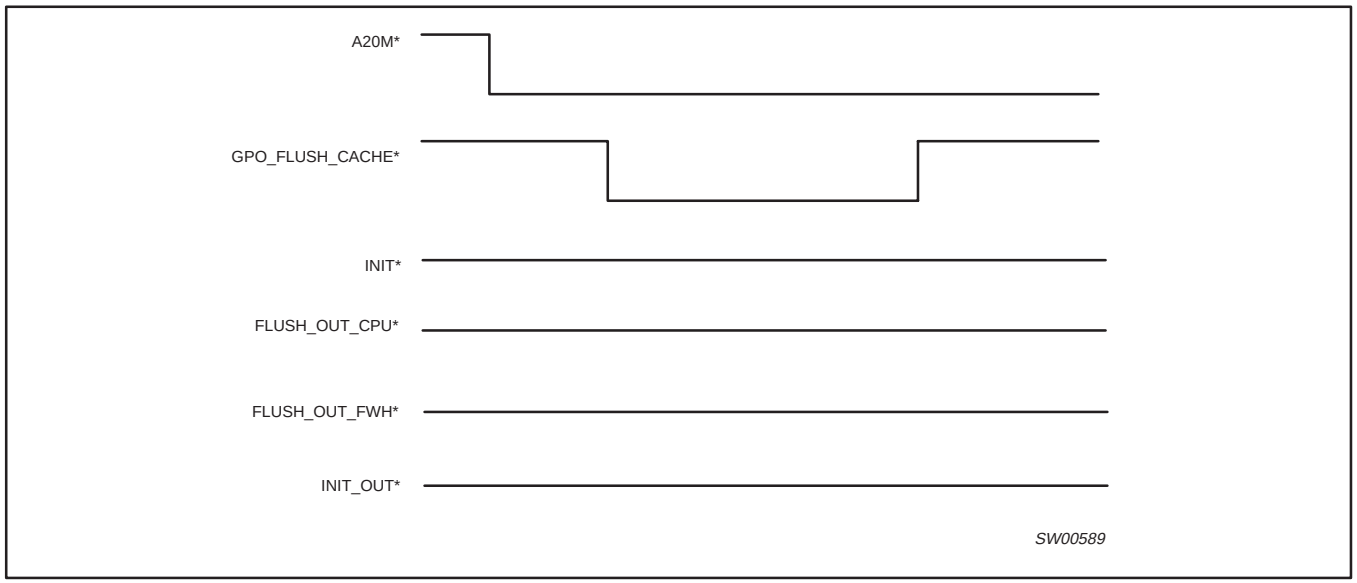


Figure 10. Waveforms for Case 5

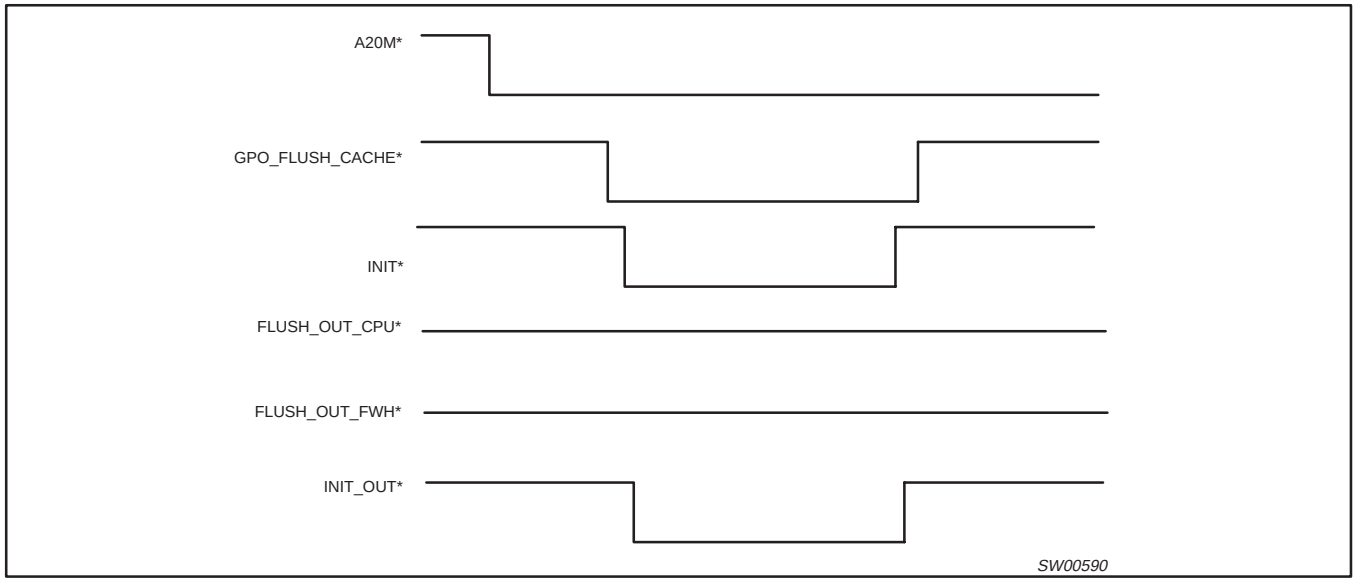


Figure 11. Waveforms for Case 6

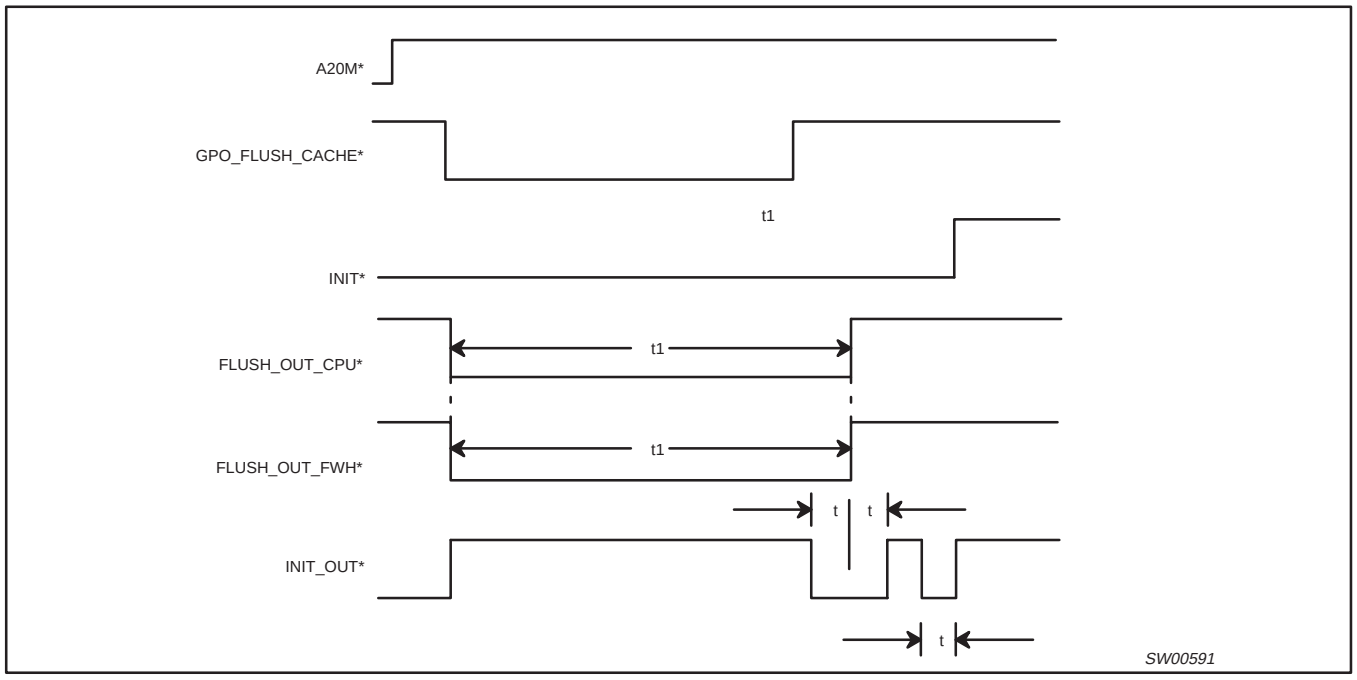


Figure 12. Waveforms for Case 7

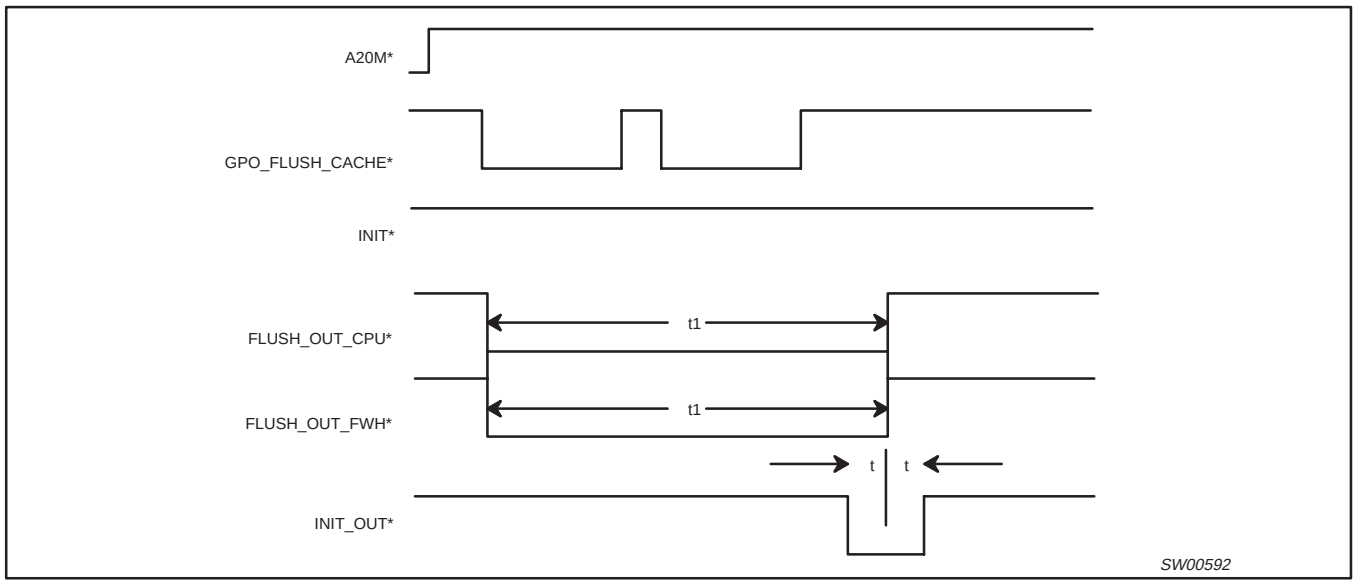


Figure 13. Waveforms for boundary GPO_FLUSH_CACHE* Case

- Timings should remain the same for both a 66 MHz or 33 MHz CLK_IN input.
- The boundary condition for INIT listed above, is a special case where immediately following the FLUSH_OUT*, INIT_OUT* cycle, the ICH2 asserts INIT* into the Glue Chip.
- The boundary condition for GPO_FLUSH_CACHE* listed above, is a special case where immediately following the first assertion of GPO_FLUSH_CACHE*, the GPO is de-asserted, then re-asserted again before the timings have had a chance to complete.

NOTE:

1. Nominal timing values with tolerances are listed in the DC Characteristics table.

GPO_FLUSH_CACHE* – input to logic, GPO from the ICH2, programmed active low.

INIT* – input to logic, INIT* signal from the ICH2.

A20M* – input to logic, A20M* signal from the ICH2.

FLUSH_OUT_CPU* – output of logic, route to CPU FLUSH* pin.

FLUSH_OUT_CPU* – output of logic, routed to FWH INIT* pin.

INIT_OUT* – output of logic, routed to CPU INIT* pin.

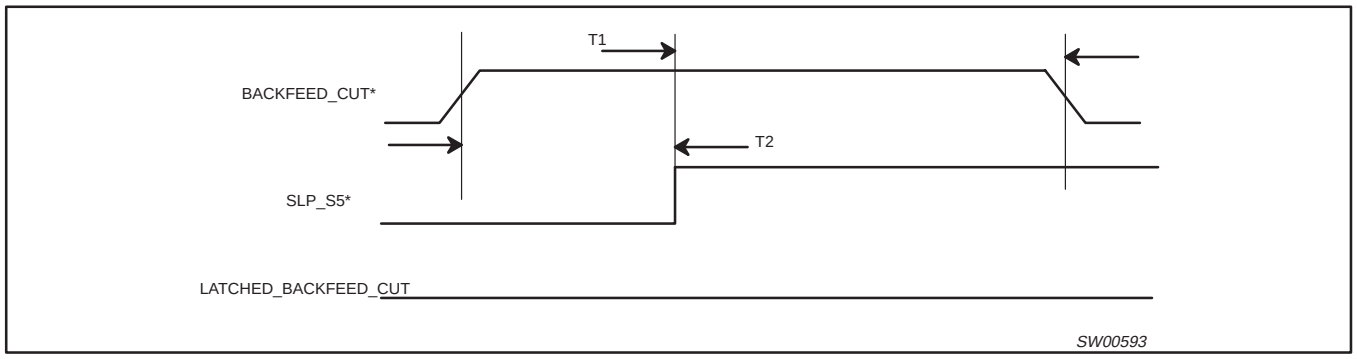


Figure 14. Power up signal sequencing

Power up signal sequencing is shown in Figure 14. BACKFEED_CUT* is following the power rail up to its final value. LATCHED_BACKFEED_CUT should stay low, never turning on. SLP_S5* goes to its high value when the power rails have stabilized, ~25 msec after power on. BACKFEED_CUT* is pulled low a period T1 after SLP_S5* goes high. T1 can be as short as 1msec. Typical measured values are ~200 msec. T1 and T2 are guaranteed by the inherent design of the system and are not controlled by Glue Chip.

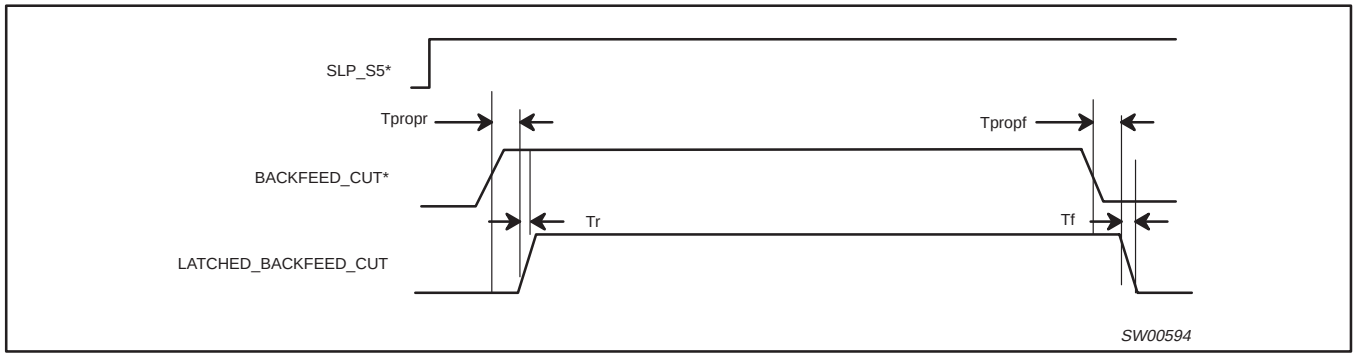


Figure 15. 1st sequence timing

The first possible sequence is with SLP_S5*staying HIGH and BACKFEED_CUT* transitioning from LOW to HIGH, remaining HIGH for an undetermined period and then going back to LOW and the system is back at the end of the power-up sequence. The power-up sequence is shown in Figure 15. During these BACKFEED_CUT* transitions, the propagation delays, rise and fall times, and going into regulation times LATCHED_BACKFEED_CUT are as described in Figure 16. The first sequence starts can start at the end of the power-up sequence at any time.

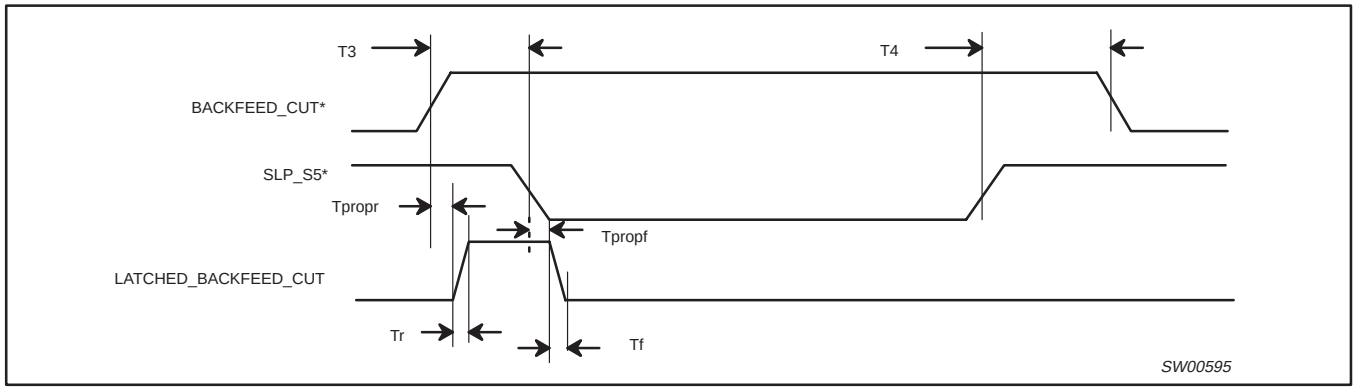


Figure 16. 2nd sequence timing

Signal sequencing for the second possible sequence is shown in Figure 16. BACKFEED_CUT* goes from LOW to HIGH and SLP_S5* goes from HIGH to LOW, 30 µsec to 65 µsec (T3) later. LATCHED_BACKFEED_CUT goes HIGH when BACKFEED_CUT* goes HIGH and then LATCHED_BACKFEED_CUT returns to LOW when SLP_S5* goes LOW. BACKFEED_CUT* stays HIGH and SLP_S5* stays low for an indeterminate time and then SLP_S5* will go HIGH. A minimum of 1msec (T4) later, BACKFEED_CUT* will go LOW and the system is back at the end of the power-up sequence. Typical measured values of T4 are ~250 msec. During all transitions, the propagation delays, rise and fall times, and going into regulation times for LATCHED_BACKFEED_CUT are as described in Figure 16. The first sequence starts can start at the end of the power-up sequence at any time.

RSMRST* GENERATION

RSMRST* is a delayed 3.3 V hysteresis copy of V_5PO_STBY. RSMRST* is delayed going inactive from the rising edge of V_5PO_STBY by 32 ms, nominal. This delay starts when V_5PO_STBY hits the trip point. There is minimal delay on the falling edge.

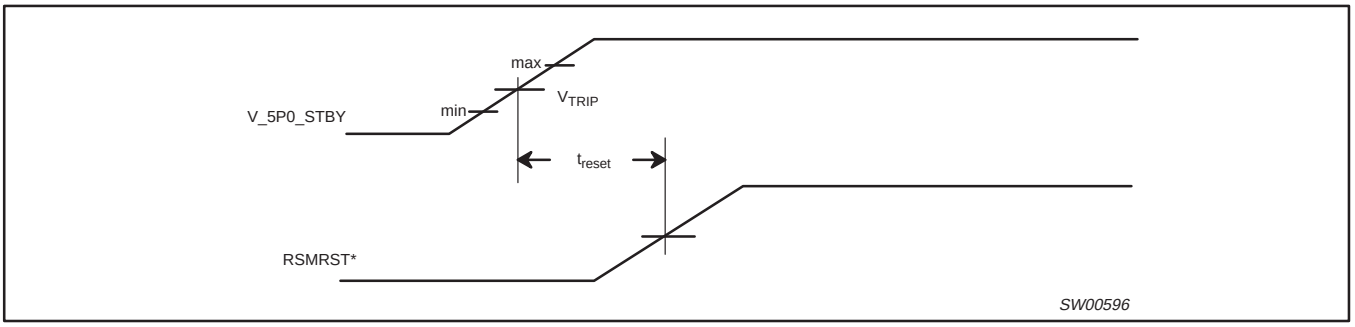


Figure 17. Resume reset functionality

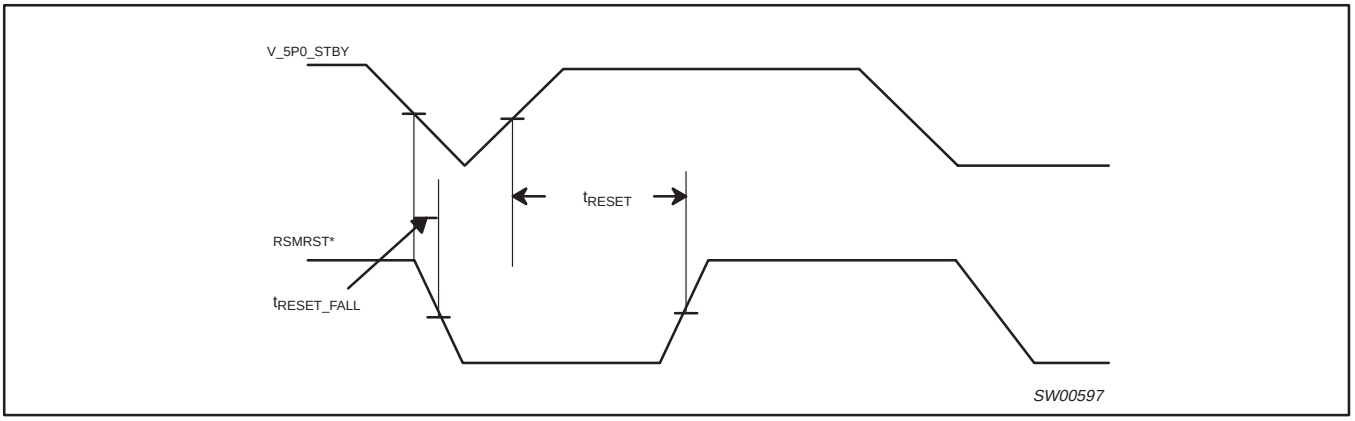


Figure 18. Resume reset functionality during brown out

AUDIO-DISABLE

AUD_EN	PCIRST		AUD_RST
0	0		0
0	1		0
0	0		0
0	1		1

MUTE AUDIO CIRCUIT

MUTE_AUD	AUD_SHDN
0	1
1	0

HD SINGLE COLOR LED DRIVER

PRIMARY_HD	SECONDARY_HD	SCSI	HD_LED
0	0	0	0
0	X	X	0
X	0	X	0
X	X	0	0
1	1	1	HI–Z

IDE RESET SIGNAL GENERATION AND PCRIST DRIVE STRENGTH

PCIRST	IDE_RSTDRV[1]	PCIRST_OUT
0	0	0
1	1	1

NOTE:
1. IDE_RSTDRV is a 5 V copy of PCIRST. PCIRST_OUT is a 3.3 V copy of PCIRST.

PWRGD SIGNAL GENERATION

FPRST	PWRGD_PS	PWRGD_3V
0	0	0
0	1	0
1	0	0
1	1	1

FLUSH_OUT / INIT_OUT CIRCUIT

CASE	A20M	GPO_FLUSH_CACHE	INIT	FLUSH_OUT_CPU	FLUSH_OUT_FWH	INIT_OUT
1	1	Falling edge	0	0(for t1)	0(for t1)	0, Hi-Z, then 0 (delayed by t1-t, then active for 2*t)
2	1	Falling edge	1	0(for t1)	0(for t1)	Hi-Z, 0 (delayed by t1-t, then active for 2*t)
3	X	1	0	Hi-Z	Hi-Z	0
4	X	1	1	Hi-Z	Hi-Z	Hi-Z
5	0	Falling edge	1	Hi-Z	Hi-Z	Hi-Z
6	0	Falling edge	0	Hi-Z	Hi-Z	0

CLK_IN AND SEL_33_66

SEL_33_66	CLK_IN RATE
0	66 MHz
1	33 MHz

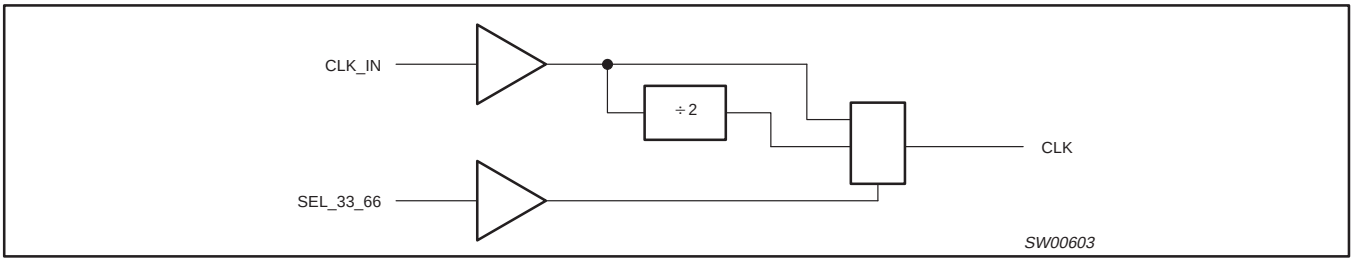


Figure 19.

GP_IN/GP_OUT GENERAL PURPOSE GATES

GP1_INA	GP1_INB	GP1_OUT
0	0	1
0	1	1
1	0	1
1	1	0

GP_IN/GP_OUT GENERAL PURPOSE GATES (continued)

GP2_IN	GP2_OUT
0	1
1	0

GP_IN/GP_OUT GENERAL PURPOSE GATES (continued)

GP3_IN	GP3_OUT
0	0
1	1

POWER SEQUENCING / BACKFEED_CUT

PWRGD_PS	SLP_S3	BACKFEED_CUT
0	0	HI-Z
0	1	HI-Z
1	0	HI-Z
1	1	0

POWER SUPPLY TURN-ON CIRCUIT

SLOTOCC	SLP_S3	SLP_S3A
0	0	Hi-Z
0	1	0
1	0	Hi-Z
1	1	Hi-Z

RAMBUS_SCK_BJT

PWRGD_3V	SCK_BJT_GATE
0	Hi-Z
1	0

VGA DCC VOLTAGE TRANSLATION

3V_DDCSDA	3V_DDCSCL	5V_DDCSDA	5V_DDCSCL
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

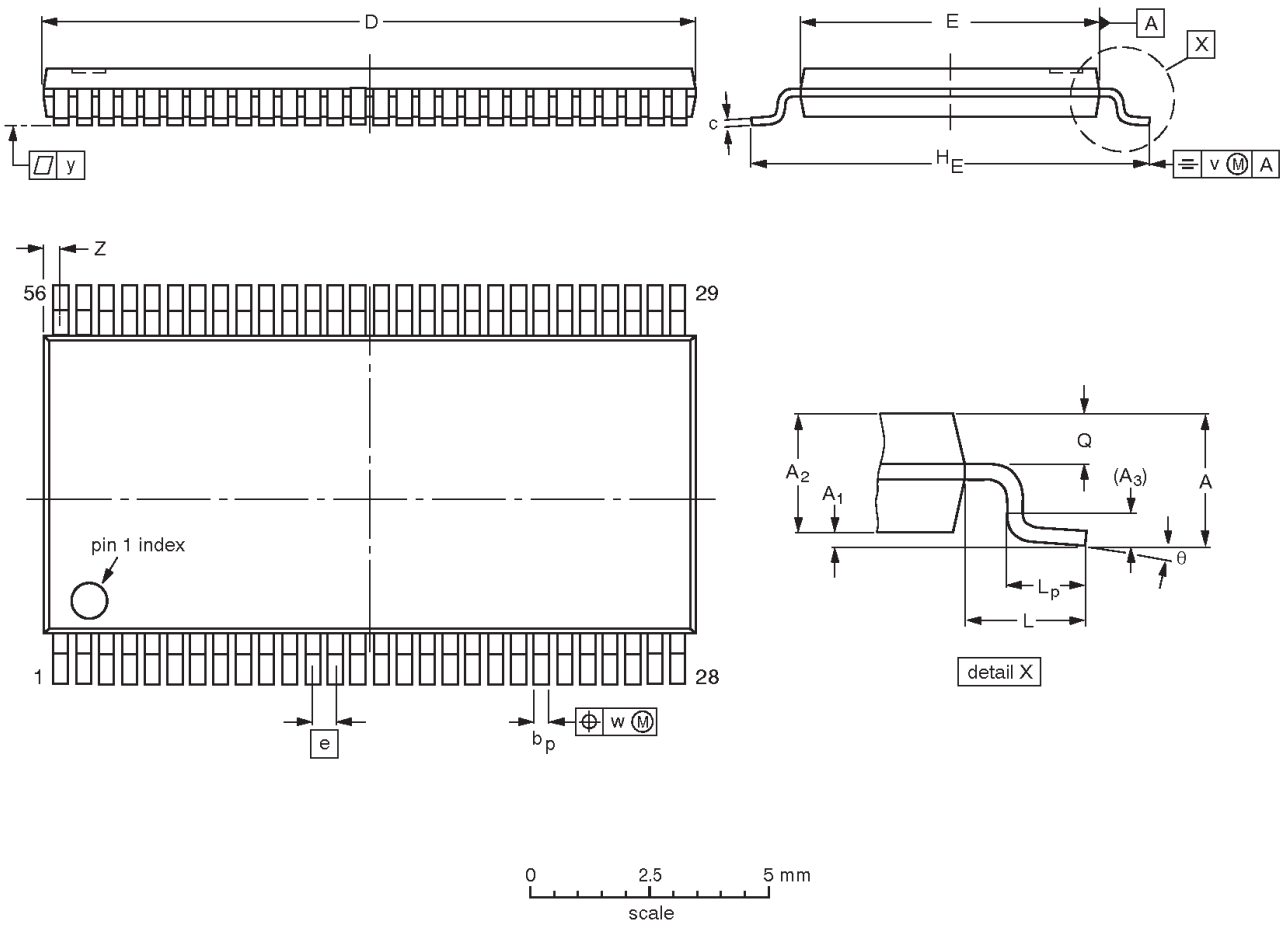
HSYNC / VSYNC VOLTAGE TRANSLATION

HSYNC_3V	HSYNC_5V	VSYNC_3V	VSYNC_5V
0	0	0	0
1	1	1	1

POWER LED DRIVER

YLW_BLNK	SLP_S5	YLW_LED	GRN_BLNK	SLP_S5	GRN_LED
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	HI-Z	1	1	Hi-Z

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153					~~95-02-10~~ 99-12-27

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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