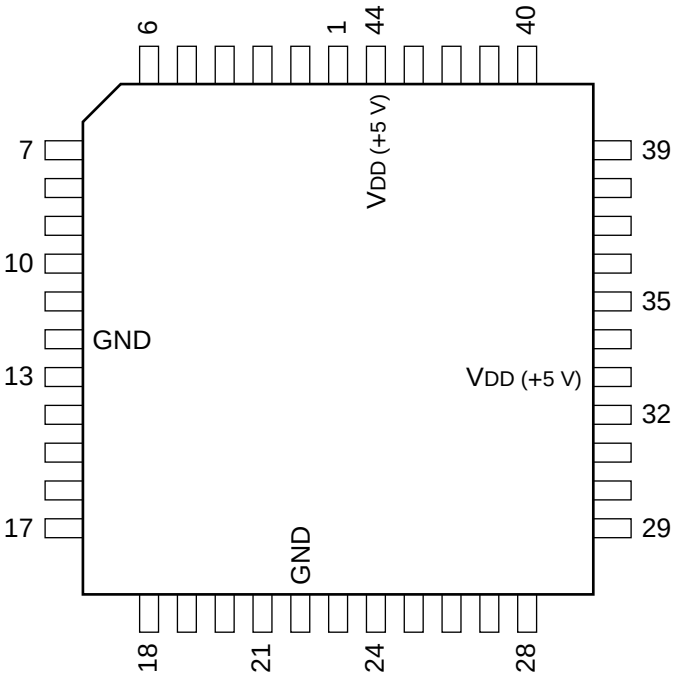
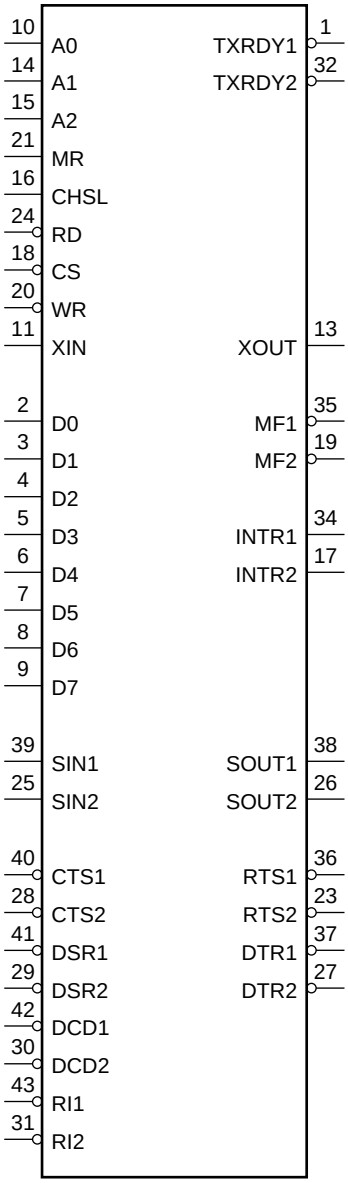
C-MOS ASYNCHRONOUS TRANSMITTER/RECEIVER WITH FIFO

—TOP VIEW—





(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	$\overline{\text{TXRDY1}}$	23	O	$\overline{\text{RTS2}}$
2	I/O	D0	24	I	$\overline{\text{RD}}$
3	I/O	D1	25	I	SIN2
4	I/O	D2	26	O	SOUT2
5	I/O	D3	27	O	$\overline{\text{DTR2}}$
6	I/O	D4	28	I	$\overline{\text{CTS2}}$
7	I/O	D5	29	I	$\overline{\text{DSR2}}$
8	I/O	D6	30	I	$\overline{\text{DCD2}}$
9	I/O	D7	31	I	$\overline{\text{RI2}}$
10	I	A0	32	O	$\overline{\text{TXRDY2}}$
11	I	XIN	33	—	V_{DD}
12	—	V_{SS}	34	O	INTR1
13	O	XOUT	35	O	$\overline{\text{MF1}}$
14	I	A1	36	O	$\overline{\text{RTS1}}$
15	I	A2	37	O	$\overline{\text{DTR1}}$
16	I	CHSL	38	O	SOUT1
17	O	INTR2	39	I	SIN1
18	I	$\overline{\text{CS}}$	40	I	$\overline{\text{CTS1}}$
19	O	$\overline{\text{MF2}}$	41	I	$\overline{\text{DSR1}}$
20	I	$\overline{\text{WR}}$	42	I	$\overline{\text{DCD1}}$
21	I	MR	43	I	$\overline{\text{RI1}}$
22	—	V_{SS}	44	—	V_{DD}

INPUT

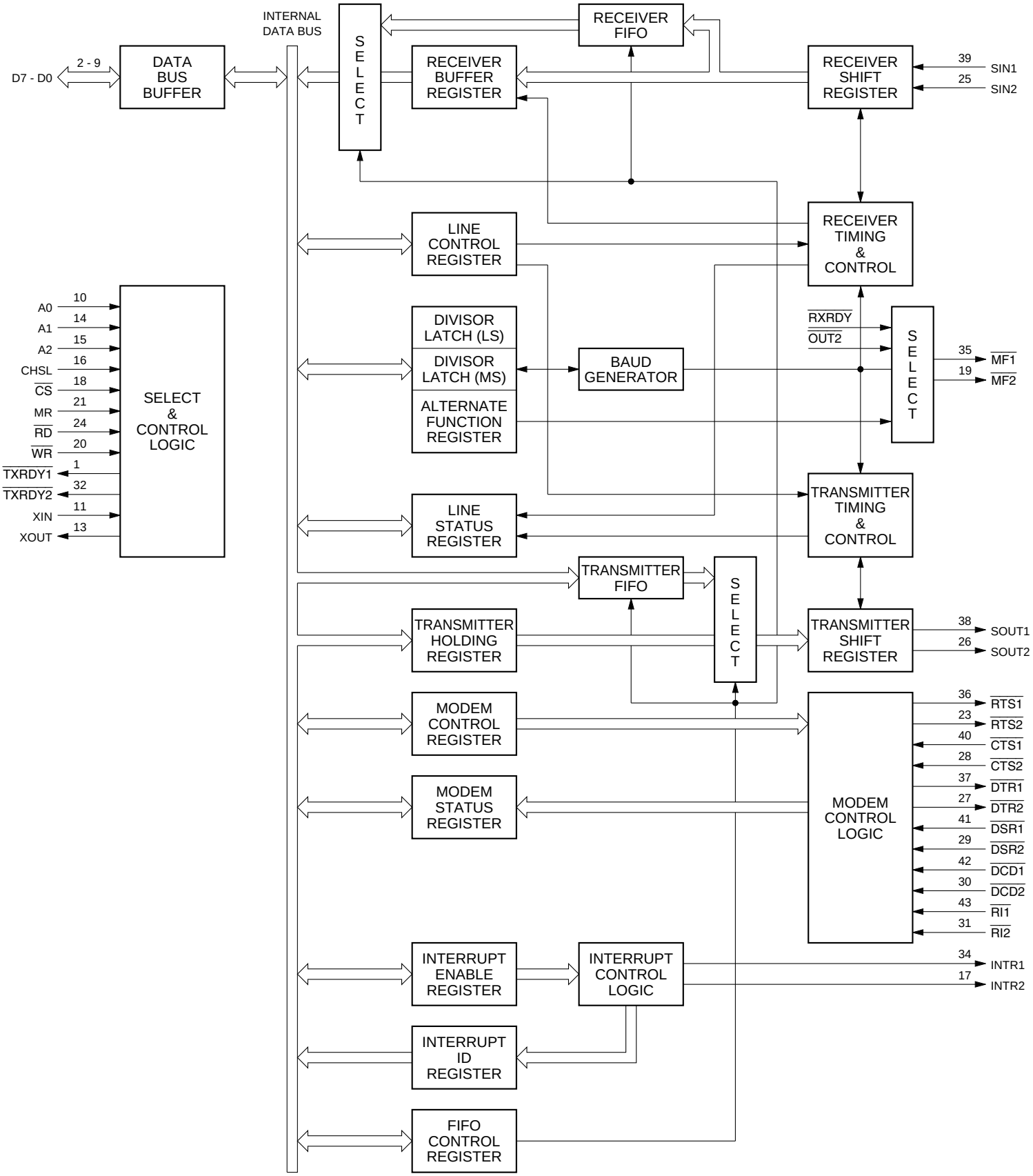
A0 - 2 : REGISTER ADDRESS DATA 0 - 2
CHSL : CHANNEL SELECT
$\overline{\text{CS}}$: CHIP SELECT
$\overline{\text{CTS1}}$, $\overline{2}$: CLEAR TO SEND 1, 2
$\overline{\text{DCD1}}$, $\overline{2}$: DATA CARRIER DETECT 1, 2
$\overline{\text{DSR1}}$, $\overline{2}$: DATA SET READY 1, 2
MR : MASTER RESET
$\overline{\text{RD}}$: READ
$\overline{\text{RI1}}$, $\overline{2}$: RING INDICATOR 1, 2
SIN1, 2 : SERIAL DATA
$\overline{\text{WR}}$: WRITE
XIN : EXTERNAL CRYSTAL

OUTPUT

$\overline{\text{DTR1}}$, $\overline{2}$: DATA TERMINAL READY 1, 2
INTR1, 2 : INTERRUPT 1, 2
$\overline{\text{MF1}}$, $\overline{2}$: MULTI-FUNCTION 1, 2
$\overline{\text{RTS1}}$, $\overline{2}$: REQUEST TO SEND 1, 2
SOUT1, 2 : SERIAL DATA 1, 2
$\overline{\text{TXRDY1}}$, $\overline{2}$: TRANSMITTER READY 1, 2
XOUT : EXTERNAL CRYSTAL

INPUT/OUTPUT

D0 - D7 : DATA BUS 0 - 7


INTERNAL
DATA BUS
D7 - D0
2 - 9
DATA
BUS
BUFFER
SELECT
RECEIVER
FIFO
RECEIVER
BUFFER
REGISTER
RECEIVER
SHIFT
REGISTER
39
SIN1
25
SIN2
LINE
CONTROL
REGISTER
RECEIVER
TIMING
&
CONTROL
A0
A1
A2
CHSL
CS
MR
RD
WR
TXRDY1
TXRDY2
XIN
XOUT
10
14
15
16
18
21
24
20
1
32
11
13
SELECT
&
CONTROL
LOGIC
DIVISOR
LATCH (LS)
DIVISOR
LATCH (MS)
ALTERNATE
FUNCTION
REGISTER
BAUD
GENERATOR
RXRDY
OUT2
SELECT
35
MF1
19
MF2
LINE
STATUS
REGISTER
TRANSMITTER
TIMING
&
CONTROL
TRANSMITTER
FIFO
SELECT
TRANSMITTER
HOLDING
REGISTER
TRANSMITTER
SHIFT
REGISTER
38
SOUT1
26
SOUT2
MODEM
CONTROL
REGISTER
MODEM
CONTROL
LOGIC
36
RTS1
23
RTS2
40
CTS1
28
CTS2
37
DTR1
27
DTR2
41
DSR1
29
DSR2
42
DCD1
30
DCD2
43
RI1
31
RI2
MODEM
STATUS
REGISTER
INTERRUPT
ENABLE
REGISTER
INTERRUPT
CONTROL
LOGIC
34
INTR1
17
INTR2
INTERRUPT
ID
REGISTER
FIFO
CONTROL
REGISTER