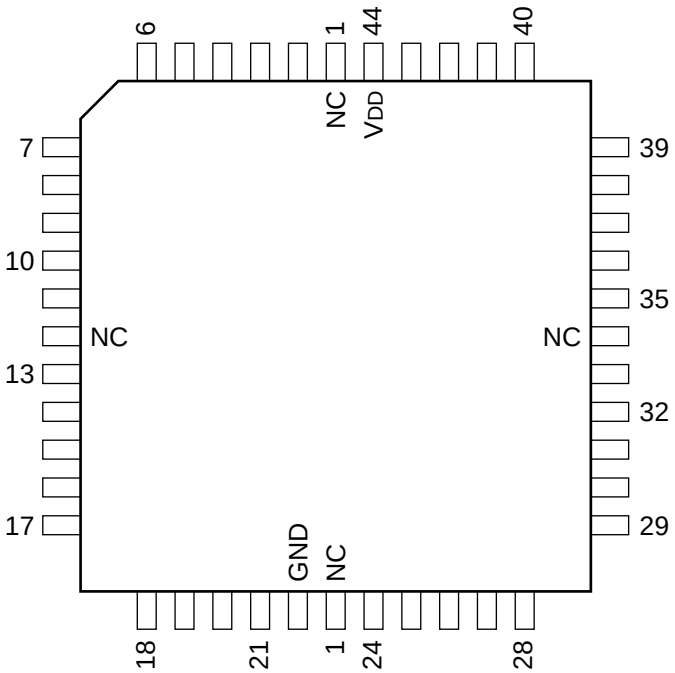
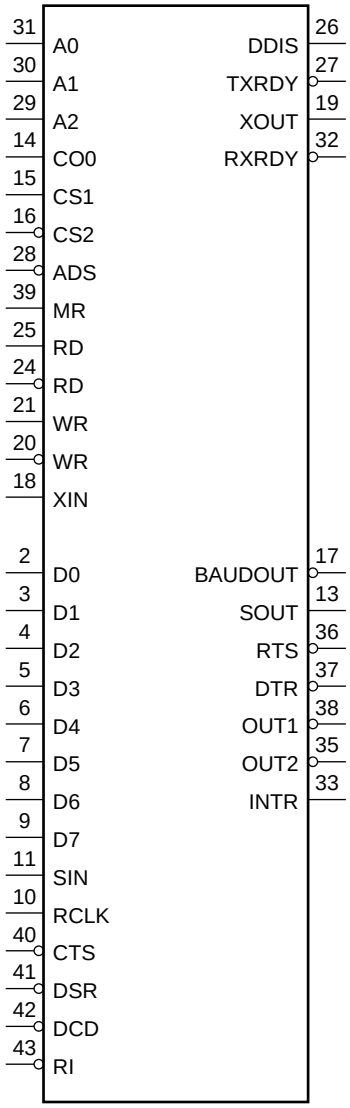
C-MOS UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO

—TOP VIEW—





PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	NC	12	—	NC	23	—	NC	34	—	NC
2	I/O	D0	13	O	SOUT	24	I	$\overline{RD}$	35	O	$\overline{OUT2}$
3	I/O	D1	14	I	CS0	25	I	RD	36	O	$\overline{RTS}$
4	I/O	D2	15	I	CS1	26	O	DDIS	37	O	$\overline{DTR}$
5	I/O	D3	16	I	$\overline{CS2}$	27	O	$\overline{TXRDY}$	38	O	$\overline{OUT1}$
6	I/O	D4	17	O	$\overline{BAUDOUT}$	28	I	$\overline{ADS}$	39	I	MR
7	I/O	D5	18	I	XIN	29	I	A2	40	I	$\overline{CTS}$
8	I/O	D6	19	O	XOUT	30	I	A1	41	I	$\overline{DSR}$
9	I/O	D7	20	I	$\overline{WR}$	31	I	A0	42	I	$\overline{DCD}$
10	I	RCLK	21	I	WR	32	O	$\overline{RXRDY}$	43	I	$\overline{RI}$
11	I	SIN	22	—	GND	33	O	INTR	44	—	V_{DD}

INPUT

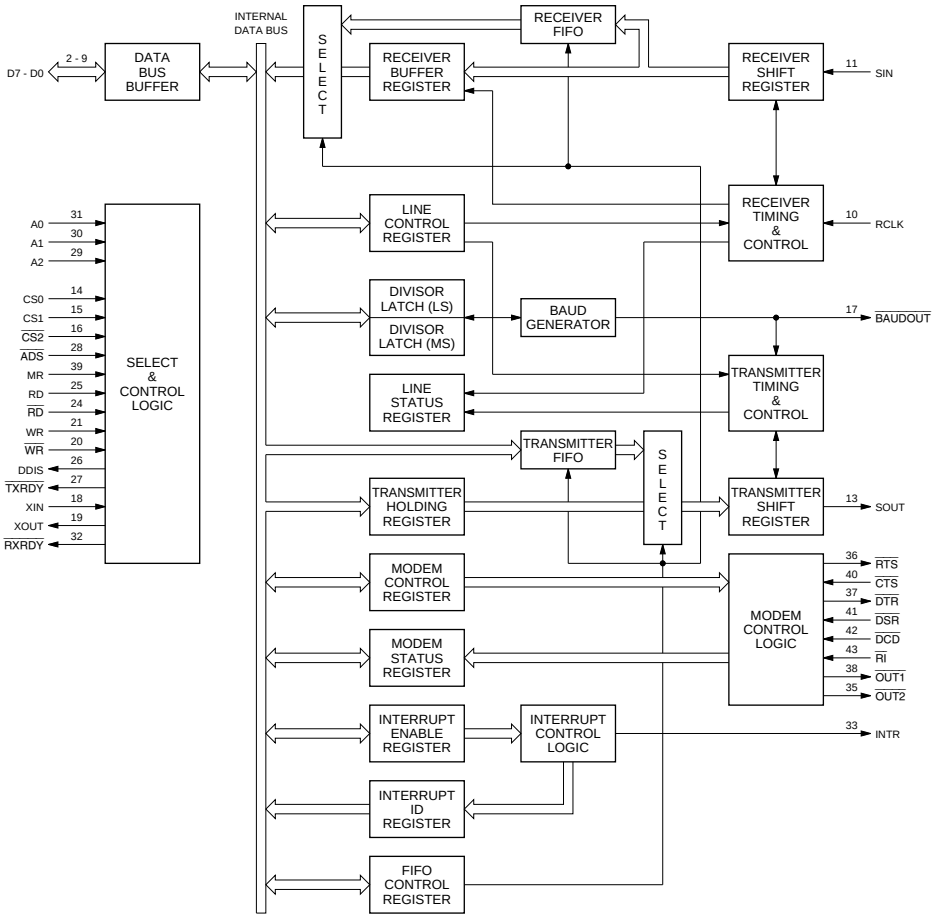
A0 - 2 : REGISTER ADDRESS DATA
$\overline{ADS}$: ADDRESS STROBE
CS0, 1, $\overline{2}$: CHIP SELECT
$\overline{CTS}$: CLEAR TO SEND
$\overline{DCD}$: DATA CARRIER DETECT
$\overline{DSR}$: DATA SET READY
MR : MASTER RESET
RCLK : RECEIVER CLOCK
RD : READ
$\overline{RI}$: RING INDICATOR
SIN : SERIAL DATA
WR : WRITE
XIN : EXTERNAL CRYSTAL

OUTPUT

$\overline{BAUDOUT}$: BAUD OUT
DDIS : DRIVER DISABLE
$\overline{DTR}$: DATA TERMINAL READY
INTR : INTERRUPT
$\overline{OUT1}$, $\overline{2}$: OUTPUT 1, 2
$\overline{RTS}$: REQUEST TO SEND
$\overline{RXRDY}$: RECEIVE READY
SOUT : SERIAL DATA
$\overline{TXRDY}$: TRANSMIT READY
XOUT : EXTERNAL CRYSTAL

INPUT/OUTPUT

D7 - D0 : DATA BUS


INTERNAL
DATA BUS
D7 - D0
2 - 9
DATA
BUS
BUFFER
SELECT
RECEIVER
FIFO
RECEIVER
BUFFER
REGISTER
RECEIVER
SHIFT
REGISTER
11
SIN
RECEIVER
TIMING
&
CONTROL
10
RCLK
LINE
CONTROL
REGISTER
DIVISOR
LATCH (LS)
DIVISOR
LATCH (MS)
BAUD
GENERATOR
17
BAUDOUT
LINE
STATUS
REGISTER
TRANSMITTER
TIMING
&
CONTROL
TRANSMITTER
FIFO
SELECT
TRANSMITTER
HOLDING
REGISTER
TRANSMITTER
SHIFT
REGISTER
13
SOUT
MODEM
CONTROL
REGISTER
MODEM
CONTROL
LOGIC
36
RTS
40
CTS
37
DTR
41
DSR
42
DCD
43
RI
38
OUT1
35
OUT2
MODEM
STATUS
REGISTER
INTERRUPT
ENABLE
REGISTER
INTERRUPT
CONTROL
LOGIC
33
INTR
INTERRUPT
ID
REGISTER
FIFO
CONTROL
REGISTER
SELECT
&
CONTROL
LOGIC
31
A0
30
A1
29
A2
14
CS0
15
CS1
16
CS2
28
ADS
39
MR
25
RD
24
RD
21
WR
20
WR
26
DDIS
27
TXRDY
18
XIN
19
XOUT
32
RXRDY