

# PBR 532 01/1 LPC Line Resistor Network

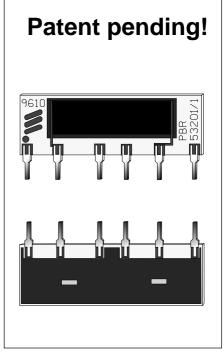
# **Description**

The Line Protection Resistor Network (LPC) PBR 532 01/1 consists of a ratio matched pair of thickfilm resistors and a Ring Feed / Trip Power Resistor on a ceramic substrate. PBR 532 01/1 is used in telephone line interface overvoltage protection networks, where the LPC resistors limit the current flow through voltage clamping devices such as diodes, tranzorbs, silicon thyristor diode transient suppressors etc.

The Ring Feed Resistor (  $430~\Omega$  ) can handle high power pulses during ringing . The resistors will withstand multiple voltage/current surges of either polarity without failure and with only a negligible change inside specified values. If exposed to power cross conditions, the included Thermal fuses will open depending on the applied condition. The PBR 532 01/1 meets requirements set forth in Bellcore TR-NWT 001089 and UL 1459.

# **Key Features**

- Two matched (  $20 \Omega$  ) resistors in a single-in-line package
- Includes a Ring Feed / Trip Power resistor (  $430 \Omega$  )
- Ratio match maintained after multiple surges
- Ratio match maintained after multiple power cross (first level)
- Safe fuse function for destructive power cross ( second level )
- Non-flammable materials
- Auto insertable
- · Low mechanical profile.



Line Resistor Network PBR 532 01/1.

# Preliminary



# **Absolute Maximum Ratings**

 $T_{amb}$  = +25 ± 2 °C unless otherwise stated.

Parameter	Symbol	Min	Max.	Unit
Temperature				
Operating temperature range	$T_{amb}$	-40	+85	°C
Power Dissipation, T <sub>amb</sub> = + 85 °C				
Per resistor	P <sub>diss</sub>		2	W
Per Resistor Network	P <sub>diss</sub>		2	W
Surge Voltage 10/700 μs, 1500 V (note 1, 2, 4)				
Change in resistance after 10 surges CM - DM	$\Delta$ R1, $\Delta$ R2, $\Delta$ R3	-2	+2	%
Change in ratio (matching) after 10 surges (CM - DM)	Δ(R1/R2)	-1	+1	%
Surge Voltage 6/400 μs, 600 V (note 1, 3, 4)				
Change in resistance after 10 surges CM - DM	$\Delta$ R1, $\Delta$ R2, $\Delta$ R3	-2	+2	%
Change in ratio (matching) after 10 surges (CM - DM)	Δ(R1/R2)	-1	+1	%
Surge Voltage 1/2 μs, 1500 V (note 1, 3)				
Change in resistance after 10 surges CM - DM	ΔR1, ΔR2 , ΔR3	-2	+2	%
Change in ratio (matching) after 10 surges (CM - DM)	Δ(R1/R2)	-1	+1	%
Surge Voltage 2/10 μs, 665 V (note 1, 3)				
Change in resistance after 20 surges CM - DM	$\Delta$ R1, $\Delta$ R2, $\Delta$ R3	-2	+2	%
Change in ratio (matching) after 20 surges (CM - DM)	Δ(R1/R2)	-1	+1	%
Power Induction 600 VAC, 600 $\Omega$ (note 1, 4)				
Duration of Voltage	t <sub>on</sub>		1,0	S
Change in resistance after 60 applications CM - DM (60 s pulse to pulse)	ΔR1, ΔR2 , ΔR3	-2	+2	%
Change in ratio (matching) after 60 applications (CM - DM)	Δ(R1/R2)	-1	+1	%
Power Induction 220 VAC, 600 $\Omega$ (note 1, 4)				
Duration of Voltage	t <sub>on</sub>		15	min
Change in resistance after 1 application CM	ΔR1, ΔR2 , ΔR3	-2	+2	%
Change in ratio (matching) after 1 application (CM)	Δ(R1/R2)	-1	+1	%
Power Cross 220 VAC, $\leq$ 10 $\Omega$ (note 1, 5)				
Duration of Voltage	t <sub>on</sub>		15	min
Power Cross Destructive, $\leq$ 3 $\Omega$ (note 1, 5)				
Duration of Voltage	t <sub>on</sub>		15	min
Voltage	Ü	100	600	VAC

### **Electrical Characteristics**

 $T_{amb}$  = +25  $\pm$  2 °C unless otherwise stated.

Parameter	Condition	Min	Typical	Max.	Unit
Resistance/Ratio					
Resistor R1, R2		19,8	20	20,2	Ω
Ratio R1/R2		0,995	1,0	1,005	-
R1, R2: Resistance Vs Temperature	$T_{amb} = -40 \text{ to } + 85 ^{\circ}\text{C}$	19,7	20,0	20,3	Ω
Tracking R1 - R2	$T_{amb} = -40 \text{ to } + 85 ^{\circ}\text{C}$	0,995	1,00	1,005	-
Resistor R3		421	430	439	Ω
Insulation					
Insulation R1 - R2 - R3	U = 1000 VDC	1000			$M\Omega$

#### Notes

Note 1: Common Mode (CM) and Differential Mode (DM) are applied if stated. DM equals R1 or R2 tested, CM R1 and R2 simultaneously Note 2: Surge voltage shape measured according to IEC 60-2, section 4. Surge voltage, peak voltage, shape and schematics according to ITU-T rec. k17. The surge peak voltage over the resistors: 500 V.

Note 3: Surge voltage shape measured according to IEC 60-2, section 4. Surge voltage pulse shape over the resistor.

Note 4: Reference: ITU-T k20

Note 5: For the test, the requirements are:

- The line resistor is not to start to burn with open flame
- No induction of fire of the surroundings

 No operating of circuit included fuse's (wire simulator fuse)

Conditions (Reference: TR-NWT 001089, ¶ 4.5, Second level tests):

a) max. 600 VAC, Rs = 20 per lead, CM, Initial current 0,5 A, Current increased not more than 20 % per 15 min period. b) 600 VAC, Rs =  $20 \Omega$ , CM c) 600 VAC, Rs =  $600 \Omega$ , CM



# **Pin Description**

Figure 1: Circuit diagram Pin 1 is the leftmost pin on the side with marking. Pin 7 and 9 are named a and b and equals the outgoing line. All other combinations of placing of a and b are less severe than above stated due to the design of the Line resistor.

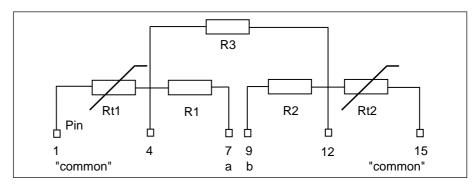


Figure 1. Circuit diagram.

## **Functional Description**

#### General

The Line Protection Resistor Network consists of three thick film resistors in combination with thermal fuse's.

#### **Fuse Function of the LPC**

For destructive power cross, the LPC will break open (either the substrate or the thermal fuse). The thermal fuse is activated at low currents which only heats the resistor network and the substrate will break open at high currents. The thermal fuse will operate when temperature within the LPC is

more than 240 °C for 20 s. The thermal fuse will then safely open and stop the current flow and therefore protect the PCB from high temperatures.

The actual power required for operating the fuse depends on the cooling of the resistor network. The cooling is dependent on the mass of the PCB (number of layers, area of metal layer etc.) and the air cooling (forced air cooling, convection etc.). For destructive power cross, the LPC will break open (either the substrate or the Thermal Fuse).It is also designed to fulfil surge voltage requirements set forth in ITU-T k17/k20 and Bellcore.

#### High voltage characteristics

For high voltages, i.e. surge voltage and power cross test, the resistance of the LPC is not lower than 19,5 ohms and not higher than 20,5 ohms.

#### Break open characteristics

The LPC has the following break open characteristics: Common Mode (CM) and Differential Mode (DM) are applied if stated. DM equals R1 or R2 tested, CM R1 and R2 simultaneously.

Note: In DM, the LPC will not break both the "a"- and "b" branch open; i.e. if the voltage is applied to "a", only R1 will break open within stated time. See also diagram 1.

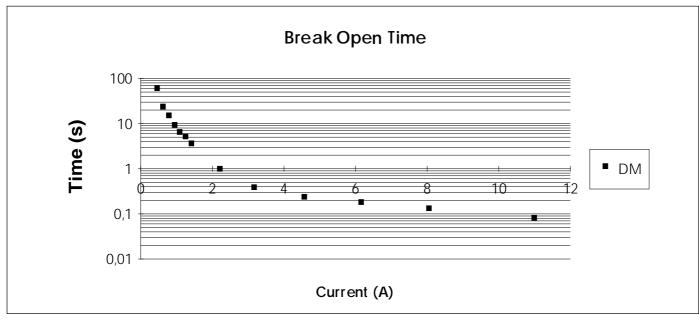


Figure 2. Diagram 1 Break open Time.

# Preliminary



## **Quality Specifications**

The LPC is delivered at the following AQL:

Resistance, Ratio:
 AQL 0,4, Level II
Surge Voltage, Power Cross:
 AQL 1,0, Level S-3
according to
IEC 410, MIL STD 105.

#### Pin types and Package

Three different pins are available:

*Type A:* (On Request) Non-preformed lead for 0,8-1,0 mm through-hole-mounting

Type B: Pre-formed lead for 1,0 mm through-hole-mounting

*Type C:* (On Request) Pre-formed lead for 0,8 mm through-hole-mounting

Two types of packages are available:

*Bulk:* with the LPC's individually fixed in a carrier.

Taped: with the LPC's placed on a tape as described in IEC 286-2.

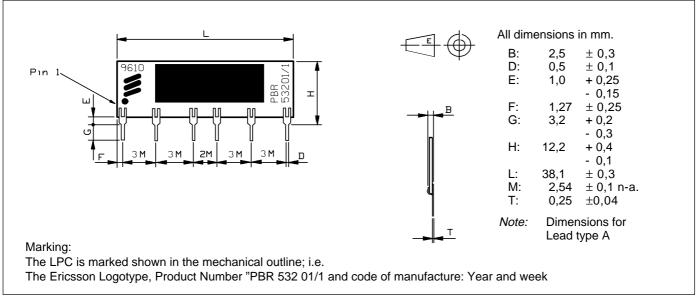


Figure. 3 Mechanical outline.

# **Ordering Information**

The LPC may be ordered as:

PBR 532 01/1 AK, PBR 532 01/1 BK and PBR 532 01/1 CK for Bulk PBR 532 01/1 AT, PBR 532 01/1 BT and PBR 532 01/1 CT for Taped

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