

PBL 3798/5 Subscriber Line Interface Circuit

Description

PBL 3798/5 is an analog Subscriber Line Interface Circuit (SLIC), which is fabricated in a 75 V bipolar, monolithic process.

The programmable, constant current feed circuit incorporates a switch mode regulator to minimize on-chip power dissipation. A stand-by state further reduces idle power dissipation, while allowing the supervisory functions to be active.

Tip-ring polarity is reversible without altering SLIC supervisory and voice frequency (vf) functions. Tip and ring outputs can be set to high impedance states. These and other operating states are activated via a parallel, four bit control word.

An external resistor controls the off-hook detector threshold current. A ground key detector with internal reference reports tip/ring dc current unbalance. The ring trip detector can operate with both balanced and unbalanced ringing systems. The three detectors are read via a shared output.

Ring and test relay drivers with internal clamp diodes are provided.

The complex or real two-wire impedance is set by a scaled, lumped element network.

Two- to four-wire and four- to two-wire signal conversion is provided by the SLIC in conjunction with either a conventional or a programmable CODEC/filter.

Longitudinal line voltages are suppressed by a control loop within the SLIC.

The PBL 3798/5 package is 32-pin PLCC (batwing) or 44-pin PLCC, and the temperature range is -20°C to +70°C.

The PBL 3798/5 is specified to meet the requirements of BTNR 306, 315.

Key Features

- On-chip switch mode regulator to minimize power dissipation
- Programmable, constant current feed
- Line feed characteristics independent of battery variations
- Tip-ring polarity reversal function
- Tip and ring open circuit state; tip open with ring active state
- Detectors:
 - programmable loop current/ring ground detector
 - ground key detector
 - ring trip detector
- Ring and test relay drivers
- Line terminating impedance, complex or real, set by a simple external network
- Hybrid function with conventional or programmable CODEC/filters
- 70 dB longitudinal to metallic balance
- 79 mA peak longitudinal current suppression
- Idle noise < 7 dBrnC; < -83 dBup

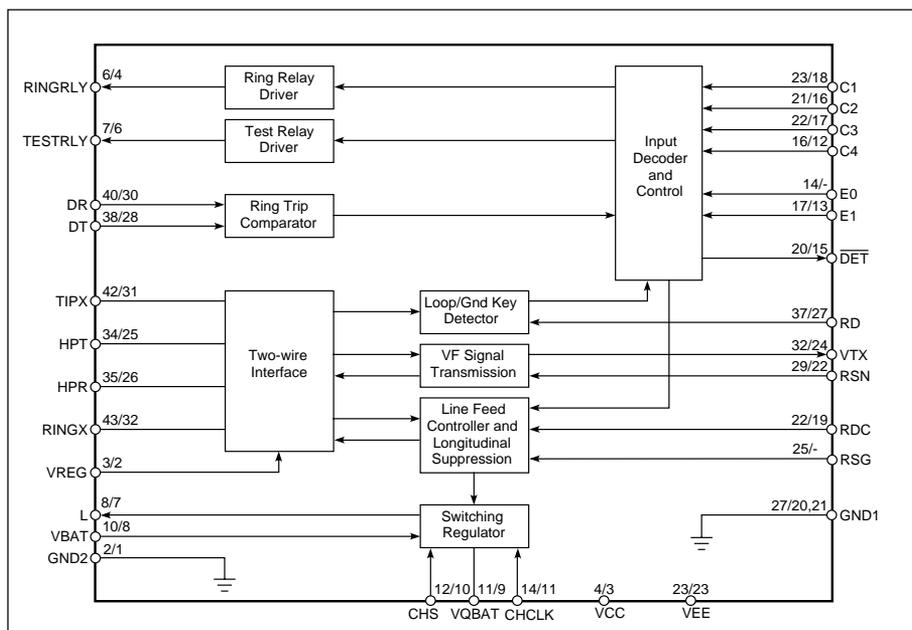
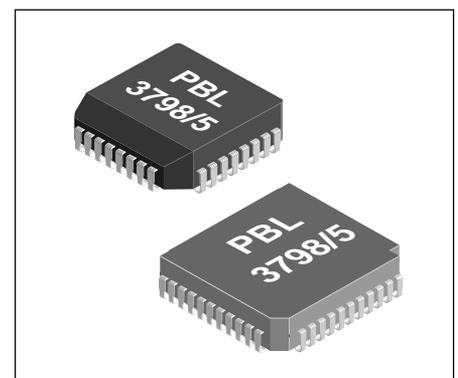


Figure 1. Block diagram.



32-pin PLCC, 44-pin PLCC

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature and Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating ambient temperature range	T_{Amb}	-40	+85	°C
Operating junction temperature range (Note 1)	T_j	-40	+135	°C
Power Supply				
V_{CC} with respect to ground	V_{CC}	-0.4	+6.5	V
V_{EE} with respect to ground	V_{EE}	-6.5	+0.4	V
V_{Bat} with respect to ground	V_{Bat}	-70	+0.4	V
Power Dissipation				
Continuous power dissipation at $T_{Amb} = 70$ °C (Note 3)				
32-pin, j-leaded chip carrier (RN)			1.7	W
44-pin, j-leaded chip carrier (QN)			1.5	W
Ground				
Voltage between GND1 and GND2 (Note 4)		-0.1	+0.1	V
Switch Mode Regulator				
Peak current through regulator switch (pin L)	I_{IPk}		150	mA
Regulator switch output (pin L) peak off-state voltage	V_{IPk}		+2	V
Relay Drivers				
Test relay supply voltage	V_{TRly}	V_{Bat}	V_{CC}	V
Ring relay supply voltage	V_{RRly}	V_{Bat}	V_{CC}	V
Test relay current	I_{TRly}		80	mA
Ring relay current	I_{RRly}		80	mA
Ring Trip Comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	0	V
Input current, $t_p = 10$ ms	I_{DT}, I_{DR}	-2	+2	mA
Digital Inputs, Outputs C1 - C4, E0, E1, \overline{DET}, CHCLK				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage (\overline{DET} not active)	V_{OD}	-0.3	V_{CC}	V
Output current	I_{OD}		3	mA
TIPX and RINGX Terminals				
TIPX or RINGX continuous voltage (Notes 5, 6)	V_{T^1}, V_R	-70	1	V
TIPX or RINGX, pulsed voltage, $t_w < 10$ ms and $t_{rep} > 10$ s (Notes 5, 6)	V_{T^1}, V_R	-70	5	V
TIPX or RINGX, pulsed voltage, $t_w < 1$ μ s and $t_{rep} > 10$ s (Notes 5, 6)	V_{T^1}, V_R	-90	10	V
TIPX or RINGX, pulsed voltage, $t_w < 250$ ns and $t_{rep} > 10$ s (Notes 5, 6, 7)	V_{T^1}, V_R	-120	15	V
TIPX or RINGX current	I_{Ldc}	-105	105	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	-20	70	°C
Case temperature	T_{Case}	-20	90	°C
V_{CC} with respect to ground	V_{CC}	4.75	5.25	V
V_{EE} with respect to ground	V_{EE}	-5.25	-4.75	V
V_{Bat} with respect to ground (Notes 8, 11)	V_{Bat}	-58	-40	V
GND2 with respect to GND1 (Note 10)	V_{G12}	0	0	V

Notes

1. The circuit includes thermal protection. Refer to section Over-temperature protection. Operation above 135 °C may degrade device reliability.
3. A power derating diagram for 32-pin PLCC is shown in figure 19. Values apply for junction temperature of 120°C without heatsink.
4. The GND1 and GND2 pins should be connected together via a direct printed circuit board trace.
5. V_T and V_R are referenced to ground. t_w is pulse width of a rectangular test pulse and t_{rep} is pulse repetition rate.
6. These voltage ratings require a diode to be installed in series with the VBAT pin as shown in figure 12 (D₇).
7. R_{F1} , $R_{F2} \geq 20 \Omega$ is also required. Pulse supplied to TIP and RING outside R_{F1} , R_{F2} .
8. For long loop applications with $-63 V < V_{Bat} < -56 V$, the saturation guard reference voltage V_{SGRef} , should be adjusted by calculating a value for resistor R_{SG} as described in the text. Note that the adjustment terminal, RSG, is available only on the 44-pin leaded chip carrier package.
9. V_{Bat} should be applied with a $\partial V_{Bat} / \partial t < 4 V / \mu\text{sec}$. A time constant of 2.6 μs is suggested (e.g. 5.6 Ω and 0.47 μF). The VBAT terminal must at all times be at a lower potential than any other terminal to maintain proper junction isolation. Refer to section Power-up sequence.
10. GND1 and GND2 must be connected before supply voltages.
11. A VBAT of maximum -40 v may be used. However with a VBAT of -40 to -46 V, the performance on long lines** will degrade outside the specified limits. Parameters effected are; Line current, longitudinal balance, idle channel noise and VBAT PSRR.
** Long lines is in this case outside the constant current range with the VBAT dependant saturation guard activated.

Electrical Characteristics

$-20 \text{ }^\circ\text{C} \leq T_{Amb} \leq 70 \text{ }^\circ\text{C}$, $V_{CC} = +5 V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $-58 V \leq V_{Bat} \leq -46 V$, GND1 = GND2, Z_{TR} (2-wire ac terminating impedance) = 600 Ω , Z_L (line impedance) = 600 Ω , $R_{F1} = R_{F2} = 0 \Omega$, $R_T = 60 \text{ k}\Omega$, $R_{RX} = 30 \text{ k}\Omega$, $R_{DC1} = R_{DC2} = 3.9 \text{ k}\Omega$, $R_{SG} = \infty$, $R_D = 51.1 \text{ k}\Omega$, $R_{CH} = 910 \Omega$, $R_{Bat} = 10 \Omega$, $C_{HP} = 0.33 \mu\text{F}$, $C_{DC} = 0.33 \mu\text{F}$, $C_D = 0.01 \mu\text{F}$, $C_{TC} = C_{RC} = 2200 \text{ pF}$, $C_{CH1} = 0.047 \mu\text{F}$, $C_{CH2} = 1500\text{pF}$, $C_{Rt} = 0.47 \mu\text{F}$, $C_{Bat} = 0.47 \mu\text{F}$, $C_Q = 0.33 \mu\text{F}$, $L = 1\text{mH}$, unless otherwise specified. The specifications are with respect to exact external component values.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
2-wire port						
Overload level, V_{TRO}	2	1% THD, $E_L = 0$, $f = 1 \text{ kHz}$, (Note 1)	3.1 9.0 9.0	3.5 10.1 10.1		V_{PK} dBm dBu
Input impedance, Z_{TRX}		Note 3				
Longitudinal impedance, Z_{LoT} , Z_{LoR}	3	$f \leq 100 \text{ Hz}$		25	40	Ω/wire
Longitudinal current limit, I_{LoT} , I_{LoR}		$f \leq 100 \text{ Hz}$				
		Active state	20	28		$\text{mA}_{rms}/\text{wire}$
		Stand-by state	8.5	19		$\text{mA}_{rms}/\text{wire}$
Longitudinal to metallic balance, (L1), Blme	4	40 Hz < f < 4kHz Blme = $20 \cdot \log(E_{lo}/V_{tr})$				
		Normal polarity	47	70		dB
		Reversed polarity	47	65		dB

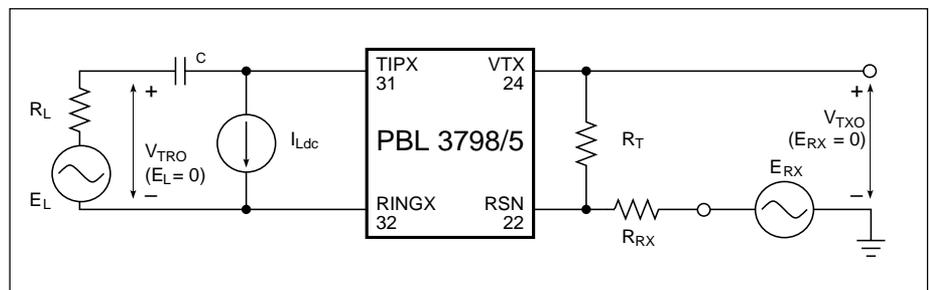


Figure 2. Overload level.
 $1/\omega C \ll R_L$, $R_L = 600 \text{ ohm}$,
 $R_T = 60 \text{ kohms}$, $R_{RX} = 30 \text{ kohms}$.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Longitudinal to four wire balance Blfe (Longitudinal Signal Rejection)	4	40 Hz < f < 4 kHz				
		Blfe = 20 • log (Elo/Vtx) Normal polarity	47	70		dB
		Reverse polarity	47	65		dB
Four wire to longitudinal balance, (L2), Bfle,	5	Bfle = 20 • log (ErX/Vlo) Etr source removed				
		0.2 kHz < f < 4.0 kHz				
(Longitudinal Signal Generation)		Normal polarity	40	50		dB
		Reversed polarity	40	50		dB
Sum of L1 + L2		Conditions as above				
		0.2kHz < f < 4.0kHz	100	110		dB
2-wire return loss, r		$r = 20 \cdot \log \left \frac{Z_L + Z_{TR}}{Z_L - Z_{TR}} \right $, Note 5				
		0.2kHz ≤ f < 0.5kHz	30	32		dB
		0.5kHz ≤ f < 1.0kHz	25	27		dB
		1.0kHz ≤ f ≤ 3.4kHz	15	17		dB
Polarity reversal time, t _{pol}		Normal to reversed polarity or reversed to normal polarity		4	15	ms
TIPX idle voltage, V _{Ti}		Normal polarity, stand-by				
		V _{Bat} = -48V	-5.0	-3.5	-2.0	V
		V _{Bat} = -63V, Note 6	-5.0	-3.5	-2.0	V
TIPX to RINGX idle voltage, V _{Tr0}		Active and standby				
		V _{Bat} = -48V, R _i = open loop				
		Normal polarity			42	V
		Reversed polarity	-42			V

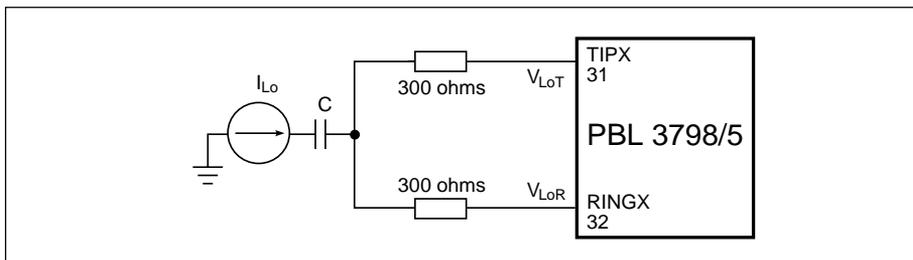


Figure 3. Longitudinal input impedance.
 $Z_{LoT} = Z_{LoR} = \frac{V_{LoT} + V_{LoR}}{I_{Lo}}$

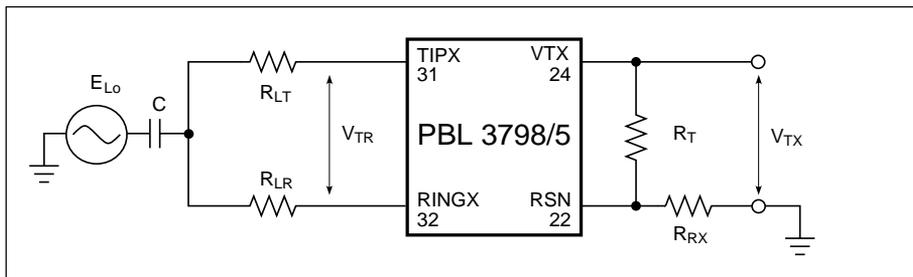


Figure 4. Longitudinal-to-metallic (B_{LME})
and Longitudinal-to-four-wire (B_{LFE})
balance.
 $1/\omega C \ll 150 \Omega$,
 $R_{LT} = R_{LR} = 300 \Omega$, $R_T = 60 \text{ k}\Omega$,
 $R_{RX} = 30 \text{ k}\Omega$.

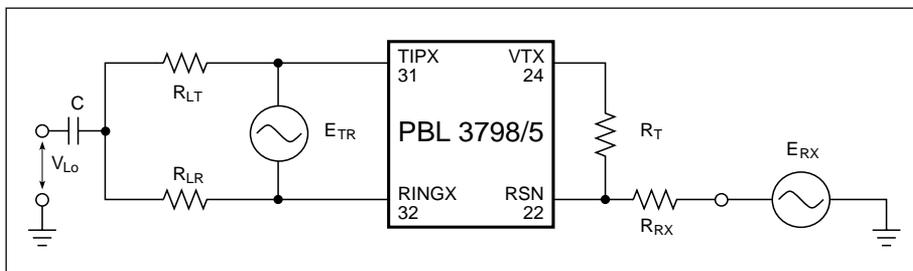


Figure 5. Metallic-to-longitudinal (B_{LME})
and four-wire-to-longitudinal (B_{LFE})
balance.
 $1/\omega C \ll 150 \Omega$,
 $R_{LT} = R_{LR} = 300 \Omega$, $R_T = 60 \text{ k}\Omega$,
 $R_{RX} = 30 \text{ k}\Omega$.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
4-wire Transmit Port (VTX)						
Overload level, V_{TXO}	2	Load impedance > 20 k Ω , $f = 1$ kHz, 1% THD, $E_{RX} = 0$ Note 7	3.1 9.0	3.5 10.1		V_{pk} dBu
Output offset voltage, ΔV_{TX}			-50	± 5	+50	mV
Output impedance, Z_{TX}		0.2kHz $\leq f \leq$ 3.4kHz		10	20	Ω
4-wire Receive Port (RSN)						
RSN dc voltage, V_{RSN}		$I_{RSN} = 0$	-10	0	+10	mV
RSN impedance, Z_{RSN}		0.2kHz $\leq f \leq$ 3.4kHz		3	20	Ω
RSN current (I_{RSN}) to metallic loop current (I_L) gain, a_{RSN}		0.2kHz $\leq f \leq$ 3.4kHz, $a_{RSN} = \frac{I_L}{I_{RSN}}$		40		dB
Frequency Response						
Two-wire to four-wire, g_{2-4}	6	0.3kHz $\leq f \leq$ 3.4kHz Relative to 1.0 kHz, 0 dBu $E_{RX} = 0$ V, (Notes 2, 8)	-0.15	± 0.03	+0.15	dB
Four-wire to two-wire, g_{4-2}	6	0.3kHz $\leq f \leq$ 3.4kHz Relative to 1.0 kHz, 0 dBu $E_L = 0$ V, (Notes 2, 9)	-0.15	± 0.03	+0.15	dB
Four-wire to four-wire, g_{4-4}	6	0.3kHz $\leq f \leq$ 3.4kHz Relative to 1.0 kHz, 0 dBu $E_L = 0$ V, (Notes 2, 9)	-0.15	± 0.06	+0.15	dB
Insertion Loss						
Two-wire to four-wire, G_{2-4}	6	0 dBu, 1 kHz, $E_{RX} = 0$ (Notes 8, 10)	-0.15	± 0.1	+0.15	dB
Four-wire to two-wire, G_{4-2}	6	0 dBu, 1 kHz, $E_L = 0$ 16 kHz (Notes 9, 10)	-0.15 -0.88	± 0.1	+0.15 -0.28	dB dB
Four-wire to four-wire, G_{4-4}	6	0 dBu, 1 kHz, $E_L = 0$ (Notes 9, 10)	-0.15	± 0.1	+0.15	dB
Gain Tracking						
Two-wire to four-wire (Note 8) and Four-wire to two-wire (Note 9)	6	Referenced to -10 dBu, 1 kHz -10 dBu to -55 dBu	-0.15		+0.15	dB
Noise						
Idle channel noise at two-wire (TIPX-RINGX) or four-wire (VTX) port	6	$E_{RX} = E_L = 0$, Notes 2, 11 C-msg weighting Psophometrical weighting		7 -83	10 -80	dBmC dBup

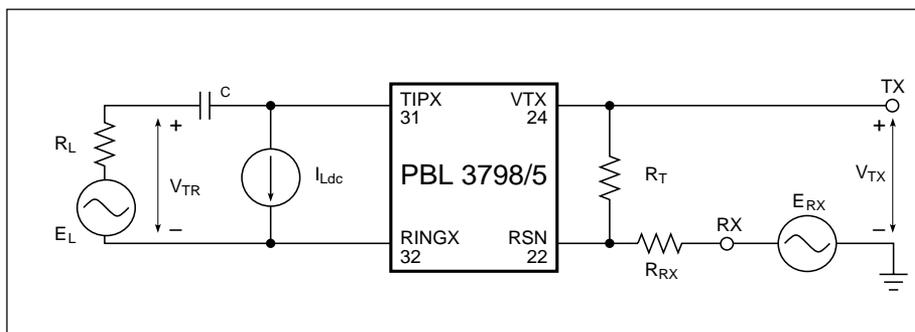


Figure 6. Frequency response, insertion loss, gain tracking, idle channel noise, THD, inter-modulation.
 $1/\omega C \ll R_L$, $R_L = 600 \Omega$,
 $R_T = 60 \text{ k}\Omega$, $R_{RX} = 30 \text{ k}\Omega$.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Single Frequency out-of-band Noise (Note 12, 20)						
Metallic, V_{TR}	7	BTNR 306, Issue 1 January 1985, fig. 7b				
Longitudinal, V_{Lo}	7	BTNR 306, Issue 1 January 1985, fig 7c				
Chopper noise Metallic, V_{tr}	7	128 kHz and its harmonics			-55	dBu
Longitudinal, V_{Lo}					-50	dBu
Total Harmonic Distortion						
Two-wire to four-wire, Four-wire to two-wire	6	$0.3\text{kHz} \leq f \leq 3.4\text{kHz}$ 0 dBu, 1 kHz test signal, Note 2		-64	-50	dB
Intermodulation						
Type $2f_1 - f_2$	6	$0.3\text{ kHz} < f_1, f_2 < 3.4\text{ kHz}$, Level $f_1 = \text{level } f_2 = -25\text{ to } 0\text{ dBv}$ $f_1 \neq nf_2, f_2 \neq nf_1$, Note 2				
Two-wire to four-wire		$E_{RX} = 0$		-60	-50	dB
Four-wire to two-wire		$E_L = 0$		-60	-50	dB
Type $f_1 \pm 50\text{ Hz}$	6	$0.3\text{kHz} < f_1 < 3.4\text{kHz}$ Level 50 Hz = level $f_1 - 14\text{ dB}$, Level $f_1 = -15\text{ dBv to } 0\text{ dBv}$ $f_1 \neq n \cdot 50\text{ Hz}$, Note 2				
Two-wire to four-wire		$E_{RX} = 0$		-65	-50	dB
Battery Feed Characteristics						
Loop current in constant current region, $ I_{Ldc} $	17	$R_{DC1} = R_{DC2} = 3.9\text{ k}\Omega$ Active state $p = 1$, Active polarity reversal state $p = -1$	30 -34	32 -32	34 -30	mA mA
		$I_{Ldc} = p \cdot \frac{250}{R_{DC1} + R_{DC2}}$				
		Stand-by state $p = 1$	14.4	16	17.6	mA
		Stand-by polarity reversal state $p = -1$	-17.6	-16	-14.4	mA
		$I_{Ldc} = p \cdot \frac{125}{R_{DC1} + R_{DC2}}$				
Loop current in constant current region at maximum loop resistance, $ I_{Ldc} $	17	$R_{DC1} = R_{DC2} = 3.9\text{ k}\Omega$ Active state $V_{Bat} = -48\text{ V}, R_{Lmax} = 950\ \Omega$	30			mA
Loop current outside constant current region, $ I_{Ldc} $	17	$R_{DC1} = R_{DC2} = 3.9\text{ k}\Omega$ Active state $V_{Bat} = -48\text{ V}, R_{Lmax} = 2\text{ k}\Omega$ Note 13	15.5			mA

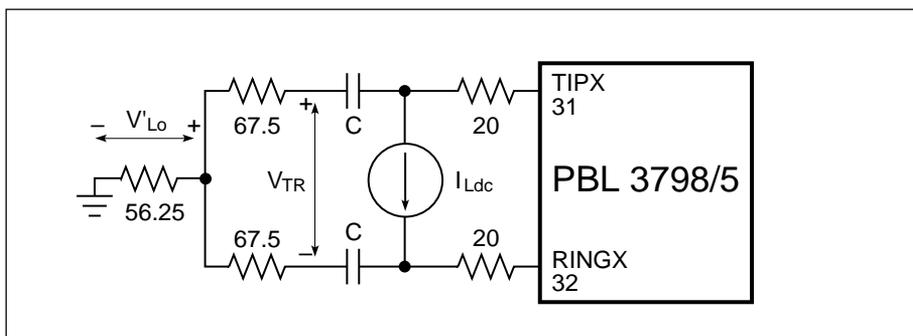


Figure 7. Single-frequency out of band noise.
Resistance values in ohms,
 $V'_{Lo} = 1.6 \cdot V_{Lo}$
 $1/\omega C \ll 100\text{ ohms}$

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Tip Open Circuit State						
TIPX current, I_{LTLkTo}	8	Tip open circuit state $V_{Bat} < V_{TTO} < 0$	-100	±5	100	µA
RINGX current, I_{LRT0}	8	Tip open circuit state $R_{LRGnd} = 0 \Omega$	22	35	50	mA
RINGX voltage, V_{RT0}	8	$I_{LRT0} < 22 \text{ mA}$	$V_{Bat} + 1$	$V_{Bat} + 4$	$V_{Bat} + 6$	V
Loop Current Detector						
Loop current detector conversion factor On-hook to off-hook, K_{LThOff}		$I_{LThOff} = K_{LThOff}/R_D$ Active, standby, polarity reversal state	395	465	535	V
		Tip open circuit state (Note 14)	745	930	1115	V
Loop current detector conversion factor Off-hook to on-hook, K_{LThOn}		$I_{LThOn} = K_{LThOn}/R_D$ Active, standby, polarity reversal state	348	410	472	V
		Tip open circuit state (Note 14)	655	820	985	V
Loop current detector conversion factor hysteresis, K_{LTh}		Active, standby and Polarity reversal state (Note 15)	20	55	90	V
Dial pulse distortion		10 pps, Off-hook: 600 Ω On-hook: ∞ ohm		1	5	%
Ring Trip Comparator Inputs (DT, DR)						
Offset voltage, ΔV_{DTR}	9	$V_{Bat} + 1 \text{ V} < V_{DT}, V_{DR} < -2 \text{ V}$ $R = 200 \text{ k}\Omega$ $R = 0\Omega$	-40 -20	±10 ±10	40 20	mV mV
Input offset current, ΔI_B	9	$V_{Bat} + 1 \text{ V} < V_{DT}, V_{DR} < -2 \text{ V}, R = 200 \text{ k}\Omega$		0.05	1	µA
Input bias current, I_B	9	$V_{Bat} + 1 \text{ V} < V_{DT}, V_{DR} < -2 \text{ V}, R = 200 \text{ k}\Omega$ $I_B = (I_{DT} + I_{DR})/2$		0.1	1	µA
Input resistance unbalanced, R_{DT}, R_{DR}		$V_{Bat} + 1 \text{ V} < V_{DT}, V_{DR} < -2 \text{ V}$		1		MΩ
balanced, R_{DTR}				3		MΩ
Common mode range, V_{DT}, V_{DR}			$V_{Bat} + 1$		-2	V
VReg Voltage (AGC Function)						
VReg voltage		Active and polarity reversal states RDC1 = RDC2 = 3.9 kΩ RL = 544 Ω RL = 744 Ω	-30.0 -36.3	-27.8 -33.6	-25.6 -30.9	V V

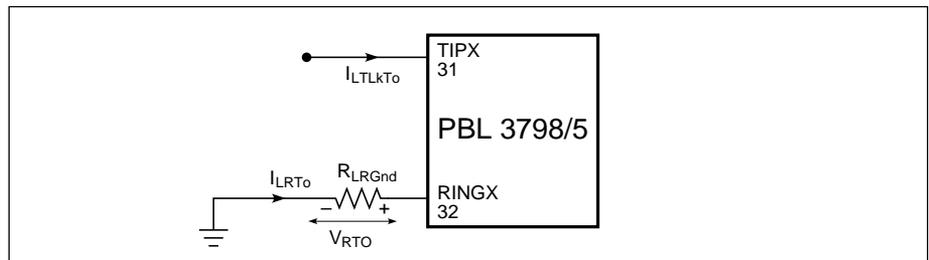


Figure 8. Tip open circuit state.

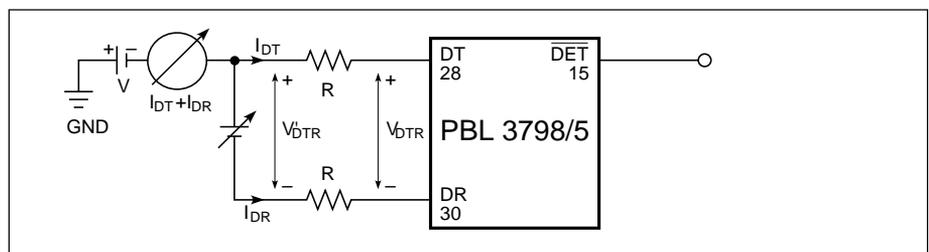
Figure 9. Ring trip comparator.

$$2V < V < |V_{Bat} + 1|,$$

$$\frac{I_{DT} + I_{DR}}{2} = I_B,$$

$$V_{DTR} = \Delta V_{DTR'}$$

$$\Delta I_B = \frac{V'_{DTR} - V_{DTR}}{R}$$



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Ground Key Detector						
Ground key detection threshold, R_{Gnd}	10	Active & stand-by states, $E_0 = E_1 = 1$ Note 19, 21				
		Switch S1 open 0-70°C	1.7		10.0	kΩ
		Switch S2 open $R_{SG} \neq \infty$	1.7		15.0	kΩ
		Switch S1 open -20 - 0°C not guaranteed				
		Switch S1 closed	0.9		10.0	kΩ
Longitudinal current threshold, I_{LoGkTh}	10	S1 closed		8		mA
Relay Driver Outputs (RINGRLY, TESTRLY)						
On state voltage, V_{TRly}, V_{RRly}		$I_{TRly}, I_{RRly} = 25 \text{ mA}$ $-20^\circ\text{C} < T_{Amb} < 25^\circ\text{C}$	$V_{CC}-2.0$	$V_{CC}-1.8$		V
		$25^\circ\text{C} < T_{Amb} < 70^\circ\text{C}$	$V_{CC}-1.8$	$V_{CC}-1.6$	$V_{CC}-1.0$	V
Off state leakage current, I_{TRly}, I_{RRly}		$V_{TRly}, V_{RRly} = V_{Bat}$		5	100	μA
Clamp voltage		$I_{TRly}, I_{RRly} = 25 \text{ mA}$	$V_{Bat}-3$		$V_{Bat}-1$	V
Digital Inputs (C1-C4, E0, E1, CHCLK)						
Input low voltage, V_{IL}					0.8	V
Input high voltage, V_{IH}			2.0			V
Input low current, I_{IL}		$V_{IL} = 0.4 \text{ V}$	-0.4			mA
Input high current, I_{IH}		$V_{IH} = 2.4 \text{ V}$			40	μA
Digital Output (DET)						
Output low voltage, V_{OL}		$I_{OL} = 1.0 \text{ mA}$			0.45	V
Output high voltage, V_{OH}		$I_{OH} = -0.1 \text{ mA}$	2.4			V
Resistive pull-up			12	15	18	kΩ
Switch Mode Regulator Transistor Output (L)						
Switch transistor saturation voltage, V_{ISat}		$I_L = 100 \text{ mA}$, Note 16			1.5	V
Leakage current, I_{Ilk}		$V_L = 0 \text{ V}$			200	μA
Switch Mode Regulator Clock Input (CHCLK)						
Clock frequency, f_{ChClk}			253	256	259	kHz
Rise and fall time					50	ns
Duty cycle ratio			46		54	%
Power Supply Rejection Ratio (PSRR)						
V_{CC} to two-wire port and V_{CC} to four-wire port rejection ratio, $PSRR_{CC}$		saturation guard off				
		50 Hz < f < 4 kHz	35			dB
		4 kHz < f < 50 kHz	30			dB
		saturation guard on				
		50 Hz < f < 50 kHz	20			dB
		Note 17				
V_{EE} to two-wire port and V_{EE} to four-wire port rejection ratio, $PSRR_{EE}$		50 Hz < f < 4 kHz	10			dB
		4 kHz < f < 50 kHz	0			dB
		Note 17				
V_{Bat} to two-wire port and V_{Bat} to four-wire port rejection ratio, $PSRR_{Bat}$		50 Hz < f < 4 kHz	25			dB
		4 kHz < f < 50 kHz, -20-+70°	20			dB
		Note 17				

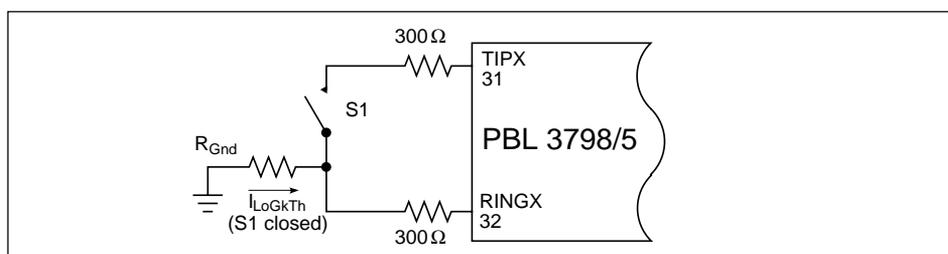


Figure 10. Ground key detector.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Power Supply Currents (relay drivers off)						
V_{CC} supply current, I_{CC}		On- or off-hook, active state		8	12	mA
V_{EE} supply current, $ I_{EE} $		On- or off-hook, active state		6	9	mA
V_{Bat} supply current, $ I_{Bat} $		On-hook, active state		3.5	6	mA
Power Dissipation						
On-hook total dissipation, P_{OnOp}		$V_{Bat} = -48$ V, Open circuit state		60	100	mW
On-hook total dissipation, P_{OnSb}		$V_{Bat} = -48$ V, Stand-by state		190	350	mW
On-hook total dissipation, P_{OnAct}		$V_{Bat} = -48$ V, Active state		225	350	mW
Off-hook total dissipation, P_{Off68}		$V_{Bat} = -48$ V, Active state $R_L = 600 \Omega$, $R_{DC1} = R_{DC2} = 3.125 \text{ k}\Omega$ Note 18		700	1000	mW
Temperature Guard						
Junction temperature at threshold, T_{JG}				140		$^{\circ}\text{C}$
Temperature guard hysteresis, ∂T_{JG}				10		$^{\circ}\text{C}$

Notes

- The overload level is specified at the two-wire port with the signal source at the four-wire receive port, i.e. $E_L = 0$ in figure 2.
- dBm is the ratio between power level P and a 1 mW reference power level, expressed in decibels, i.e.

$$\text{dBm} = 10 \cdot \log_{10} \frac{P}{1 \text{ mW}}$$
 dBu is the ratio between voltage Vrms and a 0.775 Vrms reference, expressed in decibels, i.e.

$$\text{dBu} = 20 \cdot \log_{10} \frac{V_{\text{rms}}}{0.775 \text{ Vrms}}$$
 dBu = dBm at impedance level 600 ohms
 dBv is the ratio between voltage V and a 1 V reference, expressed in decibels, i.e.

$$\text{dBv} = 20 \cdot \log_{10} \frac{V}{1 \text{ V}}$$
 dBup is the ratio between voltage V_p , measured via a psophometrical filter and a 0.775 Vrms reference, expressed in decibels, i.e.

$$\text{dBup} = 20 \cdot \log_{10} \frac{V_p}{0.775 \text{ Vrms}}$$
 dBrnC is the ratio between power level P_C , measured via a C-message filter and a 1 pW reference power level, expressed in decibels, i.e.

$$\text{dBrnC} = 10 \cdot \log_{10} \frac{P_C}{1 \text{ pW}}$$
- The two-wire impedance, Z_{TRX} , is programmable by selection of external component values according to:

$$Z_{TRX} = Z_T / (G_{2-4} \cdot \alpha)$$
 where:
 Z_{TRX} = impedance between the TIPX and RINGX terminals
 Z_T = programming network between the VTX and RSN terminals
 G_{2-4} = TIPX-RINGX to V_{TA} gain, nom. = 1 (0 dB ± 0.15 dB)
 α = receive current gain, nominally = 100 (40 dB ± 0.15 dB)
 The fuse resistors R_F add to the impedance presented by the SLIC at terminals TIPX and RINGX for a total two-wire impedance of $Z_{TR} = Z_{TRX} + 2R_F$.
- Normal polarity is defined as the tip lead being at a more positive potential than the ring lead. Reversed polarity is defined as the ring lead being at a more positive potential than the tip lead.
- Higher return loss values can be achieved by adding a reactive component to R_T , the two-wire terminating impedance programming resistor, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground. For $R_T = 60 \text{ k}\Omega$ the capacitance value is approximately 330 pF.
- $V_{Bat} = -63$ V is applicable to the PBL 3798/5 in a 44-pin leaded chip carrier with the RSG terminal connected to the V_{EE} supply.
- The overload level, V_{TXO} , is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2-4} = 1$.
- The level is specified at the two-wire port.
- The level is specified at the four-wire receive port (RX).
- Fuse resistors R_{F1} and R_{F2} impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for $R_{F1} = R_{F2} = 0 \Omega$.
- The two-wire idle noise is specified with the port terminated in 600Ω (R_L) and with the four-wire receive port grounded ($E_{RX} = 0$, $E_L = 0$; see figure 6).
 The four-wire idle noise at VTX is specified with the two-wire port terminated in 600 ohms (R_L). The four-wire receive port is grounded ($E_{RX} = 0$, $E_L = 0$; see figure 6).
 The idle channel noise degrades by approximately 5 dB when the saturation guard is active. Refer to section Battery feed for a description of the saturation guard.
- These specifications are valid for a longitudinal impedance of 90Ω and a metallic impedance of 135Ω .

13. Refer to section Battery Feed, Case 2.
14. Refer to Loop Monitoring Function, Loop current detector-active state, Loop current detector - tip open state.
15. The loop current detector threshold hysteresis is a function of the R_D value. Refer to note 14 above.
16. V_{ISat} is the voltage across the saturated transistor, i.e. between terminals VBAT and L.
17. Power supply rejection ratio test signal is 100 mVrms (sinusoidal).
18. Fuse resistor $R_{F1} = R_{F2} = 0$ ohm.
19. R_{Gnd} resistance value less than the specified range will trigger the ground key detector, i.e. set the DET output to logic level low.
20. BTNR 306, Issue 1, January 1985 figures 7b and 7c applies, with the exception of 128 kHz and its harmonics.
21. If a R_{SG} resistor is used in the 44-pin PLCC package, the specification with $R_{SG} \neq \infty$ is applicable.

Pin Description

PLCC: 44 pin and 32-pin, j-leaded chip carrier. Refer to figure 11. Pin X/Y 44PLCC terminal/32PLCC terminal.

44PLCC	32PLCC	Symbol	Description
1	—	NC	No internal connection. Note 1.
2	1	GND2	Ground. No internal connection to GND1. Note 2.
3	2	VREG	Regulated negative voltage for power amplifiers. The switch-mode regulator inductor, filter capacitor and RC stabilization network connect to this pin.
4	3	VCC	+5 V power supply.
5	—	NC	No internal connection. Note 1.
—	5	TP	TP is a thermal conduction pin tied to substrate (V_{QBat}). Note 3.
6	4	RINGRLY	Ring relay driver output. Sources up to 80 mA from VCC.
7	6	TESTRLY	Test relay driver output. Sources up to 80 mA from VCC.
8	7	L	Switch-mode regulator drive transistor output. The 1 mH inductor and the catch diode connect to this pin. These components must be connected with shortest possible lead lengths. The catch diode, including connecting leads, must exhibit a low inductance to clamp effectively, when the regulator switch opens.
9	—	NC	No internal connection. Note 1.
10	8	VBAT	Battery supply voltage. Negative with respect to GND2.
11	9	VQBAT	Quiet battery. An external filter capacitor connects between this pin and GND1 to provide filtered battery supply to signal processing circuits.
12	10	CHS	Switch-mode regulator stabilization network input. From this pin a capacitor connects to GND1 and a series RC network to VREG.
13	—	NC	No internal connection. Note 1.
14	11	CHCLK	Switch-mode regulator TTL compatible clock input. Nominal frequency: 256 kHz.
15	—	NC	No internal connection. Note 1.
16	12	C4	C1 , C2 , C3 and C4 are TTL compatible decoder inputs controlling the SLIC operating states.
17	13	E1	Detector select input. A logic high level enables the ground key detector. A logic low level enables the loop/ring-trip detector. TTL compatible input.
18	—	NC	No internal connection. Note 1.
19	14	E0	Detector output enable. A logic high level enables the DET output. A logic low level disables the DET output. TTL compatible input. The PBL 3798 in dual-in-line package has the DET output permanently enabled.
20	15	DET	Detector output. Inputs C1...C3 and E1 select the detector to be connected to this output. When DET is enabled via E0 a logic low level indicates that the selected detector is tripped. The DET output is open collector with internal pull-up resistor (15 kohms) to VCC. When disabled, DET thus appears to be a resistor connected to V_{CC} .
21	16	C2	Refer to pin C4 description.
22	17	C3	Refer to pin C4 description.
23	18	C1	Refer to pin C4 description.
24	—	NC	No internal connection. Note 1

44PLCC	32PLCC	Symbol	Description
25	—	RSG	Saturation guard programming input. A resistor, R_{SG} , between pins RSG and VEE adjusts the saturation guard for operation with V_{Bat} from -64.5 V to -46 V. The PBL 3798/5 32 pin surface mount package have the saturation guard internally set for operation with $V_{Bat} = -48$ V.
26	19	RDC	The constant dc loop current is programmed by two resistors connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to GND1 to filter noise and other disturbances before reaching the RSN input. V_{RDC} polarity is negative for normal tip-ring polarity and positive for reversed tip-ring polarity. $ V_{RDC} = 2.5V$ in the constant current region.
27	20&21	GND1	Ground. No internal connection to GND2. Note 2.
28	—	NC	No internal connection. Note 1.
29	22	RSN	Receive summing node. 100 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing between the TIPX and RINGX terminals. Programming networks for constant loop current, 2-wire impedance, and receive gain connect to the receive summing node.
30	—	NC	No internal connection. Note 1.
31	23	VEE	-5 V power supply.
32	24	VTX	Transmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND1 referenced signal at VTX with a gain of one. The two-wire impedance programming network connects between VTX and RSN.
33	—	NC	No internal connection. Note 1.
34	25	HPT	Tip side (HPT) of ac/dc separation capacitor.
35	26	HPR	Ring side (HPR) of ac/dc separation capacitor.
36	—	NC	No internal connection. Note 1.
37	27	RD	Loop current detector programming resistor, R_D , connects from RD to VEE. A filter capacitor C_D may be connected from RD to GND1.
38	28	DT	Inverting ring trip comparator input.
39	—	NC	No internal connection. Note 1.

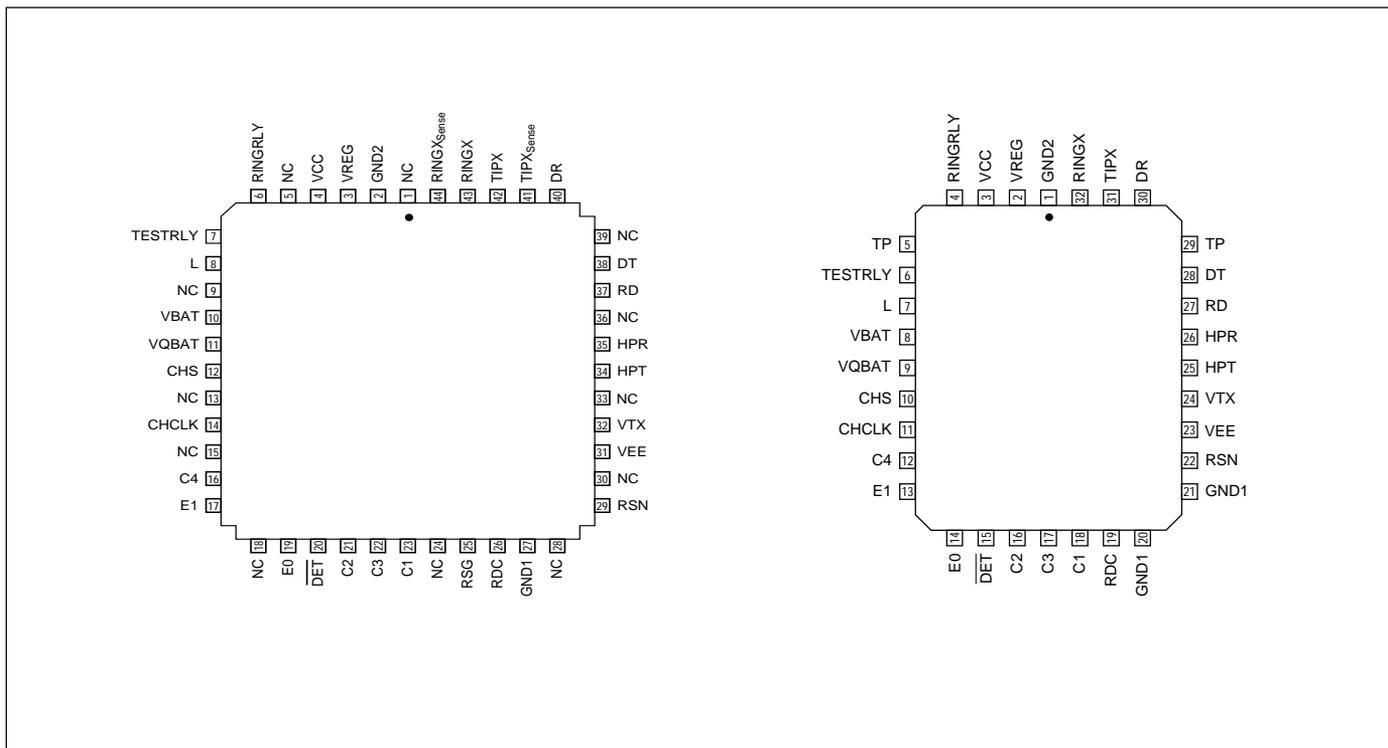
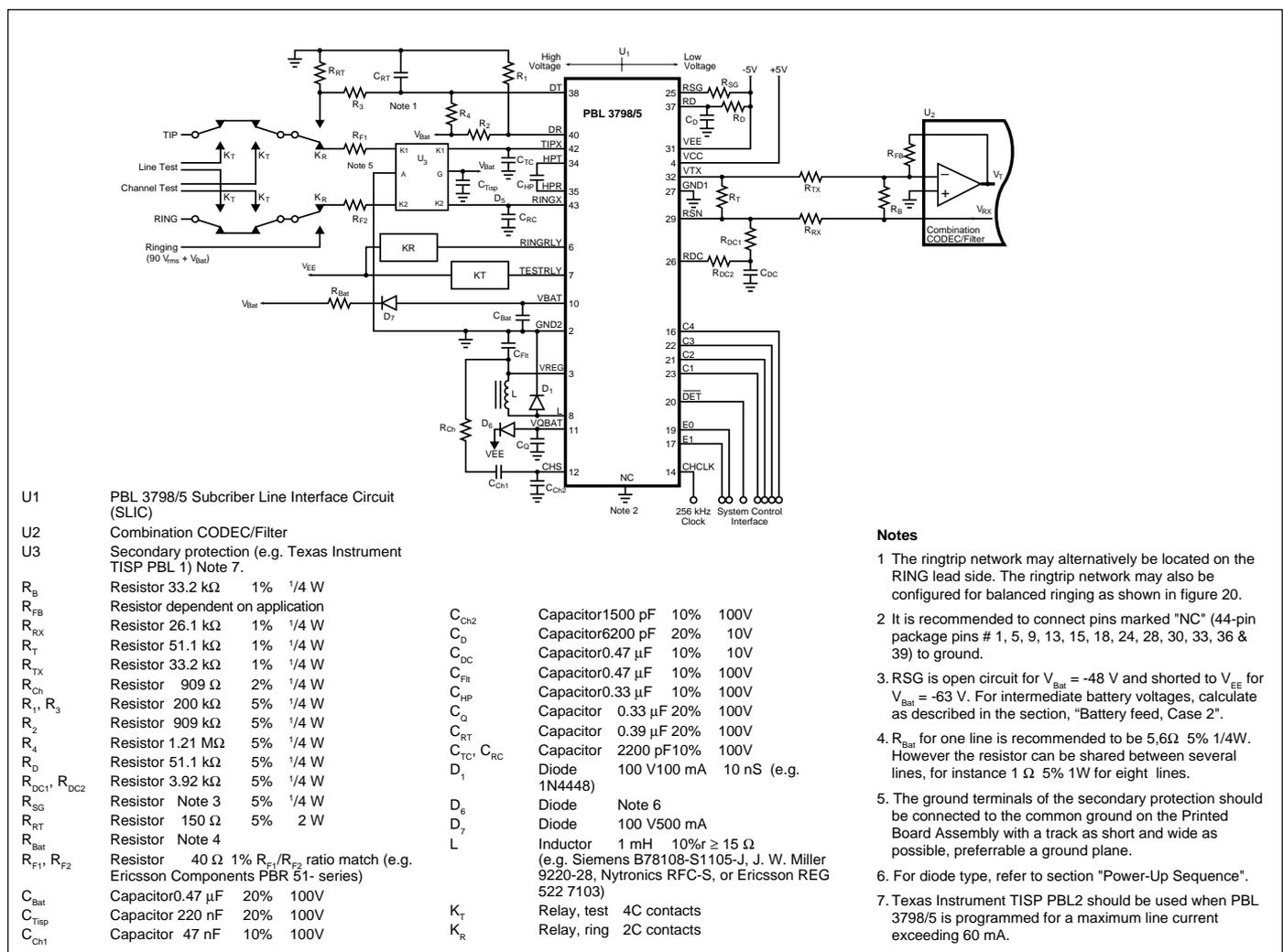


Figure 11. Pin configuration, 44-pin and 32-pin j-leaded chip carrier. Top view.

44PLCC	32PLCC	Symbol	Description
—	29	TP	TP is a thermal conduction pin tied to substrate (V_{QBat}). Note 3.
40	30	DR	Non-inverting ring trip comparator input.
41	—	TIPX _{Sense}	TIPX _{Sense} is internally connected to TIPX. TIPX _{Sense} is used during manufacturing, but requires no connection in SLIC applications, i.e. leave open.
42	31	TIPX	The TIPX pin connects to the tip lead of the 2-wire line interface via overvoltage protection components, ring and test relays.
43	32	RINGX	The RINGX pin connects to the ring lead of the 2-wire line interface via overvoltage protection components, ring and test relays.
44	—	RINGX _{Sense}	RINGX _{Sense} is internally connected to RINGX. RINGX _{Sense} is used during manufacturing, but requires no connection in SLIC applications, i.e. leave open.

Notes

1. Pins marked NC are not internally connected. It is recommended to ground these pins to provide shielding for sensitive terminals.
2. The GND1 and GND2 pins should be connected together via a direct printed circuit board trace.
3. For 32 pin PLCC, these pins (5 and 29) should be connected to V_{QBat} , serving as a heatsink.



Notes

1. The ringtrip network may alternatively be located on the RING lead side. The ringtrip network may also be configured for balanced ringing as shown in figure 20.
2. It is recommended to connect pins marked "NC" (44-pin package pins # 1, 5, 9, 13, 15, 18, 24, 28, 30, 33, 36 & 39) to ground.
3. RSG is open circuit for $V_{Bat} = -48$ V and shorted to V_{EE} for $V_{Bat} = -63$ V. For intermediate battery voltages, calculate as described in the section, "Battery feed, Case 2".
4. R_{Bat} for one line is recommended to be 5,6 Ω 5% 1/4W. However the resistor can be shared between several lines, for instance 1 Ω 5% 1W for eight lines.
5. The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferable a ground plane.
6. For diode type, refer to section "Power-Up Sequence".
7. Texas Instrument TISP PBL2 should be used when PBL 3798/5 is programmed for a maximum line current exceeding 60 mA.

Figure 12. PBL 3798/5 application example.

Functional Description and Applications Information Transmission

Overview

A simplified ac model of the transmission circuits is shown in figure 13. Neglecting the impact of the filters in figure 13 for frequencies from 300 Hz to 3.4 kHz (i.e. filter gain = 1), circuit analysis yields:

$$V_{TR} = V_{TX} + I_L \cdot 2R_F \quad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{100} \quad (2)$$

$$V_{TR} = E_L - I_L \cdot Z_L \quad (3)$$

where:

V_{TX} is the ground referenced, unity gain version of the ac metallic (transversal) voltage between the TIPX and RINGX terminals, i.e. $V_{TX} = 1 \cdot V_{TRX}$

V_{TR} is the ac metallic voltage between tip and ring.

E_L is the line open circuit ac metallic voltage.

I_L is the ac metallic current.

R_F is the overvoltage protection current limiting resistor.

Z_L is the line impedance.

Z_T is the programming network for the TIPX to RINGX impedance.

Z_{RX} controls the four-wire to two-wire gain.

V_{RX} is the analog ground referenced receive signal.

From equations (1), (2) and (3) expressions for two-wire impedance, two-wire to four-wire gain, four-wire to two-wire gain and four-wire to four wire gain may be derived.

Two-Wire Impedance

To calculate Z_{TR} , the impedance presented to the 2-wire line by the SLIC, including the resistors R_F , let $V_{RX} = 0$.

From (1) and (2):

$$Z_{TR} = \frac{Z_T}{100} + 2R_F$$

Since Z_{TR} and R_F are known Z_T may be calculated from

$$Z_T = 100 \cdot (Z_{TR} - 2R_F)$$

Example: calculate Z_T to make the terminating impedance $Z_{TR} = 900 \Omega$ in series with $2.16 \mu F$. $R_F = 40 \Omega$.

Using the expression above

$$Z_T = 100 \cdot (900 + \frac{1}{j\omega \cdot 2.16 \cdot 10^{-6}} - 2 \cdot 40)$$

$$= 82 \cdot 10^3 + \frac{1}{j\omega \cdot 21.6 \cdot 10^{-9}}$$

i.e. $Z_T = 82 \text{ k}\Omega$ in series with 21.6 nF . It is always necessary to have a high ohmic resistor in parallel with the capacitor. This gives a DC-feedback loop for low frequency which ensure stability and reduces noise.

Two-Wire to Four-Wire Gain

The two-wire to four-wire gain, G_{2-4} , can be obtained from (1) and (2) with $V_{RX} = 0$:

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/100}{Z_T/100 + 2R_F}$$

Four-Wire to Two-Wire Gain

The four-wire to two-wire gain, G_{4-2} , is derived from (1), (2) and (3) with $E_L = 0$:

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{Z_T/100 + 2R_F + Z_L}$$

Four-Wire to Four-Wire Gain

The four-wire to four-wire gain, G_{4-4} , is derived from (1), (2) and (3) with $E_L = 0$:

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L + 2R_F}{Z_T/100 + 2R_F + Z_L}$$

Hybrid Function

The PBL 3798/5 SLIC forms a particularly flexible and compact line interface when used together with Siemens Codec Filter circuit (SiCoFi) or other similar programmable CODEC/filter. The SiCoFi allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. The SiCoFi also permits the system controller to adjust transmit and receive gains as well as terminating impedance. Refer to SiCoFi or similar

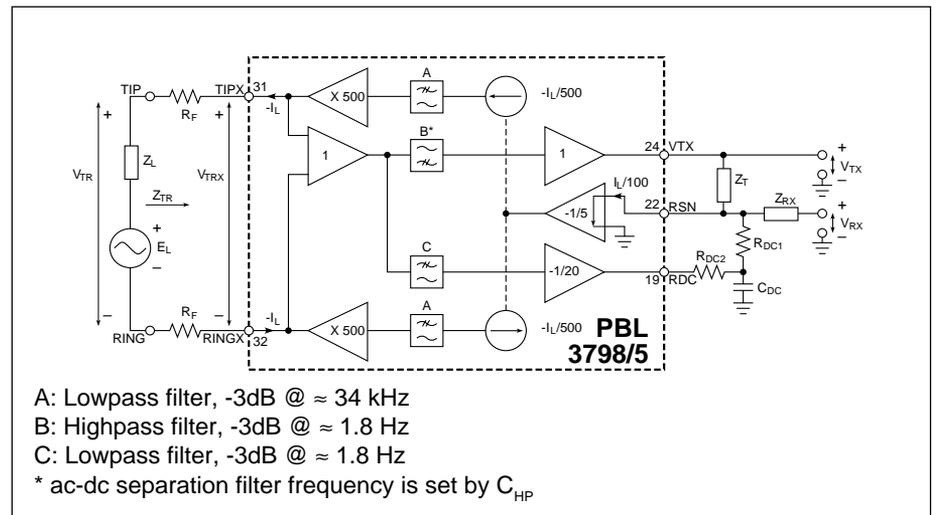


Figure 13. Simplified ac transmission circuit.

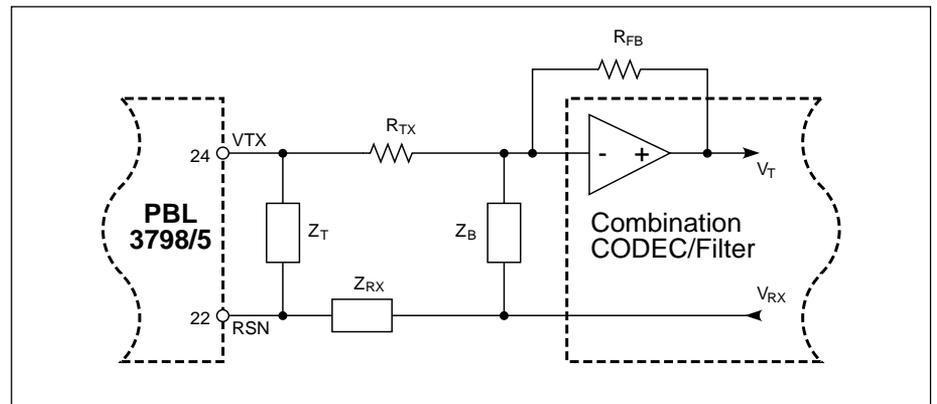


Figure 14. Hybrid function.

programmable CODEC/filter data sheets for design information.

The hybrid function in an implementation utilizing the uncommitted amplifier in a conventional CODEC/filter combination is shown in figure 14. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned at VTX. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel each other by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \quad (E_L = 0)$$

Substituting the four-wire to four-wire

gain expression, G_{4-4} , for V_{RX}/V_{TX} yields the formula for the balance network:

$$Z_B = -R_{TX} \cdot \frac{V_{RX}}{V_{TX}} = R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{Z_T/100 + 2R_F + Z_L}{Z_L + 2R_F}$$

Example: $Z_{TR} = Z_L = 900 \Omega$ (R_L) in series with $2.16 \mu F$ (C_L) $R_F = 40 \Omega$, $R_{TX} = 27.4 \text{ k}\Omega$, $G_{4-2} = -1$. Calculate Z_B .

Using the Z_B formula above:

$$Z_B = \{Z_L = Z_{TR}\} = R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{2Z_L}{Z_L + 2R_F} = \{G_{4-2} = -1\} = R_{TX} \cdot \frac{Z_L}{Z_L + 2R_F} = R_{TX} \cdot \frac{1 + j\omega \cdot R_L \cdot C_L}{1 + j\omega \cdot (R_L + 2R_F) \cdot C_L}$$

A network consisting of R_{B1} in series with the parallel combination of R_B and C_B has the same form as the required balance network, Z_B . Basic algebra yields:

$$R_{B1} = R_{TX} \cdot \frac{R_L}{R_L + 2R_F} = 25.2 \text{ k}\Omega$$

$$R_B = R_{TX} \cdot \frac{2R_F}{R_L + 2R_F} = 2237 \Omega$$

$$C_B = \frac{(R_L + 2R_F)^2 \cdot C_L}{R_{TX} \cdot 2R_F} = 0.95 \mu F$$

Longitudinal Impedance

A feedback loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Therefore longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions well within the SLIC common mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal reference voltage, V_{LoRef} . As shown below, the SLIC appears as 20Ω to ground per wire to longitudinal disturbances. It should be noted, that longitudinal currents may exceed the dc loop current without disturbing the vt transmission. From figure 15 the longitudinal impedance can be calculated:

$$\frac{V_{Lo}}{I_{Lo}} = \frac{R_{Lo}}{100} = 20 \Omega$$

where:

V_{Lo} is the longitudinal voltage

I_{Lo} is the longitudinal current

$R_{Lo} = 2 \text{ k}\Omega$ sets the longitudinal impedance

Capacitors C_{TC} and C_{RC}

The capacitors designed C_{TC} and C_{RC} in figure 12, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the diode and SCR clamps in the overvoltage protection network, before these devices have had time to activate and could damage the SLIC. C_{TC} and C_{RC} short such very fast transients to ground. The recommended value for C_{TC} and C_{RC} is 2200 pF . Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance

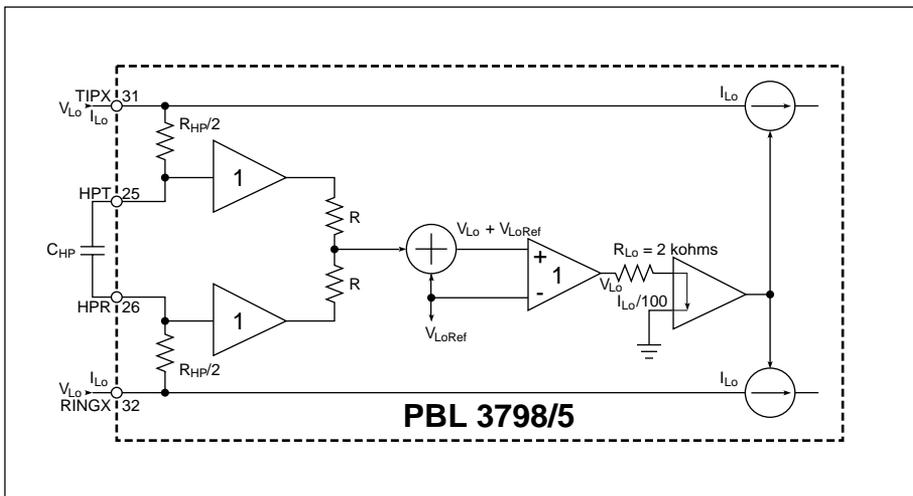


Figure 15. Longitudinal feedback loop. $V_{LoRef} = (V_{Tip} + V_{Ring})/2$ (without any longitudinal voltage component).

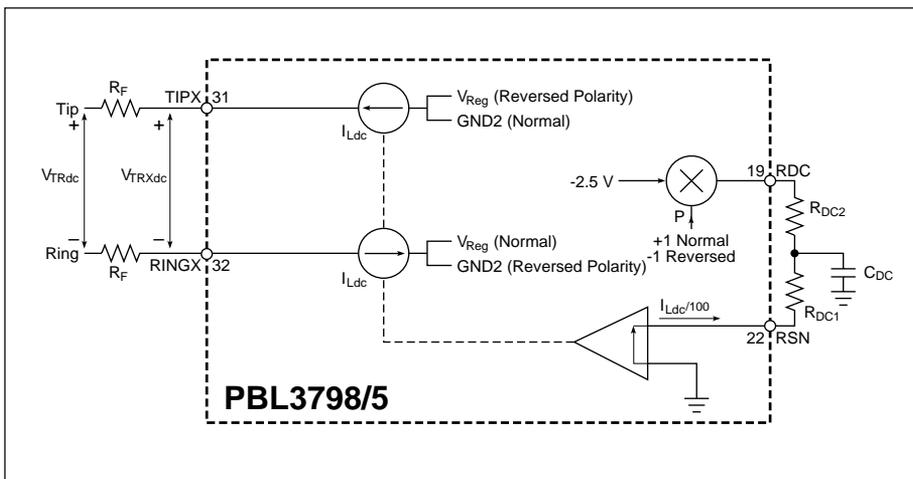


Figure 16. Battery feed.

or return loss. C_{TC} and C_{RC} contribute a metallic impedance of $1/(\pi \cdot f \cdot C_{TC}) \approx 1/(\pi \cdot f \cdot C_{RC})$, a TIPX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

Ac - dc Separation Capacitor

The high pass filter capacitor connected between terminals HPT and HPR provides separation between circuits sensing TIPX-RINGX dc conditions and circuits processing vf signals. The recommended C_{HP} capacitance value of 220 nF will position the 3 dB break point at 1.8 Hz.

Battery Feed

Overview

The PBL 3798/5 SLIC synthesizes a constant current feed system without the disadvantage of high feed circuit power dissipation on short loops. To reduce power dissipation a switch mode regulator efficiently down-converts the battery supply voltage. The down-converted voltage is applied to the line drive amplifiers and is automatically adjusted to be precisely enough to feed the loop current as well as to allow distortion free vf signal transmission.

The magnitude of the constant loop current is set by two external resistors.

The battery feed polarity can be set to either normal or reversed polarity via the SLIC digital control inputs.

To permit the line drive amplifiers to operate without signal distortion even on high resistance or open circuit loops, a saturation guard circuit limits the loop voltage, when the tip to ring dc voltage

approaches the available battery supply voltage.

With the SLIC set to the stand-by state, power is further conserved by limiting the short circuit loop current to 50% of the active state short circuit current.

The following paragraphs describe the battery feed circuit in detail. At the end of this section a paragraph, Battery feed circuit programming procedure, summarizes the few simple calculations necessary to program the battery feed.

**Case 1: SLIC in the Active or Active Polarity Reversal State; $|V_{TRdc}| < V_{SGRef}$
 $|V_{Bat}| > V_{SGRef} + 12V$**

In the active state C3, C2, C1 = 0, 1, 0 and in the active polarity reversal state C3, C2, C1 = 1, 1, 0.

The battery feed control loop is shown in block diagram form in figure 16. For tip to ring dc voltages less than the saturation guard reference voltage, V_{SGRef} (refer to case 2) the following expression is obtained from the block diagram for $R_F = 0$.

$$I_{Ldc} = p \cdot \frac{250}{R_{DC1} + R_{DC2}}$$

where:

I_{Ldc} is the constant dc loop current

R_{DC1} , R_{DC2} are the external constant current programming resistors

$p = 1$ for normal polarity, -1 for reversed polarity

In figure 17, curve segment AB is described by case 1.

Case 2: SLIC in the Active or Active Polarity Reversal State;

$$|V_{TRdc}| > V_{SGRef}, |V_{Bat}| > V_{TRdc} + 12V$$

In the active state C3, C2, C1 = 0, 1, 0 and in the active polarity reversal state C3, C2, C1 = 1, 1, 0.

When the tip to ring dc voltage approaches the V_{Bat} supply voltage, a circuit named saturation guard limits the two wire voltage to a small additional increase beyond the saturation guard threshold, V_{SGRef} . This is to maintain distortion free vf transmission through the line drive amplifiers. The saturation guard feature makes on-hook transmission possible.

The tip to ring voltage at which the saturation guard becomes active, V_{SGRef} can be calculated from

$$V_{SGRef} = \frac{34,1}{1 - \frac{0,676}{R_{SG} + 2,26}}$$

where V_{SGRef} is in volts for R_{SG} in k Ω . R_{SG} is a resistor connected between terminal RSG and -5V.

Note that the RSG terminal is available only on the 44-pin surface mount package. The 32-pin surface mount package have the saturation guard internally set to $V_{SGRef} = 34.1V$.

$R_{SG} = \infty \Omega$ yields $V_{SGRef} = 34.1V$.
 $R_{SG} = 0 \Omega$ yields $V_{SGRef} = 48.6V$.

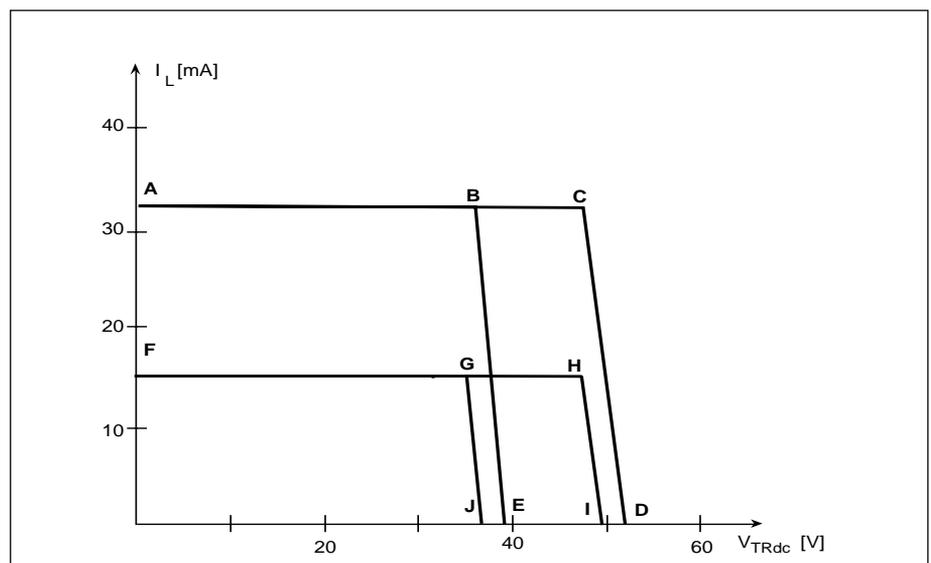
Figur 17. PBL 3798/5 battery feed
 $R_{DC1} = R_{DC2} = 3,9 \text{ k}\Omega$, $I_{Ldc} = 32 \text{ mA}$.

Curve ABE: active state. PBL 3798/5 in 32 pin or 44-pin PLCC with $R_{SG} = \infty \Omega$ and $V_{Bat} = -48V$.

Curve ACD: active state. PBL 3798/5 in 44-pin PLCC with $R_{SG} = 0 \Omega$ and $V_{Bat} = -63V$.

Curve FGJ: stand-by state. PBL 3798/5 in 32-pin or 44-pin PLCC with $R_{SG} = \infty \Omega$ and $V_{Bat} = -48V$.

Curve FHI: stand-by state. PBL 3798/5 in 44-pin PLCC with $R_{SG} = 0 \Omega$ and $V_{Bat} = -63V$.



The loop current, I_{Ldc} , as a function of the loop voltage, V_{TRdc} , for $V_{TRdc} > V_{SGRef}$ is described by

$$I_{Ldc} = \frac{V_{SGRef} - V_{TRdc}}{120} + \frac{250}{R_{DC1} + R_{DC2}}$$

The open circuit voltage is then, for a programmed loop current of 40mA, 38.9V for $R_{SG} = \text{open circuit}$ and 53.4V for $R_{SG} = 0 \Omega$.

In figure 17, PBL 3798 battery feed examples, curve segment CD and BE are described by case 2.

Case 3: SLIC in the stand-by or stand-by polarity reversal state;

$$|V_{TRdc}| < V_{SGRef}, |V_{Bat}| > V_{SGRef} + 12 V$$

The stand-by operating states reduce power dissipation.

The loop feed in the stand-by state ($C3, C2, C1 = 0, 1, 1$) and in the stand-by polarity reversal state ($C3, C2, C1 = 1, 1, 1$) is constant current according to:

$$I_{Ldc} = p \cdot \frac{125}{R_{DC1} + R_{DC2}}$$

In figure 17, PBL 3798/5 battery feed examples, this corresponds to curve segments FG and FH.

Case 4: SLIC in the Stand-By or Stand-By Polarity Reversal State;

$$|V_{TRdc}| > V_{SGRef}, |V_{Bat}| > V_{SGRef} + 12 V$$

In the stand-by state $C3, C2, C1 = 0, 1, 1$ and in the stand-by polarity reversal state $C3, C2, C1 = 1, 1, 1$.

When the tip to ring dc voltage exceeds the saturation guard reference voltage, V_{SGRef} , the loop feed is described by

$$I_{Ldc} = \frac{V_{SGRef} - V_{TRdc}}{120} + \frac{125}{R_{DC1} + R_{DC2}}$$

In figure 17, this corresponds to curve segments HI and GJ.

Case 5: SLIC in the TIPX Open Circuit State.

In the TIPX open circuit state $C3, C2, C1 = 1, 0, 0$. Refer to figure 8. In this state the TIPX terminal is set to a high-impedance state ($> 150 k\Omega$). The RINGX terminal sinks a current ($|I_{LRT0}| > 23 \text{ mA}$) until the V_{Bat} voltage is approached, whereafter the RINGX terminal changes to a constant voltage state and the RINGX current can be calculated from:

$$|I_{LRT0}| = \frac{|V_{Bat} + 4|}{R_{LRGnd}}$$

where;

R_{LRGnd} is the resistor between ground and ring lead.

C_{DC} Capacitor

Refer to the battery feed block diagram, figure 16. The battery feed programming resistors R_{DC1} and R_{DC2} together with capacitor C_{DC} form a low pass filter, which removes noise and vf signals from the battery feed control loop. The recommended 3 db break point

frequency is $160 \text{ Hz} < f_{3dB} < 240 \text{ Hz}$. The C_{DC} capacitance value is then calculated from:

$$C_{DC} = \frac{1}{2\pi \cdot f_{3dB}} \cdot \left[\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}} \right]$$

Note that $R_{DC1} = R_{DC2}$ yields minimum C_{DC} capacitance value.

Switch Mode Regulator

The switch mode regulator down-converts the V_{Bat} supply voltage to a value, which is just enough for the line drive amplifiers to feed the required loop current and maintain transmission quality. Since the voltage conversion efficiency is high and the minimum required voltage drop across the line drive amplifiers is low, a significant power dissipation reduction is realized. A 50 mA constant current feed with 200 Ω line resistance and -48 V battery will have 1.9W dissipated in the line feed circuit. The PBL 3798/5 set up for the same 50 mA constant current feed and with the same 200 Ω line resistance and $V_{Bat} = -48 \text{ V}$, would generate only 0.72 W in the line feed circuits (90% power conversion efficiency), i.e. a 1.18 W or 62.1% reduction in line card power dissipation.

Refer to figure 18 for a block diagram of the switch mode regulator. VBAT is the input voltage, which the regulator converts to VREG with high efficiency. V_{Reg} powers the line drive amplifiers. The switch mode regulator adjusts its V_{Reg} output to be equal to the reference voltage, V_{Ref} . The reference voltage is derived from the TIPX to RINGX dc metallic voltage according to

$$V_{Ref} = -(|V_{TRdc}| + V_{Bias})$$

where V_{Bias} is approximately 12 V.

Since V_{Bias} is the voltage drop across the line drive amplifiers, the SLIC power loss is greatly reduced compared to supplying the amplifiers directly from the V_{Bat} supply.

The battery supply voltage, $|V_{Bat}|$, must be larger than $|V_{Reg}|$, i.e. $|V_{Bat}| \geq |V_{TRdc}| + V_{Bias}$. If this condition is not met, the tip to ring voltage will be limited by the SLIC according to $|V_{TRdc}| = |V_{Bat}| - V_{Bias}$. Although the SLIC continues to function, this mode of operation should be avoided due to increased noise and a much reduced V_{Bat} to transmission ports rejection ratio.

To minimize noise as well as battery feed circuit power dissipation on long

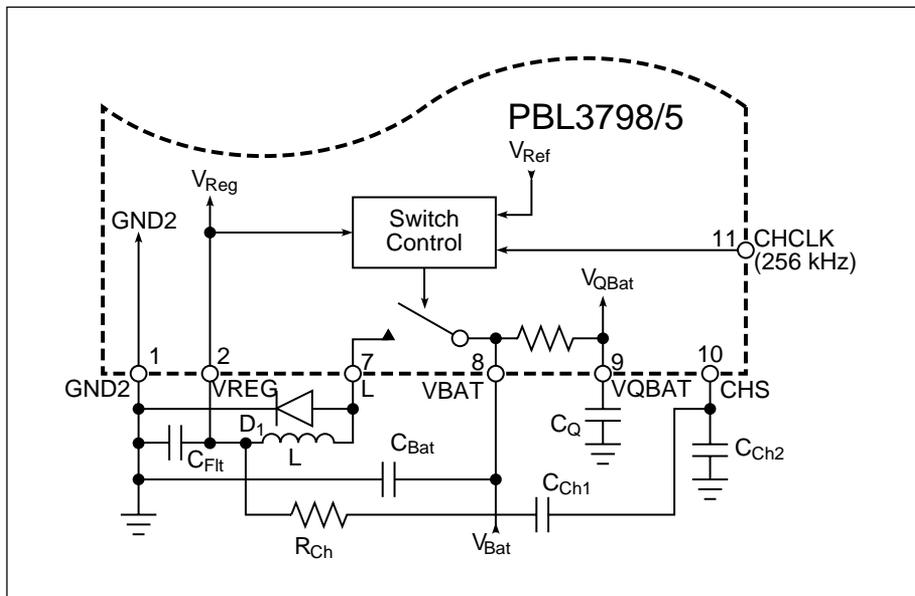


Figure 18. Switch mode regulator.

loops the switch mode regulator is automatically turned off for tip to ring dc voltages exceeding a threshold value of approximately $V_{SGRef} - 1V$. With the regulator disabled, the V_{Bat} supply voltage is passed on to the VREG input without being down-converted.

The inductor, L, should be 1 mH with a series resistance larger than 15 Ω .

A saturated inductor with less than 15 Ω of series resistance may damage the SLIC due to excessive regulator switch current.

C_{Filt} , 0.47 μF , is the regulator output filter capacitor.

The catch diode, D_1 , (e.g.1N4448) must withstand 70 V reverse voltage, conduct an average of 50 mA (150 mA peak) and turn off in less than 10 nsec.

C_{CH1} , C_{CH2} and R_{CH} make up a compensation network for an internal voltage comparator. Values are given in the applications example, figure 12.

The components associated with the switching regulator must be connected via the shortest possible PCB trace lengths. Other circuits should be kept isolated from this area. The L terminal voltage variations are large and very fast. To avoid interference the inductor and the catch diode should be located directly at this terminal. Inductors with closed magnetic path core (e.g. toroid, pot core) will reduce interference originating from the inductor.

Battery Feed Circuit Programming Procedure

Extracting the key elements from the preceding description results in the following step-by-step procedure.

1. Establish the battery feed requirements.

Constant loop current, $I_{Ldc} = ?$

Maximum loop resistance, including fuse resistors R_{F1} and R_{F2} , $R_{LMax} = ?$

Loop resistance, above which it is permissible for the loop feed to change from constant current feed to resistive feed, $R_{LSGRef} = ?$

Loop current at the maximum loop resistance (applies if

$$I_{Ldc} \cdot R_{LMax} > V_{SGRef}, I_{LMin} = ?$$

SLIC supply voltage, $V_{BAT} = ?$

2. Calculate the constant current programming components R_{DC1} and R_{DC2} from

$$R_{DC1} = R_{DC2} = \frac{250}{I_{Ldc}} \cdot \frac{1}{2}$$

3. Calculate C_{DC} from

$$C_{DC} = \frac{1}{2\pi \cdot f_{3dB}} \cdot \left[\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}} \right]$$

where $f_{3dB} \approx 200$ Hz

4. Calculate the saturation guard programming resistor, R_{SG} . PBL 3798 in 32-pin surface mount package:

No RSG terminal provided. V_{SGRef} is internally set to 34.1V. The minimum required battery voltage is $|V_{Batmin}| = V_{SGRef} + 12$ V. For loop voltages greater than V_{SGRef}

$$|V_{Batmin}| = V_{TRdc} + 12$$

PBL 3798 in 44-pin surface mount package:

RSG terminal open circuit:

$$V_{SGRef} = 34.1V.$$

R_{SG} terminal shorted to V_{EE} :

$$V_{SGRef} = 48.6V.$$

For intermediate V_{SGRef} values

calculate R_{SG} according to

$$R_{SG} = - \frac{1,59}{1 + \frac{14,5}{V_{SGRef} - 48,6}}$$

where R_{SG} is in $k\Omega$ for V_{SGRef} in volts.

The minimum required battery voltage is $|V_{Batmin}| = V_{SGRef} + 12$ V. For loop voltages greater than V_{SGRef}

$$|V_{Batmin}| = V_{TRdc} + 12$$

5. Calculate the loop resistance at which the saturation guard becomes active,

$$R_{LSGRef} = \frac{V_{SGRef}}{I_{Ldc}}$$

Confirm compatibility with requirements.

6. If $I_{Ldc} \cdot R_{LMax} > V_{SGRef}$ calculate loop current at maximum loop resistance:

$$I_{Ldc min} = \frac{V_{SGRef} + 120 \cdot \frac{250}{R_{DC1} + R_{DC2}}}{120 + R_{LMax}}$$

Confirm compatibility with requirements.

7. Recommended switch mode regulator component values:

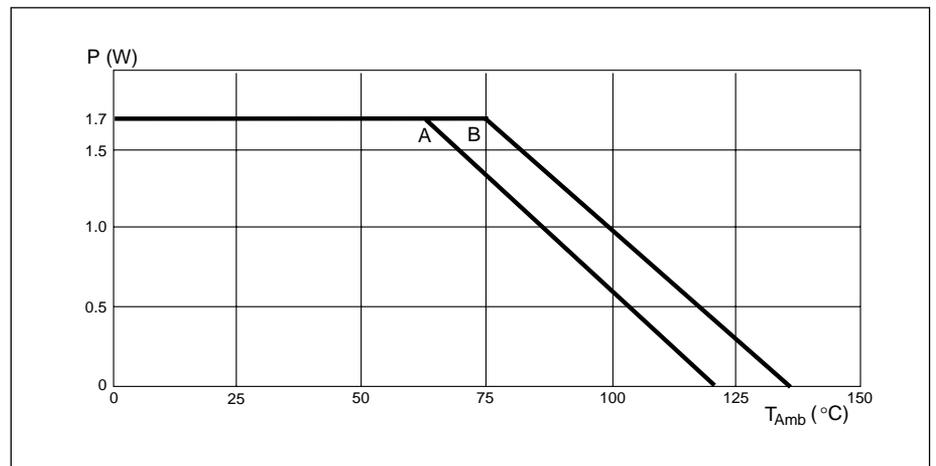
- L = 1 mH ± 10 %;
- C_{Filt} = 0.47 $\mu F \pm 10$ %, 100 V;
- D_1 = 1N4448 (or equivalent),
- R_{CH} = 909 $\Omega \pm 2$ %, 0.25 W;
- C_{CH1} = 0.047 $\mu F \pm 10$ %, 100 V;
- C_{CH2} = 1500 pF ± 10 %, 100 V.

Figure 19. Power derating, 32-pin PLCC.

$$P = \frac{T_j - T_{Amb}}{\Theta_{JA}}$$

P = power,
 T_j = junction temperature,
 T_{Amb} = ambient temperature,
 Θ_{JA} = junction-to-ambient thermal resistance.

Curve A: $T_j = 120^\circ C$, $\Theta_{JA} = 35^\circ C/W$
 Curve B: $T_j = 135^\circ C$, $\Theta_{JA} = 35^\circ C/W$



Loop Monitoring Functions

Overview

The PBL 3798/5 SLIC contains three detectors: the loop current, the ground key and the ring trip detector. These three detectors report their status via the shared DET output. The detector to be connected to the DET output is selected according to the logic states at the control inputs C1, C2, C3 and enable input E1. Enable input E0 sets the DET output to either active or high impedance state.

Loop Current Detector - Active State and Stand-by State

Active state (C3, C2, C1 = 0, 1, 0) and active polarity reversal state (C3, C2, C1 = 1, 1, 0) as well as standby state (C3, C2, C1 = 0, 1, 1) and stand-by polarity

reversal state (C3, C2, C1 = 1, 1, 1).

The loop current value at which the loop current detector changes state is programmable by calculating a value for resistor R_D . R_D connects between terminals RD and VEE.

Figure 20 shows a block diagram for the loop current detector. The two-wire interface produces a current, I_{RD} , flowing out of pin RD:

$$I_{RD} = 0.5 \cdot \frac{|I_{LT} - I_{LR}|}{300} = \frac{|I_L|}{300}$$

where I_{LT} and I_{LR} are currents flowing into the TIPX and RINGX terminals and I_L is the loop current. The voltage generated across the programming resistor R_D by I_{RD} is applied to an internal comparator with hysteresis. The comparator reference voltage for transition on-hook to off-hook is 1.55 V.

The reference voltage for a transition off-hook to on-hook is 1.37 V. A logic low level results at the DET output, when the comparator reference voltage is exceeded.

For a specified on-hook to off-hook loop current threshold, I_{LThOff} , R_D is calculated from

$$R_D = \frac{1.55 \cdot 300}{|I_{LThOff}|}$$

The calculated R_D value corresponds to an off-hook to on-hook loop current threshold, I_{LThOn} , of

$$|I_{LThOn}| = \frac{1.37 \cdot 300}{R_D}$$

Loop Current Detector - Tip Open Circuit State

Tip open circuit state (C3, C2, C1 = 1, 0, 0)

In the tip open circuit state the loop current detector function is similar to the active state, but the RD terminal current, I_{RD} , is calculated from

$$I_{RD} = \frac{I_{LR}}{600}$$

The detector is triggered at a ring lead threshold current $I_{LRThOffTo}$ with the R_D resistance value set to

$$R_D = \frac{1.55 \cdot 600}{I_{LRThOffTo}}$$

The ring lead current must be reduced to less than

$$I_{LRThOnTo} = \frac{1.37 \cdot 600}{R_D}$$

for the detector to return to its non-triggered state.

Loop Current Detector - Filter Capacitor

It is recommended to filter the signal at the RD pin with a capacitor C_D connected between terminal RD and ground.

A suggested value for C_D is:

$$C_D = \frac{1}{2\pi \cdot R_D \cdot f_{3dB}}, \text{ where } f_{3dB} = 500 \text{ Hz}$$

Ground Key Detector

Refer to figure 20 for a block diagram of the ground key detector. The ground key detector examines the difference between TIPX and RINGX currents. When the longitudinal current from ground exceeds an internally set threshold value of nominally 8 mA, the

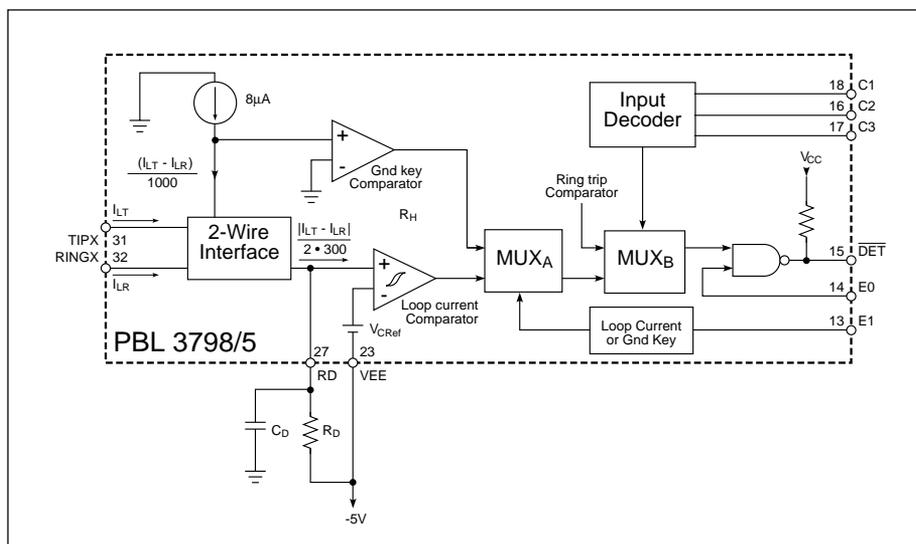


Figure 20. Loop current and ground key detector.

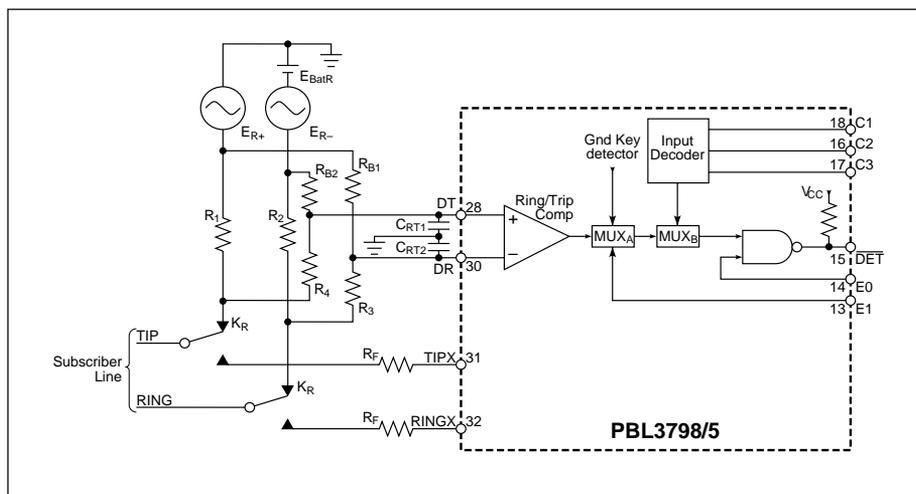


Figure 21. Ring trip network, balanced ringing.

detector triggers and sets the $\overline{\text{DET}}$ output to a logic low level. The E1 enable input must be set to logic high level to gate the ground key detector to the $\overline{\text{DET}}$ output.

The Electrical characteristics table specifies the threshold level as a function of longitudinal resistance to ground.

The ground key detector threshold is pre-programmed and cannot be changed by external components.

Ring Trip Detector

Ring trip detection is accomplished by monitoring the two-wire line for presence of dc current while ringing is applied.

When the subscriber goes off-hook with ringing applied, dc loop current starts to flow. The comparator in the SLIC with inputs DT and DR detects this current flow via an interface network. The result of the comparison is presented at the $\overline{\text{DET}}$ output. The ring trip comparator is automatically connected to the $\overline{\text{DET}}$ output, when the SLIC control inputs are set to the ringing state (C3, C2, C1 = 0, 0, 1). When off-hook during ringing is detected, the line card or system controller will proceed to disconnect the ringing source (software ringtrip) by resetting the control input logic states. Alternatively, the DET output may be monitored by circuits on the line card, which perform the ringtrip function (hardware ringtrip).

The ringing source may be balanced or unbalanced, superimposed on the V_{Bat} supply voltage. The unbalanced ringing source may be applied to either the tip lead or the ring lead with return on the

other wire. A ring relay, energized by the SLIC ring relay driver, connects the ringing source to tip and ring. For unbalanced ringing systems the loop current sensing resistor may be placed either in series with the ringing generator or in series with the return lead to ground.

Figures 21 and 22 show examples of balanced and unbalanced ringing systems. For either ringing system the ringtrip detection function is based on a polarity change at the inputs DT and DR of the ringtrip comparator.

In the unbalanced case the dc voltage drop across resistor R_{RT} is zero as long as the telephone remains on-hook. With the telephone off-hook during ringing, dc loop current will flow, causing a voltage drop across R_{RT} . The R_{RT} voltage is applied to the comparator input DT via resistor R_3 . R_4 shifts the voltage level to be within the comparator common mode range. C_{RT} removes the ac component of the ringing signal. R_1 and R_2 establish a bias voltage at comparator input DR, which is more negative than DT when the telephone is on-hook and is more positive than DT when the telephone goes off-hook during ringing.

Complete removal of the ringing signal ac component at the DT input may not be necessary. Some residual ac component at the DT input may under certain operating conditions cause the $\overline{\text{DET}}$ output to toggle between the on-hook and off-hook states at the ringing frequency. However, with the telephone off-hook the $\overline{\text{DET}}$ output will be at logic

low level for more than half the time. Therefore, by sampling the $\overline{\text{DET}}$ output, a software routine can discriminate between on-hook and off-hook through examination of the duty cycle. Full removal of the ringing frequency from the DT input while maintaining ringtrip within required time limits (approximately < 100 ms) usually mandates a second order filter rather than the first order shown in figure 22. The software approach minimizes the number of line card components.

In the balanced ringing system shown in figure 21, R_1 and R_2 are the loop current sensing resistors. With the telephone on-hook, no dc loop current flows to cause a dc voltage drop across resistors R_1 and R_2 . Voltage dividers R_{B2} , R_4 and R_{B1} , R_3 bias the ringtrip comparator input DT to be more positive than DR. With the telephone off-hook during ringing dc loop current will flow, causing a voltage drop across resistors R_1 and R_2 , which in turn will make comparator input DT more negative than DR, setting the $\overline{\text{DET}}$ output to logic low level, indicating ringtrip condition. Capacitors C_{RT1} and C_{RT2} filter the ring voltage at the comparator inputs. For 20 Hz ringing it is suitable to calculate these capacitors for a time constant of $T = 50$ ms, i. e.

$$C_{\text{RT1}} = T \cdot \left(\frac{1}{R_{\text{B2}}} + \frac{1}{R_4} \right)$$

Detector Output, $\overline{\text{DET}}$

The loop current detector, ground key detector and ringtrip comparator share a

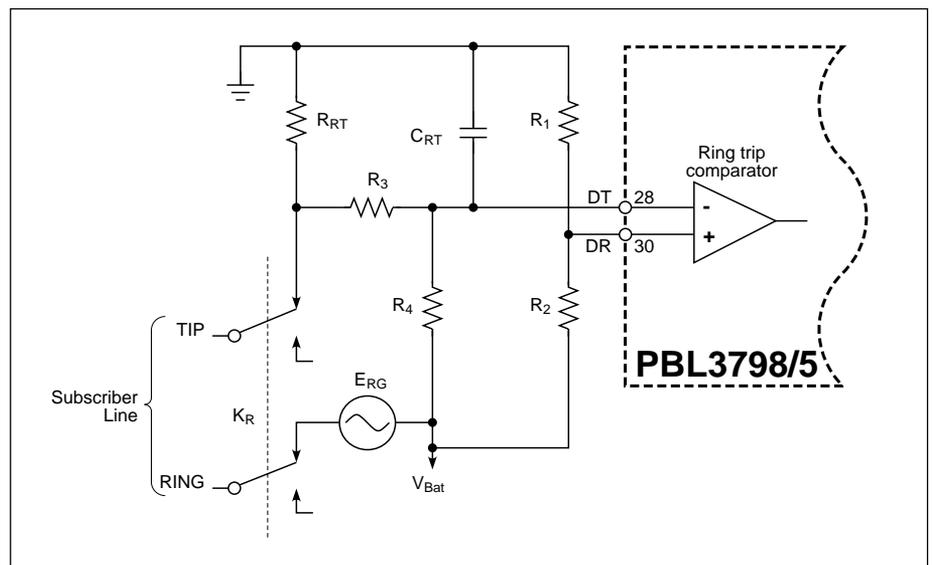


Figure 22. Ring trip network, unbalanced ringing.

common output, $\overline{\text{DET}}$. The $\overline{\text{DET}}$ output is open collector with internal pull-up resistor to V_{CC} . Via control inputs C1 through C3 and enable input E1 one of the three detectors is selected to be connected to the $\overline{\text{DET}}$ output. With enable input E0 set to logic high level the $\overline{\text{DET}}$ output is activated. In the $\overline{\text{DET}}$ active state a logic low level indicates a triggered detector condition and a logic high level reports a non-triggered detector. With E0 set to logic low level, the $\overline{\text{DET}}$ output is set to its high impedance state, i.e. connected to V_{CC} via the internal pull-up resistor.

Relay Drivers

The PBL 3798/5 SLIC contains two identical drivers for test and ring relays.

The drivers are pnp transistors in open collector configuration, sourcing up to 80 mA from the V_{CC} supply. Each driver has an internal inductive kick-back clamp diode. The relay coil may be connected to negative supply voltages ranging from ground to V_{Bat} . Control input C4 activates the test relay driver. Control inputs C1, C2 and C3 are used to operate the ring relay.

Control Inputs

Overview

The PBL 3798/5 SLIC has four TTL compatible control inputs, C1 through C4. A decoder in the SLIC interprets the control input logic conditions and sets up the commanded operating state. C1 through C3 allow for eight operating

states. The C4 control input acts directly on the test relay driver.

The control inputs interface with programmable CODEC/filters, e.g. SLAC, SiCoFi, Combo II without any interface components. Via serial I/O ports on the programmable CODEC/filter devices a microprocessor can communicate with the SLIC. In designs utilizing conventional CODEC/filters without control latches, the line card logic must contain the necessary latches for inputs C1 through C4.

Table 1 contains a summary description of the Control Inputs.

Test Relay Control (C4)

With C4 set to logic low level the test relay driver (TESTRLY) is activated. The active driver can source up to 80 mA from the V_{CC} supply. C4 set to logic high level causes the relay driver to be de-energized. The test relay driver is controlled exclusively by C4 and is independent of the C1, C2 and C3 logic levels.

Open Circuit State (C3, C2, C1 = 0, 0, 0)

In the Open Circuit State both the TIPX and RINGX power amplifiers present a high impedance to the line. The loop current and ground key detectors are not active in this state.

Ringling State (C3, C2, C1 = 0, 0, 1)

The ring relay driver (RINGRLY) is activated and the ring trip comparator is connected to the detector output ($\overline{\text{DET}}$). The TIPX and RINGX terminals are in the high impedance state and signal transmission is inhibited.

Active State (C3, C2, C1 = 0, 1, 0)

TIPX is the terminal closest to ground potential and sources loop current, while RINGX is the more negative terminal and sinks loop current. Signal transmission is normal and the loop current or ground key detector is gated to the $\overline{\text{DET}}$ output according to enable input E1 logic state.

Stand-by State (C3, C2, C1 = 0, 1, 1)

In the stand-by state the short circuit loop current is reduced to:

$$I_{Ldc} = 125 / (R_{DC1} + R_{DC2}).$$

The loop current or ground key detector is connected to the $\overline{\text{DET}}$ output in accordance with the E1 input logic state.

State #	C4 Note 1	C3	C2	C1	Operating State	Active detector Note 2
1	X	0	0	0	Open circuit	Ring trip comparator
2	X	0	0	1	Ringling	Ring trip comparator
3	X	0	1	0	Active	Loop current or ground key
4	X	0	1	1	Stand-by	Loop current or ground key
5	X	1	0	0	Tip open	Loop current, Note 3
6	X	1	0	1	Reserved	None
7	X	1	1	0	Active polarity reversal	Loop current or ground key
8	X	1	1	1	Stand-by polarity reversal	Loop current or ground key

Notes

- Control input C4 logic state (X) affects only the test relay driver and does not change the SLIC operating state. C4 at logic low level activates the test relay driver. C4 at logic high level turns the test relay driver off.
- Enable input E1 must be set to select between loop current and ground key detector.
- The ground key detector is not functional in the tip open circuit state

Table 1. PBL 3798/5 operating states.

Enable state #	E0	E1	$\overline{\text{DET}}$ output state	Active detector
1	0	X	High impedance	None
2	1	0	Active	Loop current or ringtrip. Note 1
3	1	1	Active	Ground key

Notes

- The loop current detector or the ring trip comparator is selected via C3, C2, C1 (state # 2 selects the ringtrip comparator).

Table 2. Enable inputs E0 and E1.

TIPX Open Circuit State (C3, C2, C1 = 1, 0, 0)

The TIPX power amplifier presents a high impedance to the line. The RINGX terminal is active and sinks current. The $\overline{\text{DET}}$ current detector is connected to the $\overline{\text{DET}}$ output for enable input $E1 = 0$. The detection threshold for the on-hook to off-hook transition is $I_{\text{LRTHOFFTO}} = (1.55 \cdot 600) / R_{\text{D}}$. For $E1 = 1$ the ground key detector is connected to the $\overline{\text{DET}}$ output. Note that the ground key detector is not functional in the tip open circuit state.

Reserved State (C3, C2, C1 = 1, 0, 1)

This state has no assigned function.

Active Polarity Reversal State (C3, C2, C1 = 1, 1, 0)

TIPX and RINGX polarity is reversed from the Active State: RINGX is the terminal closest to ground and sources loop current while TIPX is the more negative terminal and sinks current. Polarity reversal transition time is 4 msec. The loop current or ground key detector is connected to the $\overline{\text{DET}}$ output in accordance with the $E1$ input logic state. Signal transmission is normal.

Stand-by Polarity Reversal State (C3, C2, C1 = 1, 1, 1)

Polarity Reversal as described under state C3, C2, C1 = 1, 1, 0 and Stand-by as described under state C3, C2, C1 = 0, 1, 1.

Enable Inputs

The 32-pin and 44-pin surface mount package version of the PBL 3798/5 SLIC has two TTL compatible enable inputs, $E0$ and $E1$.

$E0$ sets the $\overline{\text{DET}}$ output to active state, when at logic high level and to high impedance state when at logic low level. $E1$ selects the loop current detector to be gated to the $\overline{\text{DET}}$ output, when at logic low level and the ground key detector when at logic high level.

Table 2 summarizes the above description of the Enable Inputs.

Overvoltage Protection

The PBL 3798 SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and

transient voltages that may be applied to the SLIC. The circuit shown in figure 12 utilizes series resistors together with a programmable overvoltage protector (e.g. Texas Instrument TISP PBL 1), serving as a secondary protection. The protector network in figure 12 is designed to meet requirements in ITU-T k20, table 1. The TISP PBL 1 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i.e. the battery voltage, V_{Bat}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by an internal diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition, clamping the overvoltage close to ground.

A gate decoupling capacitor, C_{TISP} is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. Without the capacitor even the low inductance in the track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_{F} serve the dual purposes of being non-destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross. Ericsson Components AB offers a series of thick film resistors networks (e.g. PBR 51-series and PBR 53-series) designed for this application.

Also devices with a built in resettable fuse function is offered (e.g. PBR 52-series) including positive temperature coefficient (PTC) resistors, working as resettable fuses, in series with thick film resistors. Note that it is important to always use PTC's in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore the ability to protect the SLIC will be reduced.

If there is a risk overvoltages on the V_{Bat} terminal on the SLIC, then this terminal should also be protected.

Over-Temperature Protection

A ring lead to ground short circuit fault condition, as well as other improper operating modes, may cause excessive SLIC power dissipation. If junction temperature increases beyond 140°C, the temperature guard will trigger, causing the SLIC to be set to a high impedance state. In this high impedance state power dissipation is reduced and the junction temperature will return to a safe value. Once below 130°C junction temperature the SLIC is returned back to its normal operating mode and will remain in that state assuming the fault condition has been removed.

Power-Up Sequence

The voltage at pin VBAT sets the substrate voltage, which must at all times be kept more negative than the voltage at any other terminal. This is to maintain correct junction isolation between devices on the chip. To prevent possible latch-up, the correct power-up sequence is to connect ground and V_{Bat} , then other supply voltages and signal leads. Should the V_{Bat} supply voltage be absent, a diode with a 2 A current rating, connected with its cathode to V_{EE} and anode to VQBAT, ensures the presence of the most negative supply voltage at the VQBAT pin.

The V_{Bat} voltage should not be applied at a faster rate than $dV_{\text{Bat}}/dt = 4 \text{ V}/\mu\text{sec}$, e.g. a time constant formed by a 5.1 ohm resistor in series with the VBAT pin and a 0.47 microfarad capacitor from the VBAT pin to ground. One resistor may be shared by several SLICs.

Printed Circuit Board Layout

Care in PCB layout is essential for proper function. The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN terminal. A ground plane surrounding the RSN pin is advisable. The C_{HP} capacitor should be placed close to terminals HPT and HPR to avoid unwanted disturbances.

The switch mode regulator components must be located near the pins to which they connect. It is particularly important that the catch diode and the inductor are connected via shortest possible trace lengths.

Ground terminals GND1 and GND2 should be connected via a direct PCB trace at the device location.

Ordering Information

Package	Temp. Range	Part No.
PLCC 32 pin	-20 to 70°C	PBL 3798/5RN
PLCC 44 pin	-20 to 70°C	PBL 3798/5QN

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