ERICSSON

September 1997

PBL 3767, PBL 3767/6 Subscriber Line Interface Circuit

Description

The PBL 3767 Subscriber Line Interface Circuit (SLIC) is a monolithic integrated circuit, manufactured in 75 V bipolar technology. The PBL 3767 SLIC facilitates the design of cost effective, high performance on-premises (ONS) analog line interface cards for PABX systems and terminal adapters. Small package size and few required external components result in a miniaturized design.

The PBL 3767 programmable, resistive battery feed system with short loop current limiting can operate with battery supply voltages between -24 V and -58 V.

The SLIC incorporates loop current and ring trip detection functions as well as a ring relay driver.

The two- to four-wire and four- to two-wire voice frequency (vf) signal conversion, i.e. the hybrid function, is provided by the SLIC in conjunction with either a conventional or a programmable CODEC/filter.

The PBL 3767 package is a 22 pin, plastic dual-in-line (batwing) or a 28-pin, plastic j-leaded chip carrier (PLCC).
The differences between PBL 3767 and PBL 3767/6 are the specifications for balance, output offset voltage, and insertions loss.

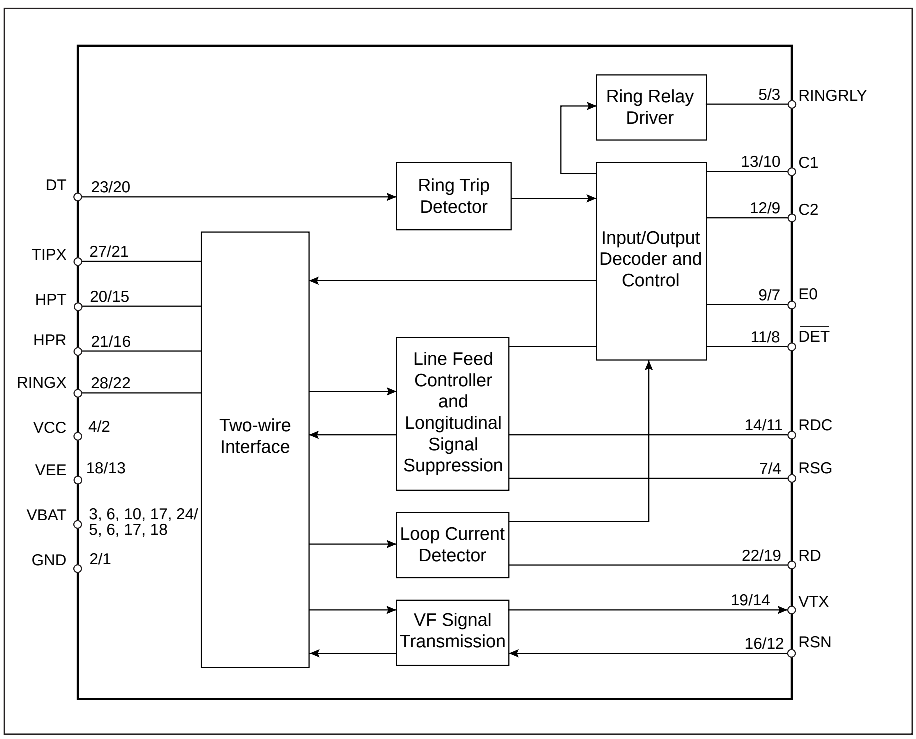
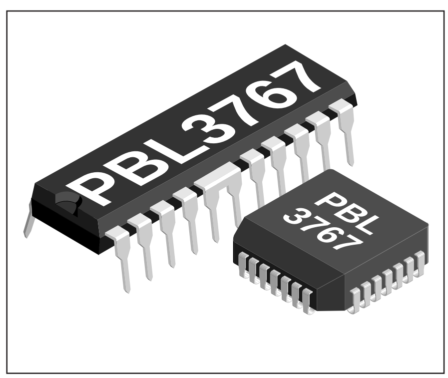


Figure 1. Block diagram. Pin numbers PLCC/DIP.

Key Features

- Low cost
- Few external components
- Programmable, resistive battery feed with short loop current limiting
- Line feed characteristics independent of battery supply variations
- -24 V to -58 V battery supply voltage range
- Detectors
  – programmable loop current detector
  – ring trip detector
- Ring relay driver
- Hybrid function with conventional or programmable CODEC/filters
- Line terminating impedance, complex or real, set by a simple external network or controlled by a programmable CODEC/filter
- Low on-hook power dissipation: 20 mW @ -28 V (35 mW @ -48 V)
- Tip-ring open circuit state for subscriber loop power denial
- Idle noise typ. -83 dBmp, typ. 7 dBrnC
- On-hook transmission



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature and humidity				
Storage temperature range	T_{Stg}	-60	+150	°C
Operating temperature range	T_{Case}	-10	+110	°C
Operating junction temperature	T_J	-10	+140	°C
Storage humidity	R_H	5	95	% RH
Power supply, -10 °C < T_{Amb} < 80 °C				
V_{CC} with respect to GND	V_{CC}	-0.5	6.5	V
V_{EE} with respect to GND	V_{EE}	-6.5	0.5	V
V_{Bat} with respect to GND	V_{Bat}	-70	V_{EE}+0,7	V
Power dissipation				
Continuous power dissipation at T_{Amb} ≤ 70 °C	P_D		1.5	W
Peak power dissipation at T_{Amb} = 70°C, t < 10 ms, t_{Rep} > 10 sec.	P_{DP}		4	W
Relay driver				
Ring relay supply voltage	V_{RRly}	V_{Bat}	0	V
Ring relay current	I_{RRly}		50	mA
Ring trip comparator				
Input voltage	V_{DT}	V_{Bat}	0	V
Input current	I_{DT}	-2	2	mA
Digital inputs, outputs (C1, C2, E0, $\overline{DET}$)				
Input voltage	V_{ID}	0	V_{CC}	V
Output voltage ($\overline{DET}$ disabled)	V_{OD}	0	V_{CC}	V
Output current ($\overline{DET}$ enabled)	I_{OD}		5	mA
TIPX and RINGX terminals, V_{Bat} = -50V				
TIPX or RINGX voltage, continuous (Note 1)	V_T, V_R	V_{Bat}	0.5	V
TIPX or RINGX, pulse = t_ω < 10 ms, t_{Rep} > 10 s (Notes 2, 3)	V_T, V_R	V_{Bat} - 20	5	V
TIPX or RINGX, pulse = t_ω < 1 µs, t_{Rep} > 10 s (Notes 2, 3)	V_T, V_R	V_{Bat} - 40	10	V
TIP or RING, pulse = t_ω < 250 ns, t_{Rep} > 10 s (Notes 2, 3)	V_T, V_R	V_{Bat} - 70	15	V
TIPX or RINGX Current				
Active	I_{Ldc} + I_{Lodc}		80	mA
Stand-by	I_{Ldc}		25	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case temperature	T_{Case}	0	90	°C
V_{CC} with respect to ground	V_{CC}	4.75	5.25	V
V_{EE} with respect to ground	V_{EE}	-5.25	-4.75	V
V_{Bat} with respect to ground (Note 4)	V_{Bat}	-58	-24	V

Notes

1. With a diode (D_2) connected in series with the V_{Bat} supply, as shown in figure 11, -70 V may be continuously applied to the TIPX or RINGX lead.
2. These voltage ratings require a diode (D_2) to be installed in series with the V_{Bat} supply as shown in figure 11.
3. V_T and V_R are referenced to ground. t_ω is the pulse width of a rectangular test pulse and t_{rep} is the pulse repetition rate.
4. -24 V < V_{Bat} < -21 V may be used in applications requiring maximum vf signal amplitudes less than 3 V_{pk} (8.75 dBm, 600 ohms).

Electrical Characteristics

0 °C < T_{Amb} < 70 °C, V_{CC} = +5 V ±5 %, V_{EE} = -5 V ±5 %, V_{Bat} = -48 V, R_{SG} = 0 ohm , R_{DC} = 20 kohms, R_D = ∞, Z_L = 600 ohms, C_{HP} = 33 nF, C_{DC} = 3.3 µF unless otherwise specified.

Parameter	Ref Fig.	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	2	Z_L = 600 ohms, 1% THD, Note 1	3.1			V_{Pk}
Input impedance, Z_{TRX}		Note 2				
Longitudinal impedance, Z_{LoT}, Z_{LoR}		f < 100 Hz		25	40	ohm/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		active state, C2, C1 = 1, 0		20		mA_{pk}/wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985				
		0.2 kHz ≤ f ≤ 3 kHz				
PBL 3767			53	58		dB
PBL 3767/6			48	58		dB
Longitudinal to metallic balance, B_{LME}	3	$B_{LME} = 20 \cdot \log \frac{\lvert E_{Lo}\rvert}{\lvert V_{TR}\rvert}$				
		0.05kHz ≤ f ≤ 3.4kHz				
PBL 3767			53	58		dB
PBL 3767/6			48	58		dB
Longitudinal to four-wire balance, B_{LFE}	3	$B_{LFE} = 20 \cdot \log \frac{\lvert E_{Lo}\rvert}{\lvert V_{TX}\rvert}$				
		0.05kHz ≤ f ≤ 3.4kHz				
PBL 3767			53	58		dB
PBL 3767/6			48	58		dB
Metallic to longitudinal balance, B_{MLE}	4	$B_{MLE} = 20 \cdot \log \frac{\lvert E_{TR}\rvert}{\lvert V_{Lo}\rvert}$, $E_{RX} = 0$				
		0.2kHz ≤ f ≤ 3.4kHz				
PBL 3767			50	55		dB
PBL 3767/6			48	55		dB
Four-wire to longitudinal balance, B_{FLE}	4	$B_{FLE} = 20 \cdot \log \frac{\lvert E_{RX}\rvert}{\lvert V_{Lo}\rvert}$, E_{TR} source removed				
		0.2kHz ≤ f ≤ 3.4kHz	40	55		dB

Figure 2. Overload level, V_{TRO}, two-wire port.

$\frac{1}{\omega C} \ll R_L$, R_L = 600 ohms,

R_T = 600 kohms, R_{RX} = 300 kohms

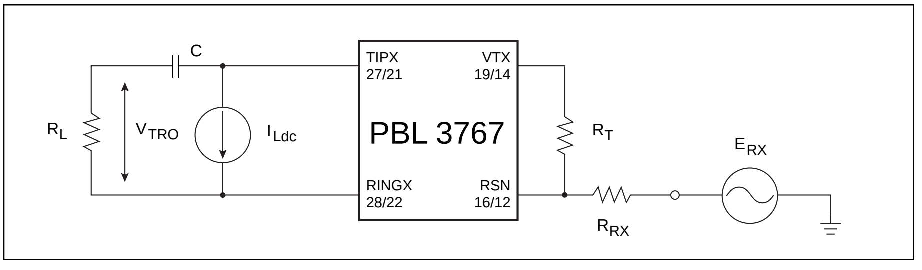
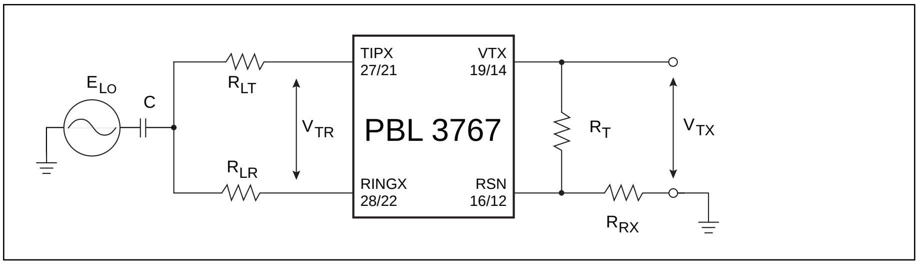


Figure 3. Longitudinal to metallic (B_{LME}) and longitudinal to four-wire (B_{LFE}) balance.

$\frac{1}{\omega C} \ll$ 150 ohms, $R_{LR} = R_{LT}$ = 300 ohms,

R_T = 600 kohms, R_{RX} = 300 kohms



Parameter	Ref Fig.	Conditions	Min	Typ	Max	Unit
Two-wire return loss, r		$r = 20 \cdot \log \frac{\lvert Z_{TRX} + Z_L \rvert}{\lvert Z_{TRX} - Z_L \rvert}$				
		$Z_{TRX} \approx Z_L$ = nom. 600Ω, Note 3				
		0.2 kHz ≤ f ≤ 0.5 kHz	25	30		dB
		0.5 kHz ≤ f ≤ 1.0 kHz	27	32		dB
		1.0 kHz ≤ f ≤ 3.4 kHz	23	25		dB
TIPX idle voltage, V_{Ti}		active, $I_L = 0$		-5		V
		stand-by, $I_L = 0$		0		V
RINGX idle voltage, V_{Ri}		active, $I_L = 0$		-43		V
		stand-by, $I_L = 0$		-48		V
Four-wire transmit port (VTX)						
Overload level, V_{TXO}	5	Load impedance < 20 kohms, 1% THD, Note 4		3.1		V_{Pk}
Output offset voltage, ΔV_{TX}						
PBL 3767			-40		+40	mV
PBL 3767/6			-55		+55	mV
Output impedance, z_{TX}		0.2 kHz < f < 3.4 kHz		<5.0	20	ohm
Four-wire receive port (RSN)						
RSN dc voltage, V_{RSN}		$I_{RSN} = 0$		0		V
RSN impedance, z_{RSN}		0.3 kHz < f < 3.4 kHz		<5	20	ohm
RSN current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		0.3 kHz < f < 3.4 kHz		1000		ratio
Frequency response						
Two-wire to four-wire, g_{2-4}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBu, 1.0 kHz. $E_{RX} = 0$ V	-0.1	0	+0.1	dB
Four-wire to two-wire, g_{4-2}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBu, 1.0 kHz. $E_L = 0$ V	-0.1	0	+0.1	dB
Four-wire to four-wire, g_{4-4}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBu, 1.0 kHz. $E_L = 0$ V	-0.1	0	+0.1	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 5				
PBL 3767			-0.20	0	+0.20	dB
PBL 3767/6			-0.25	0	+0.25	dB
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Notes 5, 6				
PBL 3767			-0.20	0	+0.20	dB
PBL 3767/6			-0.25	0	+0.25	dB
Four-wire to four-wire, G_{4-4}	6	0 dBm, 1.0 kHz, Notes 5, 6	-0.3	0	+0.3	dB

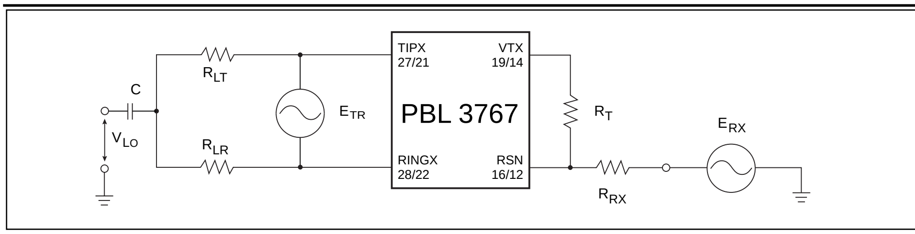


Figure 4. Metallic to longitudinal (B_{MLE}) and four-wire to longitudinal (B_{FLE}) balance.

$\frac{1}{\omega C} \ll 150$ ohms, $R_{LR} = R_{LT} = 300$ ohms,

$R_T = 600$ kohms, $R_{RX} = 300$ kohms

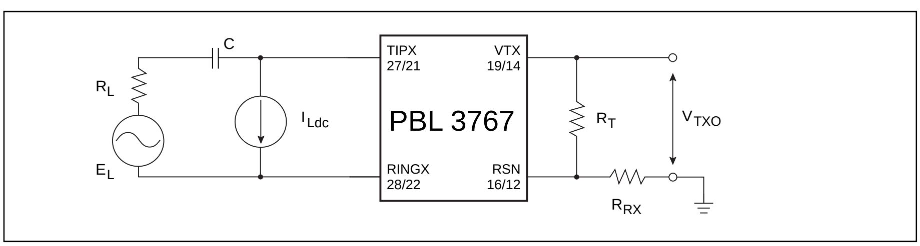


Figure 5. Overload level, V_{TXO}, four-wire transmit port.

$\frac{1}{\omega C} \ll R_L$, $R_L = 600$ ohms,

$R_T = 600$ kohms, $R_{RX} = 300$ kohms

Parameter	Ref Fig.	Conditions	Min	Typ	Max	Unit
Gain tracking						
Two-wire to four-wire	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +7 dBm	-0.15	±0.03	+0.15	dB
		-55 dBm to -40 dBm		±0.03		dB
Four-wire to two-wire	6	Ref. -10 dBm, 1.0 kHz, Note 8				
		-40 dBm to +7 dBm	-0.15	±0.03	+0.15	dB
		-55 dBm to -40 dBm		±0.03		dB
Noise						
Idle channel noise at two-wire (TIPX-RINGX) or four-wire (VTX) port		Note 9				
		Psophometrical weighting		-83	-78	dBmp
		C-message weighting		7	12	dBrnC
Harmonic distortion						
Two-wire to four-wire, Four-wire to two-wire		0.3 kHz < f < 3.4 kHz 0 dBm, 1.0 kHz test signal		-65	-54	dB
Battery feed characteristics						
Apparent battery voltage, E_{Bat}				50		V
Conversion factor, K_1			48	50	52	ratio
Feed resistance (R_{Feed}) to programming resistance (20 kΩ $+R_{DC}$)		$R_{Feed} = \frac{20 \cdot 10^3 + R_{DC}}{K_1}$				
Stand-by state loop current, I_L, tolerance range		Stand-by state, C2, C1 = 1, 0 $I_L = \frac{\lvert V_{Bat}\rvert - 3}{R_L + 1800}$ V_{Bat} tol. ±5%, T_{Amb} = 25 °C	$0.75 \cdot I_L$	I_L	$1.25 \cdot I_L$	A
Loop current detector						
On-hook to off-hook threshold, I_{LThOff}		$R_D = \infty$, Note 10		8.0		mA
Off-hook to on-hook threshold, I_{LThOn}		$R_D = \infty$, Note 10		7.3		mA
Detector threshold hysteresis, ∂I_{LTh}				0.7		mA
Loop current detector conversion factor On-hook to off-hook, K_{LThOff}		$I_{LThOff} = K_{LThOff} \cdot \left[\frac{1}{R_D} + \frac{1}{62500}\right]$ Note 11	375	500	660	V
Loop current detector conversion factor off-hook to on-hook, K_{LThOn}		$I_{LThOn} = K_{LThOn} \cdot \left[\frac{1}{R_D} + \frac{1}{62500}\right]$ Note 11		455		V
Ring trip detector						
Offset voltage, ΔV_{DTR}		Source resistance, R_S = 0	-25		25	mV
Input bias current, I_{DT}		$V_{Bat} < V_{DT} < 0$ V	-300	-100		nA
Input common mode range, V_{DT}			$V_{Bat}+1$		-2	V
Ring relay driver						
On-state voltage, V_{RRly}		I_{RRly} = 25 mA	-0.5	-0.2		V
Off state leakage current, I_{RRly}		$V_{Bat} < V_{RRly} < 0$			10	µA

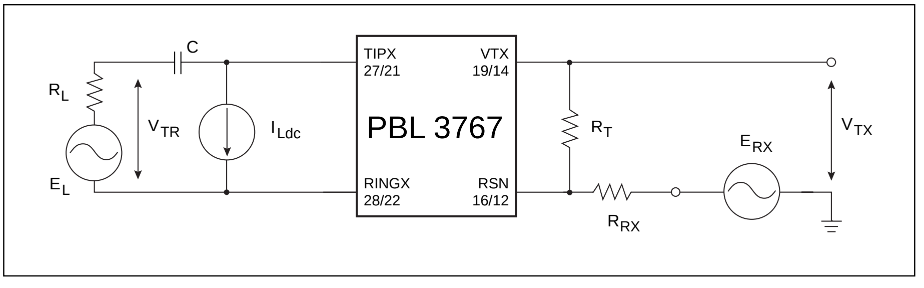


Figure 6. Frequency response, insertion loss, gain tracking.

$\frac{1}{\omega C} \ll R_L$, R_L = 600 ohms,

R_T = 600 kohms, R_{RX} = 300 kohms

Parameter	Ref. Fig.	Conditions	Min	Typ	Max	Unit
Digital inputs (C1, C2, E0)						
Input low voltage, V_{IL}			0		0.8	V
Input high voltage, V_{IH}			2.0		V_{CC}	V
Input low current, I_{IL}		V_{IL} = 0.4 V				
C1, C2			-200			µA
E0			-100			µA
Input high current, I_{IH}		V_{IH} = 2.4 V			40	µA
Digital output ($\overline{DET}$)						
Output low voltage, V_{OL}		I_{OL} = 2 mA, E0 = 0		0.4	0.6	V
Output high voltage, V_{OH}		I_{OH} = -100 µA, E0 = 0	2.7			V
Internal pull-up resistor			10	15	20	kohm
$\overline{DET}$ short circuit current, I_{ODs}		E0 = 1, $\overline{DET}$ shorted to ground		-330		µA
Power supply rejection ratio (PSRR)						
To two-wire or four-wire port, from		Note 12				
V_{CC}, $PSRR_{CC}$		50 Hz ≤ f ≤ 4 kHz	30	35		dB
		4 kHz ≤ f ≤ 50 kHz	30	35		dB
V_{EE}, $PSRR_{EE}$		50 Hz ≤ f ≤ 4 kHz	30	35		dB
		4 kHz ≤ f ≤ 50 kHz	12	18		dB
V_{Bat}, $PSRR_{Bat}$		50 Hz ≤ f ≤ 4 kHz	40	50		dB
		4 kHz ≤ f ≤ 50 kHz	30	35		dB
Power supply currents (relay driver off)						
V_{CC} current, I_{CC}		Open circuit state		1		mA
V_{EE} current, I_{EE}		C2, C1 = 0, 0		1		mA
V_{Bat} current, I_{Bat}		On-hook		0.5		mA
V_{CC} current, I_{CC}		Stand-by state		2		mA
V_{EE} current, I_{EE}		C2, C1 = 1, 1		1		mA
V_{Bat} current, I_{Bat}		On-hook		0.5		mA
V_{CC} current, I_{CC}		Active state		4		mA
V_{EE} current, I_{EE}		C2, C1 = 1, 0		2		mA
V_{Bat} current, I_{Bat}		On-hook		3		mA
Power dissipation						
Open circuit state total dissipation, P_{Op}		C2, C1 = 0, 0 On-hook ($R_L = \infty$) or off-hook (R_L = 0)		25	35	mW
Stand-by state total dissipation, P_{OnSb}		C2, C1 = 1, 1 On-hook ($R_L = \infty$)		35	45	mW
Active state total dissipation, P_{OnAct}		C2, C1 = 1, 0 On-hook ($R_L = \infty$)		160	220	mW
Active state total dissipation,		C2, C1 = 1, 0, Note 13				
$P_{OffAct200}$		Off-hook, R_L = 200 ohm		1.25	1.40	W
$P_{OffAct600}$		Off-hook, R_L = 600 ohm		1.00	1.20	W
Temperature guard						
Junction temperature at threshold, T_{JG}			145	160	170	°C
Temperature guard hysteresis, ∂T_{JG}				20		°C
Thermal resistance						
28-pin PLCC, $\theta_{JP28plcc}$		Junction to terminals 3, 6, 10, 17, 24 connected together, Note 14		10	15	°C/W
22-pin plastic DIP, $\theta_{JP22dip}$		Junction to terminals 5, 6, 17, 18 connected together, Note 14		10	15	°C/W

Notes

1. The overload level is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:

   $Z_{TRX} = Z_T/|G_{2-4} \cdot \alpha_{RSN}|$

   where

   Z_{TRX} = impedance between the TIPX and RINGX terminals

   Z_T = programming network between the VTX and RSN terminals

   G_{2-4} = TIPX - RINGX to VTX gain, nominally = 1

   α_{RSN} = receive current gain, nominally = -1000 (current defined as positive when flowing into the receive summing node, RSN and when flowing from TIPX to RINGX)
3. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistor, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground. For R_T = 600 kohms the capacitance value is approximately 33 pF.
4. The overload level is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is G_{2-4} = 1.
5. Fuse resistors R_F impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for R_F = 0.
6. The specified insertion loss tolerance does not include errors caused by external components.
7. The level is specified at the two-wire port.
8. The level is specified at the four-wire receive port and referenced to a 600 ohm impedance level.
9. The two-wire idle noise is specified with the port terminated in 600 ohms (R_L) and with the four-wire receive port grounded (E_{RX} = 0, see figure 6).

   The four-wire idle noise at VTX is specified with the two-wire port terminated in 600 ohms (R_L). The noise specification is with respect to a 600 ohm impedance level at VTX. The four-wire receive port is grounded (E_{RX} = 0, see figure 6).
10. With the RD terminal left open, the loop current detector on-hook to off-hook threshold is internally set to 8.0 mA and the off-hook to on-hook threshold to 7.3 mA. The loop current detection threshold can be set to higher values by connecting a resistor, R_D, between terminal RD and V_{EE} (-5 V), as described in section Loop Monitoring Functions.
11. Refer to section Loop Monitoring Functions, Loop Current Detector.
12. Power supply rejection ratio test signal is 100 mVrms (sinusoidal).
13. Line resistor R_F = 0 ohm.
14. Junction to ambient thermal resistance will be dependent on external thermal resistance from VBAT terminals to ambient.

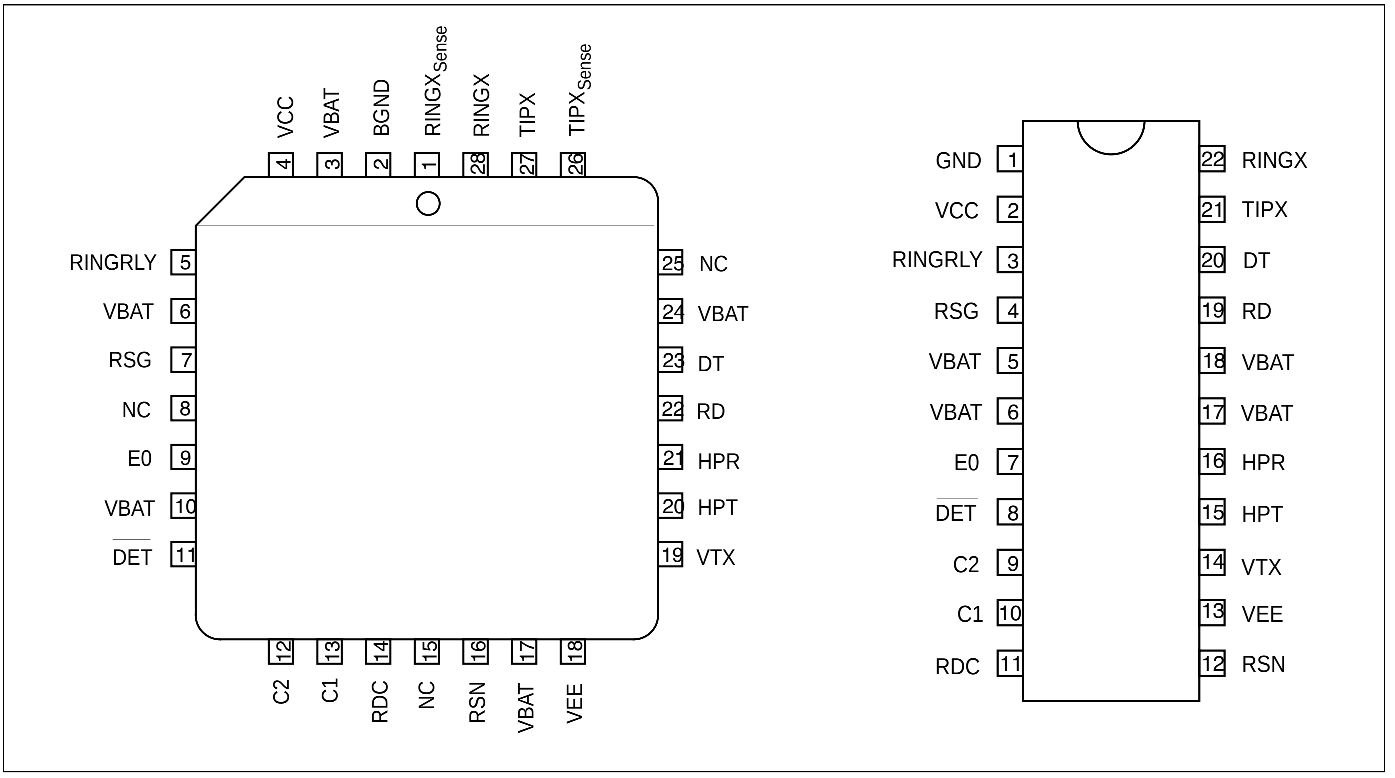


Figure 7. Pin configuration, 28-pin plastic leaded chip carrier and 22-pin plastic dual-in-line package, top view.

Pin Description

PLCC: 28-pin, plastic, j-leaded chip carrier. DIP: 22-pin, dual-in-line (batwing), plastic package. Refer to figure 7.

PLCC	DIP	Symbol	Description
1	-	$RINGX_{Sense}$	$RINGX_{Sense}$ is internally connected to RINGX. $RINGX_{Sense}$ is used during manufacturing, but requires no connection in SLIC applications, i.e. leave open.
2	1	GND	Ground.
3	-	VBAT	Refer to PLCC, terminal 6 description.
4	2	VCC	+5 V power supply.
5	3	RINGRLY	Ring relay driver output. Open emitter with grounded collector (npn). Sources 50 mA from ground to a relay coil connected to a negative voltage. Must be protected by external inductive kick-back diode. Positive voltage relay driver can be provided as a metal mask option. Contact factory for availability.
6, 3, 10, 17, 24	5, 6, 17, 18	VBAT	Battery supply voltage. Negative with respect to GND. -21 V to -58 V. All VBAT terminals should be connected to printed circuit board traces to provide heatsinking.
7	4	RSG	Saturation guard programming resistor, R_{SG}, connects from this terminal to VEE. Leave open for nominal battery voltages from -24 V to -28 V. Connect to VEE for a nominal battery voltage of -48 V. For other battery voltages and for detailed information refer to section Battery Feed.
8	-	NC	No internal connection. Note 1.
9	7	E0	TTL compatible enable input. Enables the $\overline{DET}$ output, when set to logic level low and disables the $\overline{DET}$ output, when set to logic level high. Refer to section Enable Input for detailed information.
10	-	VBAT	Refer to PLCC, terminal 6 description.

PLCC	DIP	Symbol	Description
11	8	$\overline{DET}$	Detector output. Inputs C1 and C2 select one of the two detectors to be connected to the $\overline{DET}$ output. A logic low level at the enabled (refer to E0) $\overline{DET}$ output indicates a triggered detector condition. The $\overline{DET}$ output is open collector with internal pull-up resistor (approximately 15 kohms) to VCC.
12 13	9 10	C2 C1	C1 and C2 are TTL compatible inputs controlling the SLIC operating states. Refer to section Control Inputs for details.
14	11	RDC	Dc loop feed is programmed by one resistor connected from this pin to the receive summing node (RSN). A decoupling capacitor, C_{DC}, connected from RDC to GND removes noise and other ac signals from the battery feed control loop.
15	-	NC	No internal connection. Note 1.
16	12	RSN	Receive summing node. 1000 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for feed resistance, two-wire impedance and receive gain connect to the receive summing node.
17	-	VBAT	Refer to PLCC, terminal 6 description.
18	13	VEE	-5V power supply.
19	14	VTX	Transmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one. The two-wire terminating impedance programming network connects between VTX and RSN.
20	15	HPT	Tip side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} connects to pin, HPR.
21	16	HPR	Ring side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} capacitor connects to pin, HPT.
22	19	RD	Loop current detector programming resistor R_D connects from RD to VEE. An optional filter capacitor C_D may be connected between terminal RD and ground. With the RD pin left open, the loop current detect threshold is internally set to 8.0 mA. Refer to section Loop Monitoring Functions for additional information.
23	20	DT	DT is the non-inverting ring trip comparator input. The inverting comparator input is internally connected to VEE. With DT more negative than the inverting input, the detector output, $\overline{DET}$, is at logic level low, indicating off-hook condition. The ring trip network connects to the DT input.
24	-	VBAT	Refer to PLCC, terminal 6 description.
25	-	NC	No internal connection. Note 1.
26	-	$TIPX_{Sense}$	$TIPX_{Sense}$ is internally connected to TIPX. $TIPX_{Sense}$ is used during manufacturing, but requires no connection in SLIC applications, i.e. leave open.
27 28	21 22	TIPX RINGX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relays).

Notes

1. Terminals marked NC are not internally connected to the chip. These terminals may be connected to ground for shielding.

Functional Description and Applications Information

Transmission

General

A simplified ac model of the transmission circuits is shown in figure 8. Circuit analysis yields:

$$V_{TR} = V_{TX} + I_L \cdot 2R_F \qquad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{1000} \qquad (2)$$

$$V_{TR} = E_L - I_L \cdot Z_L \qquad (3)$$

where

V_{TX} is a ground referenced unity gain version of the ac metallic voltage between the TIPX and RINGX terminals, i.e. $V_{TX} = 1 \cdot V_{TRX}$.

V_{TR} is the ac metallic voltage between tip and ring.

E_L is the line open circuit ac metallic voltage.

I_L is the ac metallic current.

R_F is a current limiting resistor in the overvoltage protection network.

Z_L is the line impedance.

Z_T determines the SLIC TIPX to RINGX impedance.

Z_{RX} controls four- to two-wire gain.

V_{RX} is the analog ground referenced receive signal.

Two-wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistors R_F, let $V_{RX} = 0$.

From (1) and (2):

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F$$

With Z_{TR} and R_F known Z_T may be calculated from

$$Z_T = 1000 \cdot (Z_{TR} - 2R_F)$$

Example: calculate Z_T to make the terminating impedance Z_{TR} = 600 ohms in series with 2.16 µF. R_F = 40 ohms.

Using the expression above

$$Z_T = 1000 \cdot \left(600 + \frac{1}{j\omega \cdot 2.16 \cdot 10^{-6}} - 2 \cdot 40\right)$$

i.e Z_T = 520 kohms in series with 2.16 nF. It is always necessary to have a high ohmic resistor in parallel with the capacitor. This gives a DC-feedback loop for low frequency which ensures stability and reduces noise.

Two-wire to Four-wire Gain

The two-wire to four-wire gain, G_{2-4}, is obtained from (1) and (2) with $V_{RX} = 0$:

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F}$$

Four-wire to Two-wire Gain

The four-wire to two-wire gain, G_{4-2}, is derived from (1), (2) and (3) with $E_L = 0$:

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{Z_T/1000 + 2R_F + Z_L}$$

Four-wire to Four-wire Gain

The four-wire to four-wire gain, G_{4-4}, is derived from (1), (2) and (3) with $E_L = 0$:

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L + 2R_F}{Z_T/1000 + 2R_F + Z_L}$$

Hybrid Function

The PBL 3767 SLIC forms a particularly flexible and compact line interface when used with programmable CODEC/filters. The programmable CODEC/filters allow for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. It also permits the system controller to adjust transmit and receive gains as well as terminating impedance. Refer to programmable CODEC/filter data sheets for design information.

The hybrid function in an implementation utilizing the uncommitted amplifier in a conventional CODEC/filter combination is shown in figure 9. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to VTX. This voltage is converted by R_{TX} to a current into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \qquad (E_L = 0)$$

Substituting the four-wire to four-wire gain expression, G_{4-4}, for V_{RX}/V_{TX} yields the formula for a balanced network:

$$Z_B = -R_{TX} \cdot \frac{V_{RX}}{V_{TX}} = R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{Z_T/1000 + 2R_F + Z_L}{Z_L + 2R_F}$$

Example: $Z_{TR} = Z_L$ = 600 ohms (R_L) in series with 2.16 µF (C_L), R_F = 40 ohms, R_{TX} = 20 kohms, G_{4-2} = -1. Calculate Z_B. Using the Z_B formula above:

$$Z_B = \{Z_L = Z_{TR}\} = R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{2Z_L}{Z_L + 2R_F} =$$

$$= \{G_{4-2} = -1\} = R_{TX} \cdot \frac{Z_L}{Z_L + 2R_F} =$$

$$= R_{TX} \cdot \frac{1 + j\omega \cdot R_L \cdot C_L}{1 + j\omega \cdot (R_L + 2R_F) \cdot C_L}$$

A network consisting of R_{B1} in series with the parallel combination of R_B and C_B has the same form as the required balance network, Z_B. Basic algebra yields:

$$R_{B1} = R_{TX} \cdot \frac{R_L}{R_L + 2R_F} = 17.6 \text{ kohms}$$

$$R_B = R_{TX} \cdot \frac{2R_F}{R_L + 2R_F} = 1353 \text{ ohms}$$

$$C_B = \frac{(R_L + 2R_F)^2 \cdot C_L}{R_{TX} \cdot 2R_F} = 0.62\ \mu F$$

Longitudinal Impedance

In the active state, a feedback loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Therefore longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, well within the SLIC common mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal reference voltage, $V_{Bat}/2$. As shown below, the SLIC appears as 20 ohms to ground per wire to longitudinal disturbances. It should be noted, that longitudinal currents may exceed the dc loop current without disturbing the vf transmission. From figure 10 the longitudinal impedance can be calculated:

$$\frac{V_{Lo}}{I_{Lo}} = \frac{R_{Lo}}{1000} = 20 \text{ ohms}$$

where

V_{Lo} is the longitudinal voltage

I_{Lo} is the longitudinal current

R_{Lo} = 20 kohms sets the longitudinal impedance

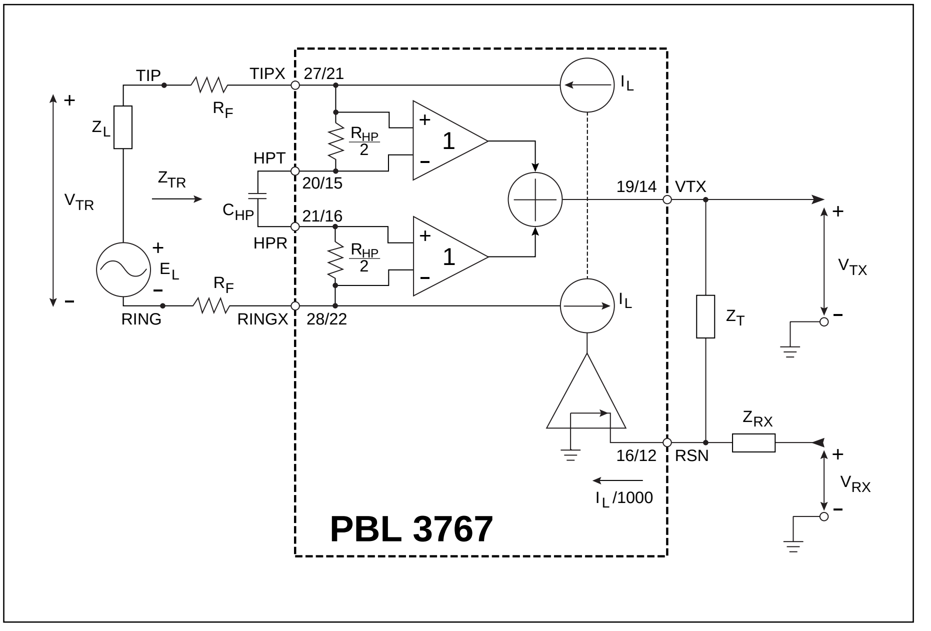


Figure 8. Simplified ac transmission circuit.

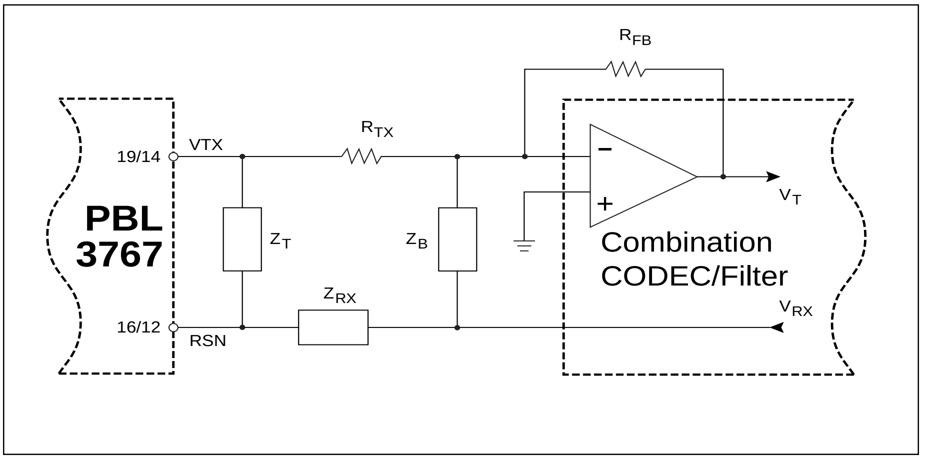


Figure 9. Hybrid function.

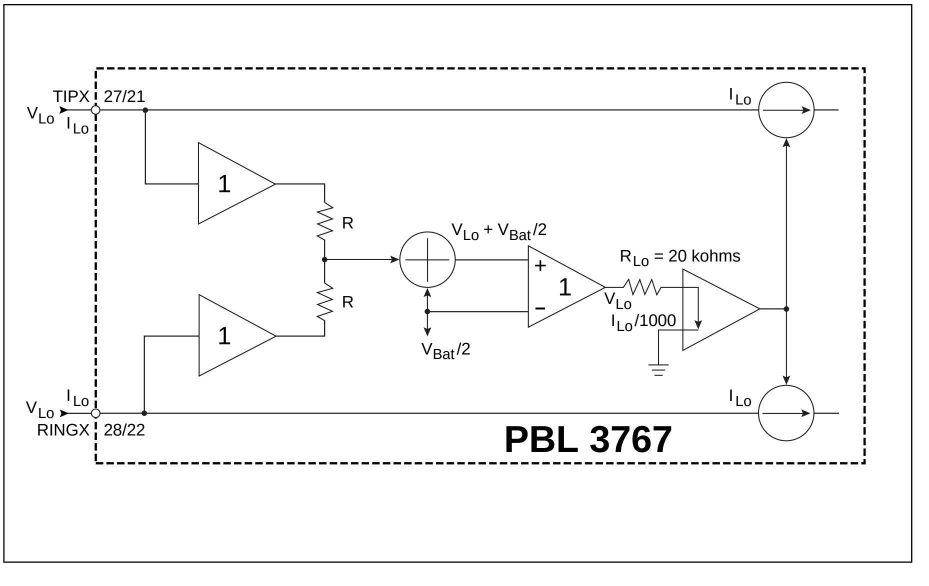
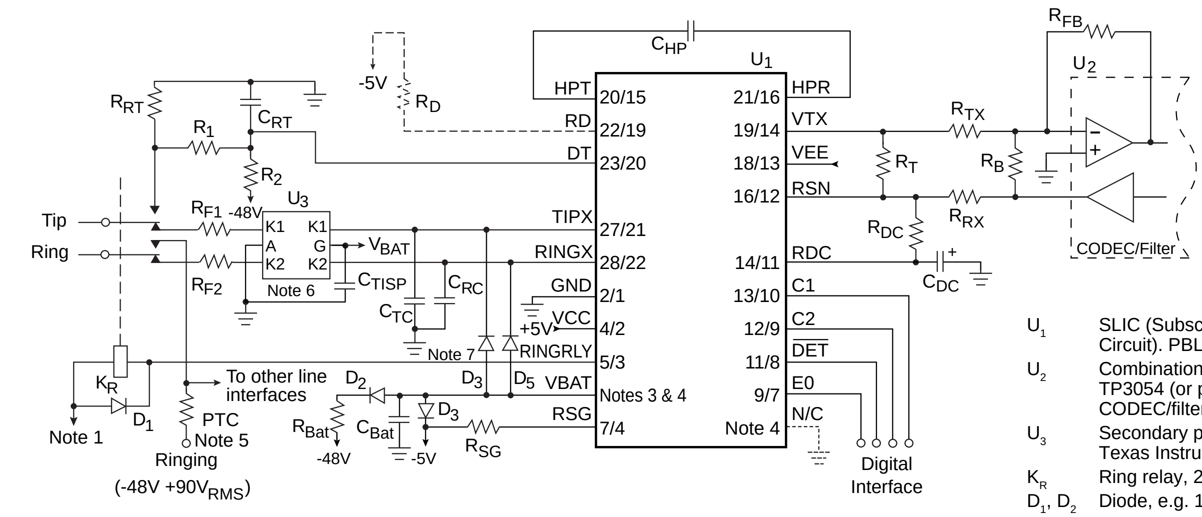


Figure 10. Longitudinal feedback loop.



U_1	SLIC (Subscriber Line Interface Circuit). PBL 3767
U_2	Combination CODEC/filter, e.g. TP3054 (or programmable CODEC/filter, e.g. SLAC)
U_3	Secondary protection (e.g. Texas Instruments TISP PBL 1
K_R	Ring relay, 2C contacts. Note 2
D_1, D_2	Diode, e.g. 1N4454
D_3	Diode, e.g. 1N4004
R_{F1},R_{F2}	Line resistor, 40 Ω, 1% match, e.g. Ericsson Components PBR 51XX
R_1	Resistor, 150 kΩ, 5%, 1/4 W
R_2	Resistor, 2 MΩ, 5%, 1/4 W
R_B	Resistor, 17.8 kΩ, %, 1/4 W
R_{Bat}	Resistor, 5.1 Ω, 5%, 1/4 W
R_D	Optional. Refer to paragraph “Loop Current Detector”.
R_{DC}	Resistor, 20 kΩ, 5%, 1/4 W
R_{FB}	Resistor, 24.3 kΩ, 1%, 1/4 W
R_{RX}	Resistor, 6261 kΩ, 1%, 1/4 W
R_{RT}	Resistor, 150 Ω, 5%, 2 W
R_{SG}	Resistor, 0 Ω (for V_{Bat} = -48V)
R_T	Resistor, 523 kΩ, 1%, 1/4 W
R_{TX}	Resistor, 20.0 kΩ, 1%, 1/4 W
C_{Bat}	Capacitor, 0.47 µF, 20%, 100 V
C_{DC}	Capacitor, 3.3 µF, 20%, 10 V
C_{HP}	Capacitor, 0.033 µF, 20%, 100V
C_{RT}	Capacitor, 0.39 µF, 20%, 100 V
C_{TC}, C_{RC}	Capacitor, 2200 pF, 20%, 100 V
C_{TISP}	Capasitor 220nF, 20%, 100V

Notes

1. The relay coil may be connected to a negative voltage, down to the V_{Bat} limit. For V_{Bat} = -48 V relay coils with voltage ratings from 5 V to 48 V may be used.
2. The plastic leaded chip carrier terminals 3, 6, 10, 17 and 24 shall all be connected to the V_{Bat} supply trace to provide heat sinking.
3. The dual-in line package terminals 5, 6, 17 and 18 shall all be connected to the V_{Bat} supply trace to provide heat sinking.
4. The plastic leaded chip carrier terminals 8, 15 and 25 are not internally connected to the chip. These terminals may be connected to ground to provide shielding.
5. It may be desirable to include a PTC or other type of short circuit protection for the ringing generator.
6. The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferable a groundplane.

Figure 11. Single channel subscriber line interface with PBL 3767 and a combination CODEC/filter.

Capacitors C_{TC} and C_{RC}

The capacitors designated C_{TC} and C_{RC} in figure 11, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the diode and SCR clamps in the overvoltage protection network, before these devices have had time to activate and could damage the SLIC. C_{TC} and C_{RC} short such very fast transients to ground. The recommeded value for C_{TC} and C_{RC} is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss. C_{TC} and C_{RC} contribute a metallic impedance of $1/(\pi \cdot f \cdot C_{TC}) \approx 1/(\pi \cdot f \cdot C_{RC})$, a TIPX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

Ac - Dc Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals HPT and HPR provides the separation between circuits sensing tip-ring dc conditions and circuits processing ac signals. A C_{HP} value of 33 nF will position the low end frequency response 3dB break point at 12 Hz (f_{3dB}) according to $f_{3dB} = 1/(2\pi \cdot R_{HP} \cdot C_{HP})$ where $R_{HP} \approx$ 400 kΩ.

Battery Feed

Overview

The PBL 3767 SLIC emulates a resistive battery feed system with loop current limiting on short loops. The block diagram in figure 12 shows the basic PBL 3767 active state battery feed system (short loop current limiting not shown.)

The emulated battery feed is a 50 V source in series with a programmable feed resistance. The apparent 50 V battery is independent of the actual supply voltage connected to the SLIC. The feed resistance value is set by an external programming resistor, R_{DC}. For short loops the battery feed reverts to quasi constant current.

To permit the line drive amplifiers to operate without vf signal distortion even on high resistance or open circuit loops, a saturation guard circuit limits the loop voltage, when the tip to ring dc voltage approaches the available battery supply voltage.

Figure 13 shows an example of PBL 3767 active state battery feed.

With the SLIC set to the stand-by state, most of the circuit is disabled, including the line drive amplifiers, to conserve power. A 2 x 900 ohm resistive feed substitutes for the active state battery feed.

The following paragraphs describe the PBL 3767 battery feed system in detail.

Case 1: SLIC in the Active State $V_{TRdc} < V_{SGRef}$, $I_{Ldc} < 760/(20000 + R_{DC})$

In the active state C1 = 0 and C2 = 1. In this operating state tip to ring voltages V_{TR} less than V_{SGRef} cause the block titled saturation guard in figure 12 to be disabled, i.e. its output is equal to zero. For this case circuit analysis yields:

$$V_{TR} = 50 \cdot \frac{R_L}{R_L + (R_{DC} + 20000)/50}$$

where

R_L = the line resistance.

R_{DC} = the programming resistance which sets the equivalent feed resistance, $R_{Feed} = (R_{DC} + 20000)/50$.

V_{TR} = the tip to ring dc metallic voltage.

Note, that for simplicity the fuse resistors R_F have not been included.

When the desired feed resistance is known, R_{DC} is calculated from

$R_{DC} = 50 \cdot R_{Feed} - 20000$

For tip to ring voltages V_{TR} less than V_{SGRef} and loop currents $I_{Ldc} < 760/(20000 + R_{DC})$ the PBL 3767 thus emulates a resistive battery feed with 50 V apparent battery and a feed resistance equal to $(R_{DC} + 20000)/50$.

Capacitor C_{DC}, connected between the RDC terminal and ground removes noise and vf signals from the battery feed control loop. C_{DC} is calculated according to

$$C_{DC} = \frac{1}{2\pi \cdot f_{DC}} \cdot \left[\frac{1}{20000} + \frac{1}{R_{DC}}\right]$$

where

f_{DC} = 5 Hz

R_{DC} = feed bridge programming resistance in ohms

C_{DC} = filter capacitor in farads

Case 2: SLIC in the Active State $V_{TRdc} < V_{SGRef}$, $760/(20000 + R_{DC}) < I_{Ldc} < 1200/(20000 + R_{DC})$

In the active state C1 = 0 and C2 = 1. In this operating range the battery feed circuit reverts to quasi constant current feed with a short circuit loop current

$I_{Ldc} = 1200/(20000 + R_{DC})$

where I_{Ldc} is in amperes for R_{DC} in ohms.

The quasi constant current feed curve is entered when the loop current exceeds

$I_{Ldc} = 760/(20000 + R_{DC})$

where I_{Ldc} is in amperes for R_{DC} in ohms.

Case 3: SLIC in the Active State $V_{TRdc} > V_{SGRef}$, $I_{Ldc} < 760/(20000 + R_{DC})$

In the active state C1 = 0 and C2 = 1. When the tip to ring dc voltage approaches the V_{Bat} supply voltage, a circuit named saturation guard limits the two-wire voltage to a small additional increase beyond the saturation guard threshold, V_{SGref}. This leaves a sufficient voltage margin to the V_{Bat} supply to maintain distortion free vf transmission through the line drive amplifiers. The saturation guard feature makes on-hook transmission possible.

The tip to ring voltage at which the saturation guard becomes active, V_{SGRef}, can be calculated from

$$V_{SGRef} = 12.5 + \frac{5 \cdot 10^5}{22.0 \cdot 10^3 + R_{SG}}$$

where

V_{SGRef} is in volts for R_{SG} in ohms

R_{SG} is a resistor connected between terminal RSG and -5 V.

R_{SG} = open circuit yields V_{SGRef} = 12.5 V

R_{SG} = 0 ohm yields V_{SGRef} = 35.2 V

The loop voltage, V_{TRdc}, as a function of the loop resistance, R_L, for $V_{TRdc} > V_{SGRef}$ is described by

$$V_{TRdc} = \frac{15.38+4.62\cdot10^5 / (22000 + R_{SG})}{R_L + (R_{DC} + 20000) / 650} \cdot R_L$$

from which the open loop voltage ($I_L = 0$) is calculated to

$$V_{TRdc} = 15.38 + \frac{4.62\cdot10^5}{22000 + R_{SG}}$$

For R_{SG} = open circuit, the open circuit tip to ring dc voltage is 15.4 V, which is compatible with V_{Bat} in the -24 V to -28 V range.

For R_{SG} = 0 ohm, the open circuit tip to ring dc voltage is 36.4 V, which is compatible with V_{Bat} in the -42 V to -58 V range.

For intermediate battery voltage, V_{Bat}, values R_{SG} can be calculated from

$$R_{SG} = \frac{4.62\cdot10^5}{V_{TRdc} - 15.38} - 22000$$

where

R_{SG} is in ohms for V_{TRdc} in volts

V_{TRdc} is the open loop tip to ring voltage.

Let $V_{TRdc} = |V_{Bat}| - 8$ V to allow distortion free transmission of a 3.1 Vpk vf signal in the on-hook mode. The 8 V margin may be reduced if a vf signal of less than 3.1 Vpk is to be transmitted in the on-hook mode.

Case 4: SLIC in the Stand-by State

In the stand-by state C1 = 1 and C2 = 1. With the SLIC operating in the stand-by, power saving state the tip and ring drive amplifiers are disconnected and a high resistance battery feed is engaged. The loop current can be calculated from

$$I_{Ldc} \approx \frac{|V_{Bat}| - 3\text{ V}}{R_L + 1800\ \Omega}$$

where

I_{Ldc} = loop current

R_L = loop resistance

V_{Bat} = battery supply voltage

-3 V = voltage drop across internal transistors

1800 Ω = feed resistance (900 Ω on the tip side, 900 Ω on the ring side)

PBL 3767 Power Dissipation and Derating

The tip to ring short circuit PBL 3767 total power dissipation, P_{ShTot}, is

$P_{ShTot} = I_{LSh} \cdot (|V_{Bat}| - I_{LSh} \cdot 2R_F) + P_{OnAct}$

where

$I_{LSh} = 1080/(20000 + R_{DC})$ is the short circuit loop current

P_{OnAct} is the active state on-hook dissipation, typically 160 mW.

The permissible maximum device dissipation is 1.5 W. The maximum allowable junction temperature is 140 °C for normal reliability requirements and 110 °C for extreme reliability requirements. The junction temperature is calculated from

$T_J = P_{ShTot} \cdot (\theta_{JP} + \theta_{PA}) + T_{Amb}$, $T_J < 140$ °C

where

$\theta_{JP} = \theta_{JP28plcc} = \theta_{JP22dip}$ is the thermal resistance from junction to all VBAT terminals, typically 10 °C/W.

θ_{PA} is the thermal resistance from all VBAT terminals to ambient. The θ_{PA} value will be dependent on line-card thermal design.

T_{Amb} is the ambient temperature in °C.

Loop Monitoring Functions

Overview

The PBL 3767 SLIC contains detectors for loop current and ring trip. These two detectors report their status via the shared $\overline{DET}$ output. A triggered detector is indicated by a logic low level at the $\overline{DET}$ output. The detector to be connected to the $\overline{DET}$ output is selected via the control interface C1 and C2. Refer to section Control Inputs for a description of the control interface. Enable input E0 sets the $\overline{DET}$ output to either active or high impedance state.

Loop Current Detector

The loop current detector is connected to the $\overline{DET}$ output in the stand-by (C2, C1 = 1, 1) and the active (C2, C1 = 1, 0) states. Refer to figure 14.

The loop current value, I_{LThOff}, at which the loop current detector changes from indicating on-hook to indicating off-hook is internally programmed to 8.0 mA. The internally set loop current detector threshold, I_{LThOn}, for the off-hook to on-hook transition is 7.3 mA.

An external resistor, R_D, may be connected from terminal RD to V_{EE} to increase the loop current detector thresholds. When the desired on-hook to off-hook loop current threshold, I_{LThOff}, is known, the R_D value is calculated from

$$R_D = \frac{1}{I_{LThOff}/500 - 1/62500}$$

where R_D is in ohms for I_{LThOff} in amperes.

The off-hook to on-hook loop current detector threshold, I_{LThOn}, for the selected R_D value is calculated from

$$I_{LThOn} = K_{LThOn} \cdot \left[\frac{1}{R_D} + \frac{1}{62500} \right]$$

where

I_{LThOn} is in amperes for R_D in ohms.

$I_{LThOn} > 7.3$ mA, $K_{LThOn} = 455$ V

The on-hook to off-hook loop current detector threshold, I_{LThOff}, for a specific R_D value is calculated from

$$I_{LThOff} = K_{LThOff} \cdot \left[\frac{1}{R_D} + \frac{1}{62500} \right]$$

where

I_{LThOff} is in amperes for R_D in ohms.

$I_{LThOff} > 8.0$ mA, $K_{LThOff} = 500$ V

During dial pulsing the loop current detector is aided by a speed-up circuit, acting on the RDC output at loop closures. The speed-up circuit will charge the C_{DC} capacitor at a more rapid rate than that set by the $(C_{DC} \cdot R_{DC} \cdot 20000)/(R_{DC} + 20000)$ time constant, resulting in the loop current reaching the detector threshold value faster and therefore minimizing dial pulse distortion.

Loop Current Detector - Filter Capacitor

To increase the loop current detector noise immunity, a filter capacitor may be added from terminal RD to ground. A suggested value for C_D is

$$C_D = \frac{R_D + 62500}{2\pi \cdot (R_D \cdot 62500) \cdot f_{3dB}}$$

where

C_D is in farads for R_D in ohms $f_{3dB} = 500$ Hz

Note that C_D may not be required if the $\overline{DET}$ output is software filtered.

Ring Trip Detector

Ring trip detection is accomplished by monitoring the two-wire line for presence of dc current while ringing is applied. When the subscriber goes off-hook during ringing, dc loop current starts to flow. The SLIC ring trip comparator detects this current flow via an interface network. The DT comparator input is connected to pin 23/20. The other comparator input is internally connected to V_{EE}. The result of the comparison is presented at the $\overline{DET}$ output with logic low level indicating off-hook. The ring trip comparator is automatically connected to the $\overline{DET}$ output, when the SLIC control inputs are set to the ringing state (C2, C1 = 0, 1). When off-hook during ringing is detected, the line card or system controller will proceed to disconnect the ringing source (software ringtrip) by resetting the control input logic states. Alternatively, the $\overline{DET}$ output may be monitored by circuits on the line card, which perform the ringtrip function (hardware ringtrip).

The ringing source may be balanced or unbalanced, superimposed on the V_{Bat} supply voltage. A ring relay, energized by the SLIC ring relay driver, connects the ringing source to tip and ring. For unbalanced ringing systems the loop current sensing resistor, R_{RT}, is placed in series with the return lead to ground.

Figures 15 and 16 show examples of unbalanced and balanced ringing systems. For either ringing system the ringtrip detection function is based on a polarity change at the inputs of the ringtrip comparator.

In the unbalanced case the dc voltage drop across resistor R_{RT} is zero, as long as the telephone remains on-hook. With the telephone off-hook during ringing, dc loop current will flow, causing a voltage drop across R_{RT}. The R_{RT} voltage is applied to the comparator input DT via resistor R_1. R_2 shifts the voltage level to be compatible with the inverting input V_{EE} reference voltage. C_{RT} removes part of the ac component of the ringing signal.

The inverting comparator input is biased at V_{EE}, which is more negative than DT when the telephone is on-hook and is more positive than DT when the telephone goes off-hook during ringing.

Complete removal of the ringing signal ac component at the DT input is not necessary. Some residual ac component at the DT input may, under certain operating conditions, cause the $\overline{DET}$ output to toggle between the on-hook and off-hook states at the ringing frequency. However, with the telephone off-hook, the $\overline{DET}$ output will be at logic low level for more than half the time. Therefore, by sampling the $\overline{DET}$ output, a software routine can discriminate between on-hook and off-hook through examination of the duty cycle. Full removal of the ringing frequency from the DT input, while maintaining ringtrip within required time limits (approximately < 100 ms), usually mandates a second order filter rather than the first order shown in figure 15. The software approach minimizes the number of line card components.

In the balanced ringing system shown in figure 16, R_{RT1} and R_{RT2} are the ringing feed and loop current sensing resistors. With the telephone on-hook, no dc loop current flows to cause a dc voltage drop across resistor R_{RT1}. Voltage divider R_1, R_2 and R_3 biases the ringtrip comparator input DT to be more positive than V_{EE} during on-hook. With the telephone off-hook during ringing dc loop current will flow, causing a voltage drop across resistor R_{RT1}, which will make comparator input DT more negative than V_{EE}. This will set the $\overline{DET}$ output to logic low level,

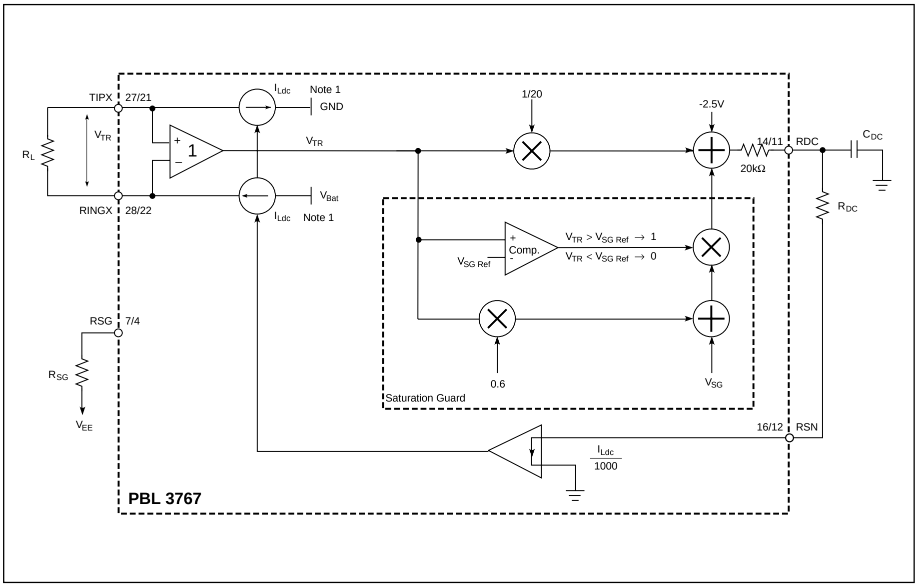


Figure 12. Battery feed (C2, C1 = 1, 0; active state).

$$V_{SGRef} = 12.5 + \frac{5 \cdot 10^5}{R_{SG} + 22\ k\Omega}$$

$$V_{SG} = -7.50 - \frac{3.0 \cdot 10^5}{R_{SG} + 22\ k\Omega}$$

Note 1. Loop current is limited for $I_{Ldc} \geq 760/(20000 + R_{DC})$, and maximum loop current is $I_{Ldcmax} = 1080/(20000 + R_{DC})$.

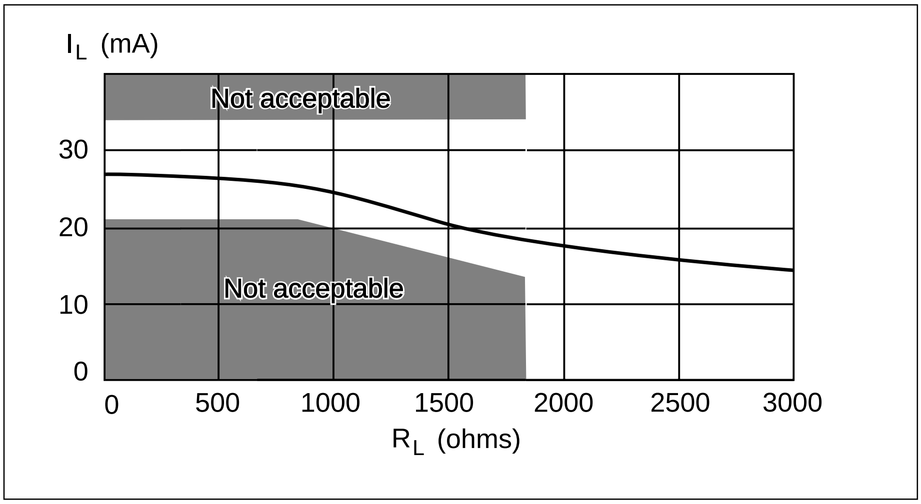


Figure 13. PBL 3767 loop feed example.

R_{DC} = 20 kohms

R_{SG} = 0 ohms (connected to V_{EE})

V_{Bat} = -58 V to -42 V

T_{Amb} = 0 °C to 70 °C

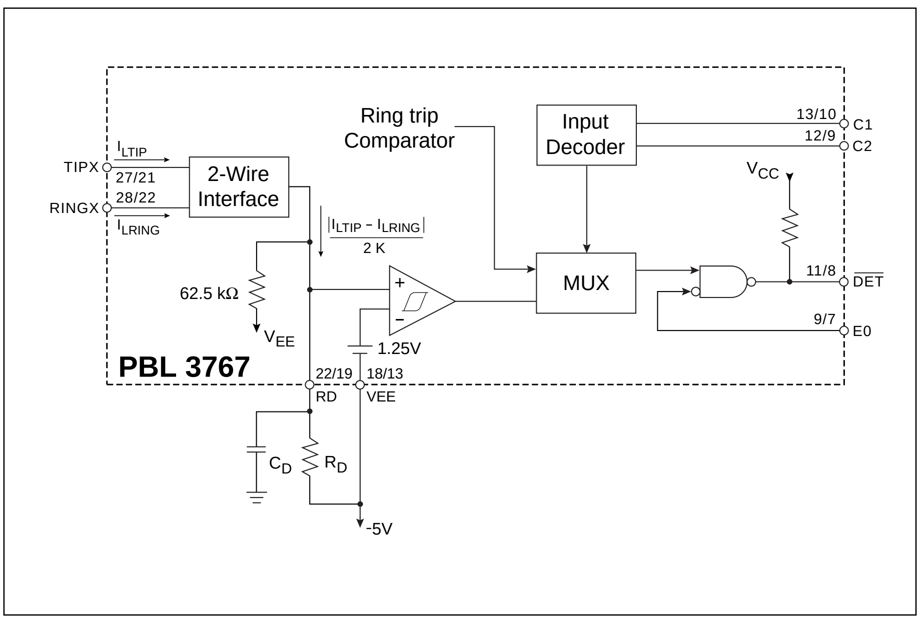


Figure 14. Loop current detector.

On-hook to off-hook loop current threshold, I_{LThOff}:

I_{LThOff} = 8.0 mA for $R_D \rightarrow \infty$

For I_{LThOff} > 8.0 mA:

$$R_D = \frac{1}{I_{LThOff}/K_{LThOff} - 1/62500},$$

K_{LThOff} = 500V (includes factor K)

indicating ringtrip condition. Capacitors C_1 and C_2 filter the ringing voltage at the comparator input. With component values according to figure 16, 20 Hz ringing will be attenuated by 20 dB and 30 Hz ringing will be attenuated by 23 dB before reaching the DT input.

Relay Driver

The PBL 3767 SLIC incorporates a ring relay driver designed as open emitter with grounded collector (npn) having a current sourcing capability of 50 mA. The relay coil must be connected to a negative voltage ≤ $|V_{Bat}|$. An external inductive kick-back clamp diode must be employed to protect the drive transistor.

Control Inputs

Overview

The PBL 3767 SLIC has two TTL compatible control inputs, C1 and C2. A decoder in the SLIC interprets the control input conditions and sets up the commanded operating state.

Open Circuit State (C2, C1 = 0, 0)

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum. No detectors are active.

Ringing State (C2, C1 = 0, 1)

The ring relay driver, RINGRLY, is activated and the ring trip comparator is connected to the detector output, $\overline{DET}$. The TIPX and RINGX terminals are in the high impedance state and signal transmission is inhibited.

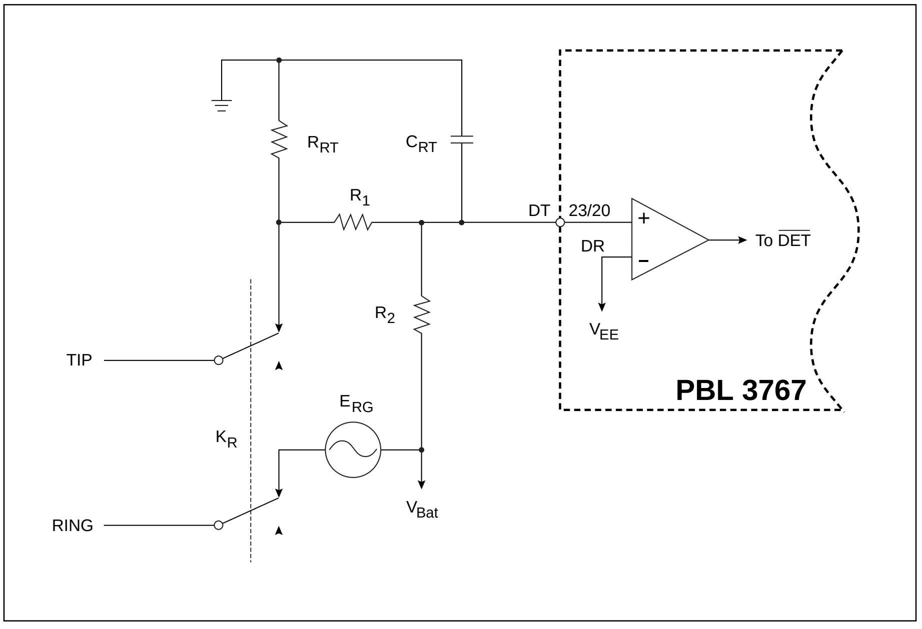


Figure 15. Example ring trip network, unbalanced ringing.

Note: *Ericsson Components unbalanced ring trip network PBA 3310 contains a two-pole filter.*

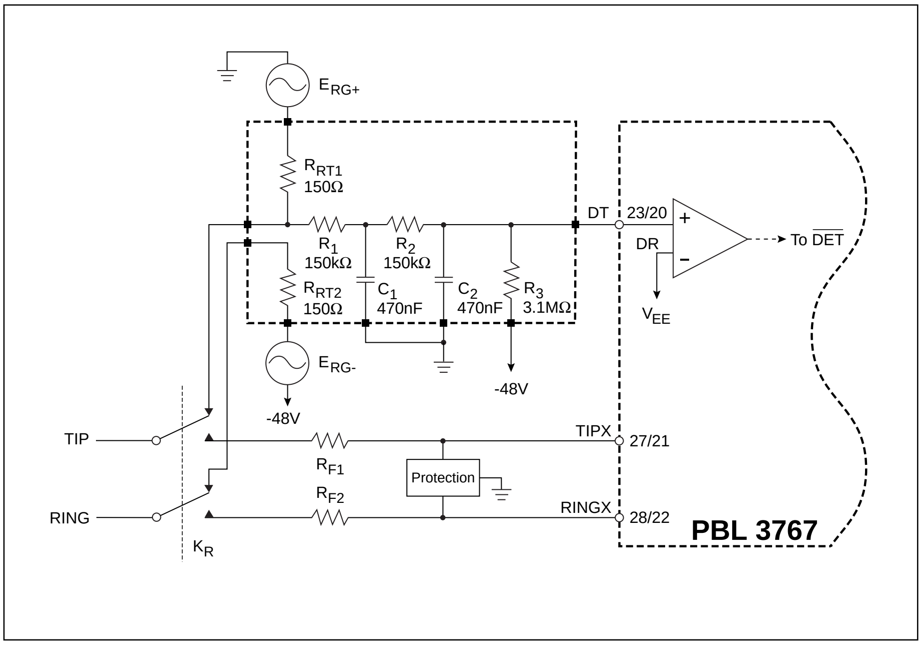


Figure 16. Example ring trip network, balanced ringing.

Active State (C2, C1 = 1, 0)

TIPX is the terminal closest to ground potential and sources loop current, while RINGX is the more negative terminal and sinks loop current. Vf signal transmission is normal. The loop current detector is activated and connected to the $\overline{DET}$ output.

Stand-By State (C2, C1 = 1, 1)

In the stand-by state the line drive amplifiers are disconnected. The loop feed is converted to resistive form according to

$$I_L \approx \frac{|V_{Bat}| - 3\ V}{R_L + 1800\ \Omega}$$

where

I_L = loop current (A)

V_{Bat} = battery supply voltage (V)

R_L = loop resistance (ohm)

The short circuit loop current (I_{LSh}) for V_{Bat} = -48V is then limited to $I_{LSh} \approx 25.0$ mA.

The loop current detector is activated in the stand-by state and is gated to the $\overline{DET}$ output.

Table 1 summarizes the above description of the control inputs.

Enable Input (E0)

TTL compatible enable input E0 controls the function of the $\overline{DET}$ output.

E0, when set to logic level low, enables the $\overline{DET}$ output, which is a collector output with internal pull-up resistor (approx. 15 kohms) to V_{CC}. A $\overline{DET}$ output at logic level low indicates triggered detector condition (loop current above threshold current or telephone off-hook during ringing). A $\overline{DET}$ output at logic level high indicates a non triggered detector condition.

E0, when set to logic level high disables the $\overline{DET}$ output; i.e. it appears as a resistor connected to V_{CC}.

Table 2 summarizes the above description of the enable input.

Overvoltage Protection

The PBL 3767 SLIC must be protected against overvoltages and power crosses. Refer to Maximum Ratings, TIPX and RINGX terminals for maximum allowable continuous and transient voltages, that may be applied to the SLIC. The circuit shown in figure 11 utilizes series resistors (R_F, R_F) together with a programmable overvoltage protector (e g Texas Instrument TISP PBL1), serving as a secondary protection. The protection network in figure 11 is designed to meet requirements in CCITT K20, Table 1.

The TISP PBL1 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i e the battery voltage, V_{Bat}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimised.

Positive overvoltages are clamped to ground by an internal diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage. If sufficient current is available from the overvoltage, then the protector will crawbar into a low voltage on-state condition, clamping the over-voltage close to ground.

A gate decoupling capacitor, C_{TISP} is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. Without the capacitor even the low inductance in the track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F, serve the dual purposes of being non-destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross. Ericsson Components AB offers a series of thick film resistors networks (e g PBR 51-series and PBR 53-series) designed for this application.

Also deviced with a build in resetable fuse function is offered (e g PBR 52-series) including positive temperature coefficient (PTC) resistors, working as resetable fuses, in series with thick film resistors. Note that it is important to always use PTC's in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore the ability to protect the SLIC will be reduced.

If there is a risk for overvoltages on the V_{Bat} terminal on the SLIC, then this terminal should also be protected.

Overtemperature Protection

A ring lead to ground short circuit fault condition, as well as other improper operating modes, may cause excessive SLIC power dissipation. If junction temperature increases beyond 160 °C, the temperature guard will trigger, causing the SLIC to be set to a high impedance state. In this high impedance state power dissipation is reduced and the junction temperature will return to a safe value. Once below 140 °C junction temperature the SLIC is returned back to its normal operating mode and will remain in that state assuming the fault condition has been removed.

Table 1. PBL 3767 operating states.

State number	C2	C1	SLIC operating state	Active detector	$\overline{DET}$ Output Note 1.
1	0	0	Open circuit	No active detector	Logic level high
2	0	1	Ringing	Ring trip detector	Ring trip status
3	1	0	Active	Loop curr. detector	Loop current status
4	1	1	Stand-by	Loop curr. detector	Loop current status

Notes

1. E0 = 0, i.e. the $\overline{DET}$ output is enabled. A logic low level at the $\overline{DET}$ output indicates a triggered detector.

Table 2. Enable input E0.

Enable state	E0	$\overline{DET}$ output status	Active detector
1	0	Active	Loop current or ring trip detector Note 1.
2	1	High impedance Note 2.	None

Notes

1. Detector selected according to Table 1.
2. In the high impedance state the $\overline{DET}$ output appears as a 15 kohms resistor to V_{CC}.

Power-up Sequence

The voltage at pin VBAT sets the substrate voltage, which must at all times be kept more negative than the voltage at any other terminal. This is to maintain correct junction isolation between devices on the chip. To prevent possible latch-up, the correct power-up sequence is to connect ground and V_{Bat}, then other supply voltages and signal leads. A diode with a 2 A current rating, connected with its cathode to V_{EE} and anode to V_{Bat}, ensures the presence of the most negative supply voltage at the VBAT terminals, should the V_{Bat} supply voltage be absent.

The V_{Bat} voltage should not be applied at a faster rate than $\partial V_{Bat}/\partial t = 4$ V/µsec or with a time constant formed by a 5.1 ohm resistor in series with the VBAT pin and a 0.47 microfarad capacitor from the VBAT pin to ground. One resistor may be shared by several SLICs.

Printed Circuit Board Lay-out

Care in PCB layout is essential for proper function. The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN terminal. A ground plane surrounding the RSN pin is advisable. The C_{HP} capacitor should be placed close to terminals HPT and HPR to avoid unwanted disturbances.

Ordering information

Package	Temp. Range	Part No.
Plastic DIP 22 pin	0 °C to 70 °C	PBL 3767N
Plastic DIP 22 pin	0 °C to 70 °C	PBL 3767/6N
PLCC 28 pin	0 °C to 70 °C	PBL 3767QN
PLCC 28 pin	0 °C to 70 °C	PBL 3767/6QN

1522-PBL 3767 Uen Rev. B

September 1997

Ericsson Components AB
S-164 81 Kista-Stockholm, Sweden
Telephone: (08) 757 50 00