APPLICATION NOTE

Demonstration Board
OQ2541HP
SDH/SONET Data&Clock Recovery

May 1996

Philips
Semiconductors

PHILIPS

SDH/SONET Data&Clock Recovery OQ2541HP

FEATURES

- Full functional testing capability, including loop mode
- Separate clock conversion and data & clock recovery functionality

4-Layer Epoxy FR4 PCB

- Differential microstrip lines with 50 Ω odd mode impedance
- SMA RF Connectors
- Single-ended and differential operation possible
- Assembly Instructions
- Full extended ground and supply voltage layers

APPLICATIONS

- Functional Verification
- Performance Evaluation
- Application Tests

ORDERING INFORMATION

To order demonstration boards, write to:

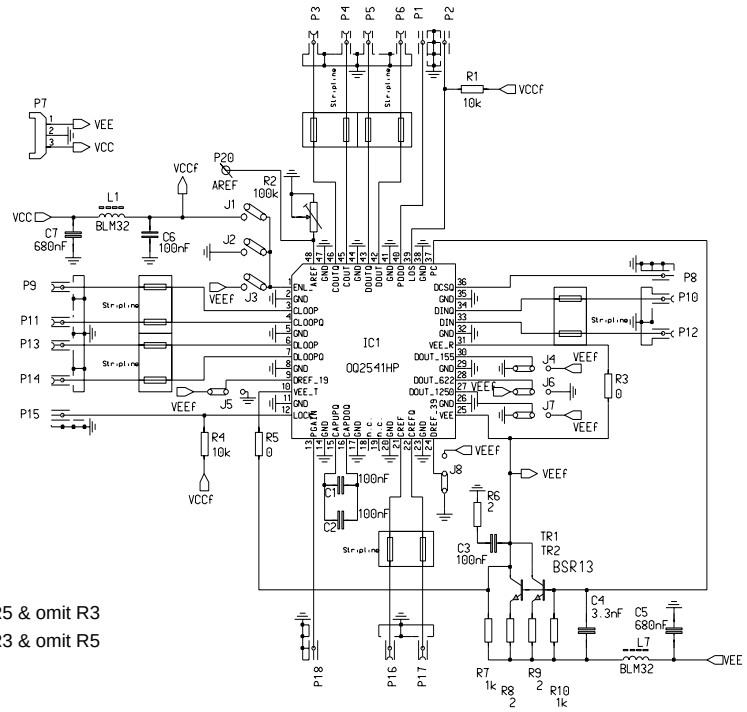
Philips Semiconductors C&M-N
Marketing Department
Gerstweg 2
6534 AE Nijmegen
The Netherlands

GENERAL DESCRIPTION

The demonstration board for the OQ2541HP data & clock recovery IC can be supplied assembled or non assembled. This board can be used to evaluate the OQ2541HP, alone, and allows the designer to do extensive testing without having to worry about other external factors. For maximum reliability the IC is soldered to the board. This application note describes the schematic and the layout of the board and contains assembly instructions. A functional test is described in detail.

A data sheet for the IC is available: “Data Sheet OQ2541HP, Preliminary specification, May 1996”

DEMO BOARD SCHEMATIC

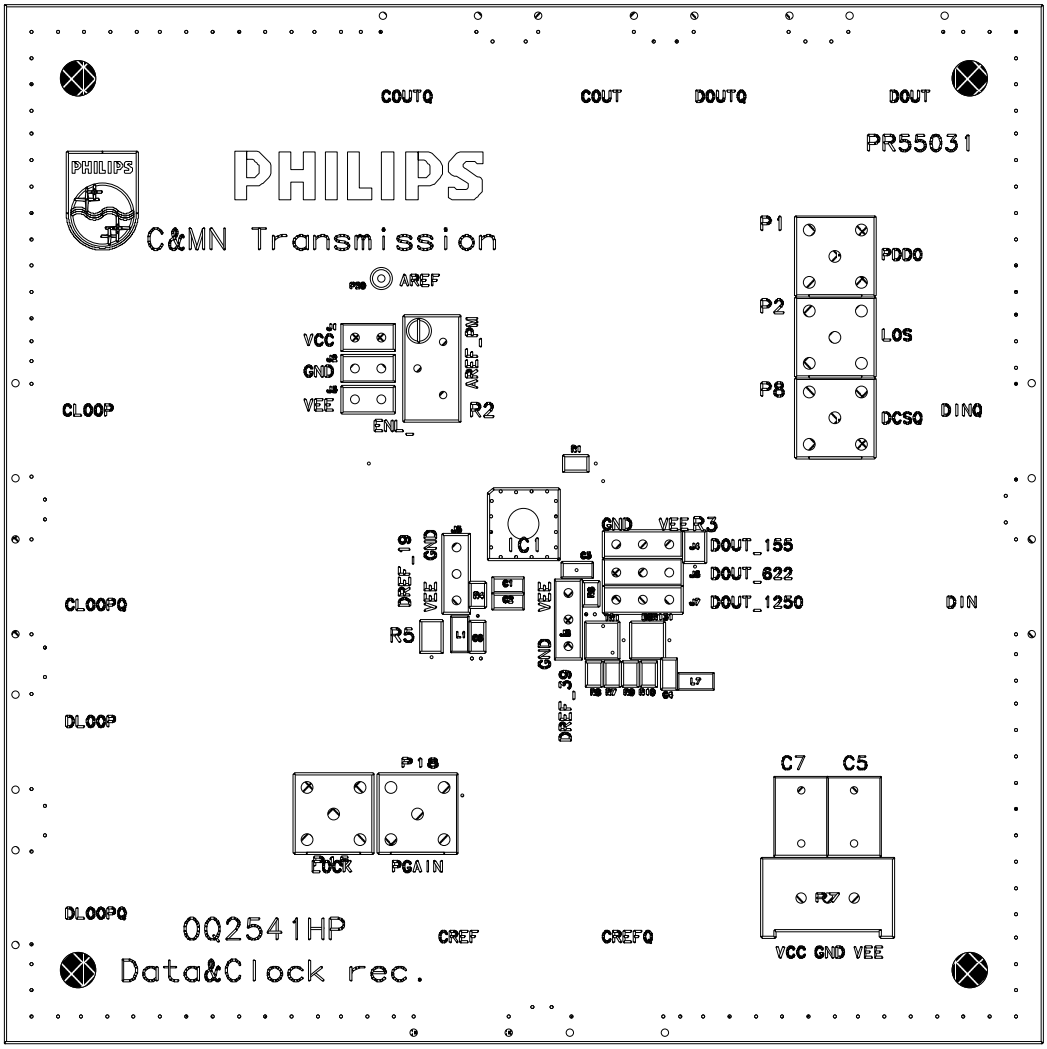


CC mode: mount R5 & omit R3
DCR mode: mount R3 & omit R5

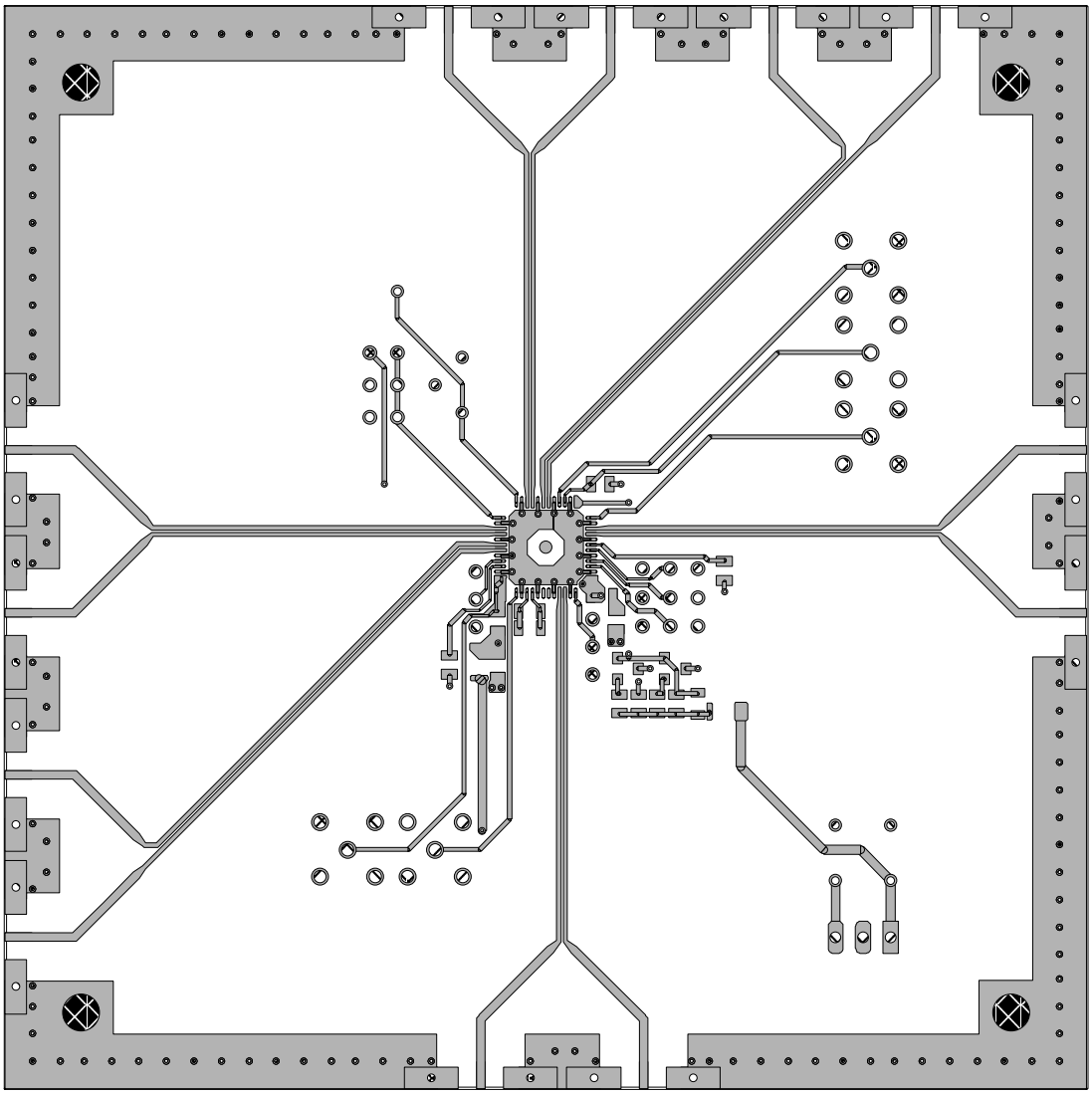
BILL OF MATERIALS

item no	count	company part no	component	series	vendor	tolerance	rating	geometry	reference
1	1	8222-411-55031	Board						
2	5	R144426	SMB CLICK str	COAX	Radiall			SMB_straight	P1,P2,P8, P15,P18
3	1	MKS3733-1-0-303	MKS3730_3p	MKS3730	Stocko			MKS3730_3p	P7
4	2		BSR13	Switching	Philips			SOT23	TR1, TR2
5	1	2422-034-15068	Solder Pin Small		Philips			Solder Pin Small	P20
6	5	2422-024-04008	Jumper_3p	print switch	Philips			Jumper_3p	J4,J5,J6,J7, J8
7	3	2422-024-04008	Jumper_2p	print switch	Philips			Jumper_2p	J1,J2,J3
8	2	2322-734-92002	0	RC11	Philips	1%	0.1 W	R0805	R3,R5
9	3	2322-730-61204	2	RC11	Philips	5%	0.1 W	R0805_hf	R6,R8,R9
10	2	2322-730-61103	10k	RC11	Philips	5%	0.1 W	R0805_hf	R1,R4
11	2	2322-730-61102	1k	RC11	Philips	5%	0.1 W	R0805_hf	R7,R10
12	4	2222-910-16649	100 nF	C910-X7R	Philips	10%	25 V	C0805_hf	C1,C2,C3, C6
13	1	2222-590-16621	3.3 nF	C590-X7R	Philips	10%	63 V	C0805_hf	C4
14	2	2222-370-11684	680 nF	MKT 370	Philips	10%	63 V	C370_C	C5, C7
15	1	2122-362-00729	100k	3296Y	Bourns	10%	0.5 W	BO3296Y	R2
16	1	PN-OQ2541HP	OQ2541HP	IC_Universal	Philips			SOT313	IC1
17	2	BLM32A07	BLM32	CBD	Murata			BLM32	L1, L7
18	12	142-0801-811	SMA Launcher	COAX	EF Johnson			SMA	P3,P4,P5, P6,P9,P10, P11,P12, P13,014, P16,P17

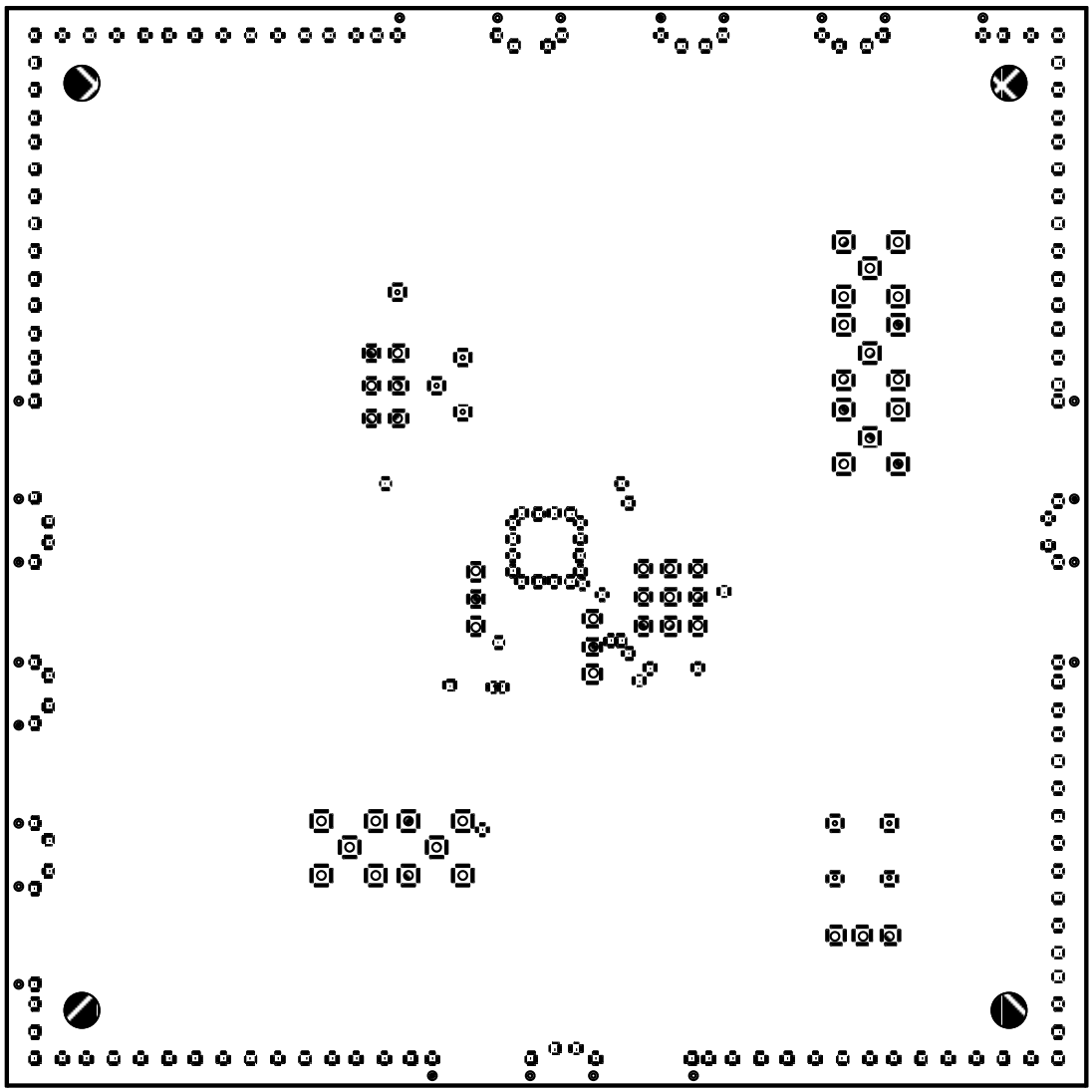
DEMO BOARD ASSEMBLY DRAWING



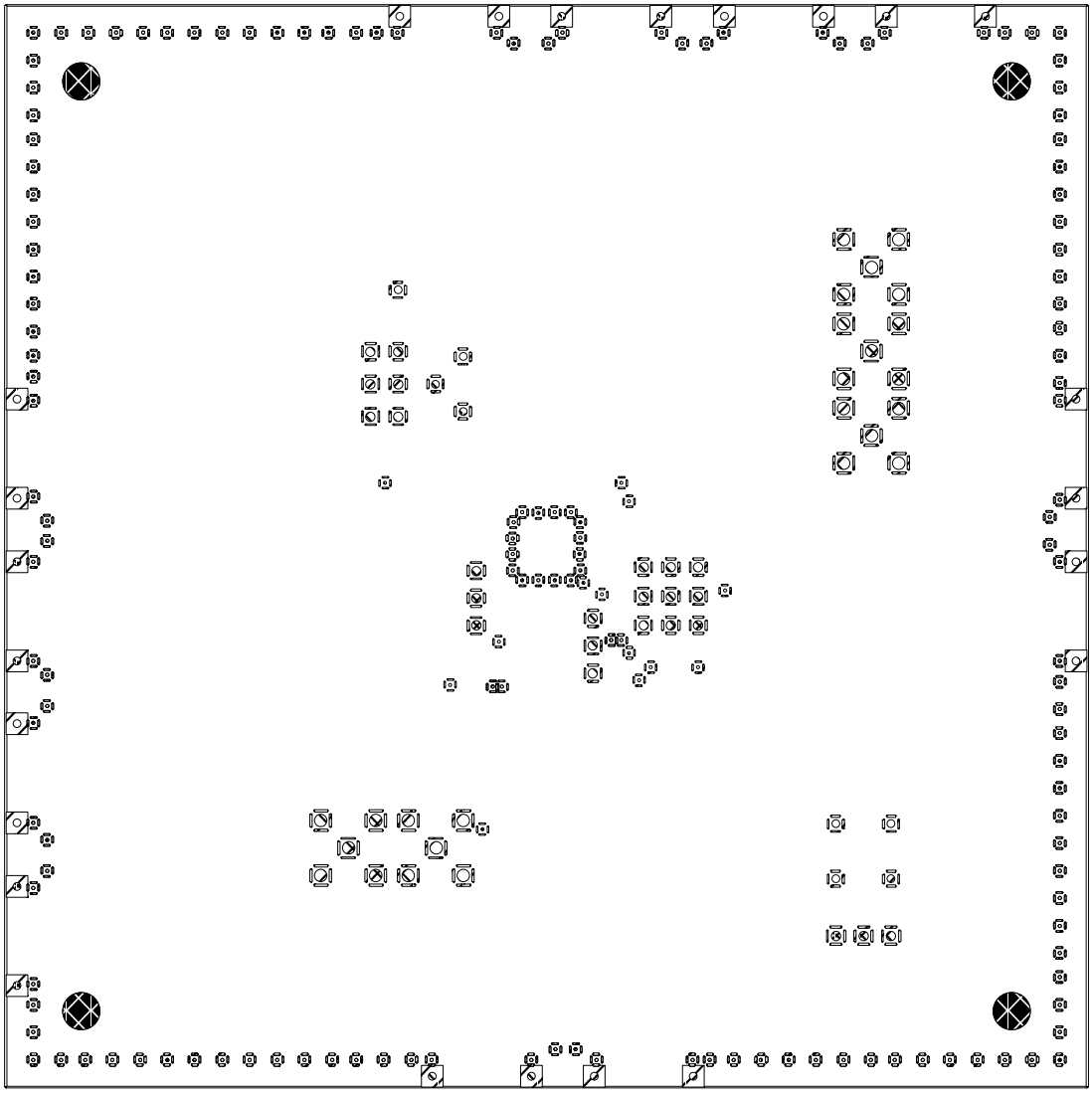
LAYOUT: TOP LAYER, SIGNAL LAYER



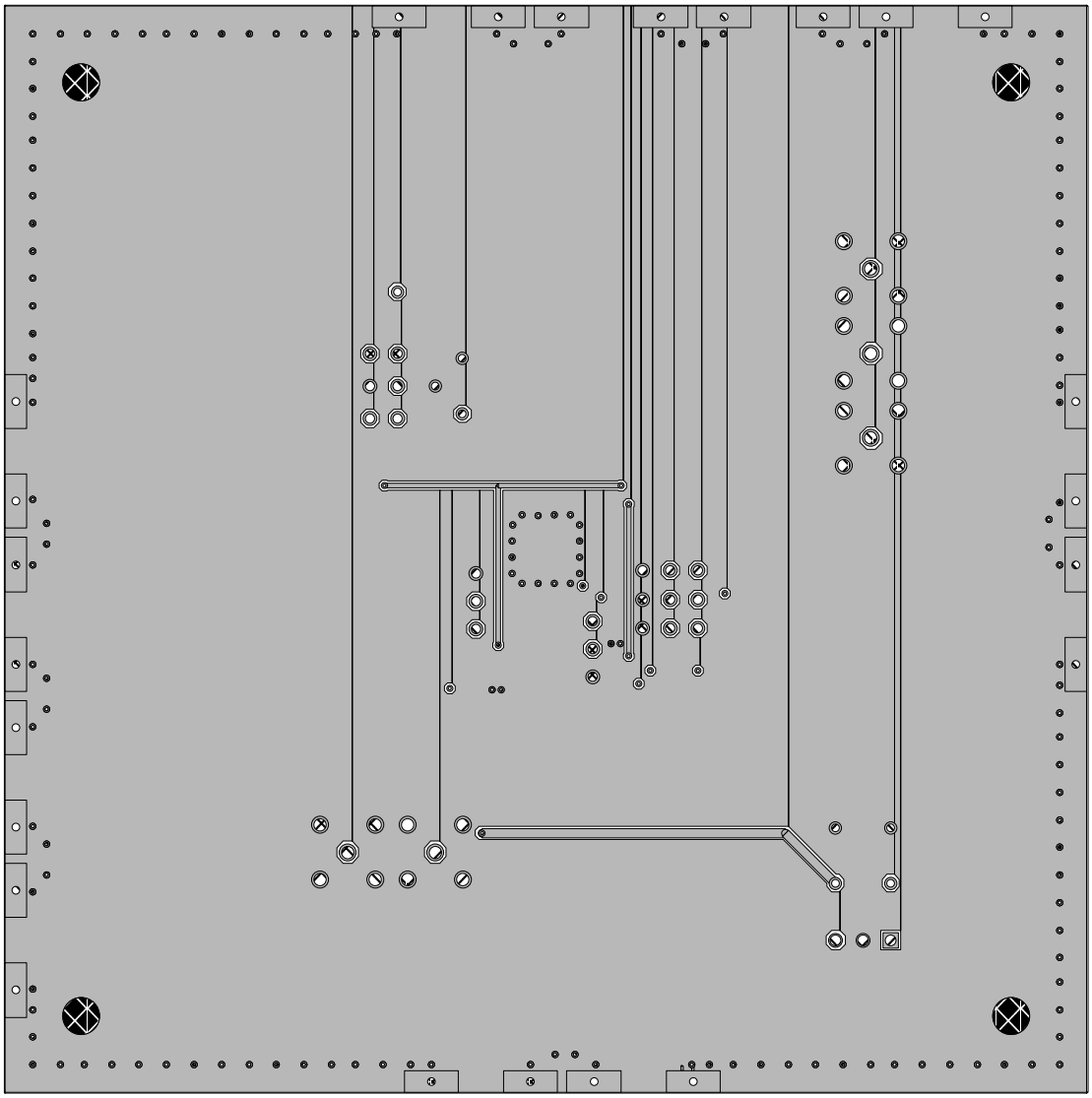
LAYOUT: 2ND LAYER, GROUND LAYER (NEGATIVE PROJECTION)



LAYOUT: 3RD LAYER, SUPPLY LAYER (NEGATIVE PROJECTION)



LAYOUT: BOTTOM LAYER, GND & SIGNAL LAYER



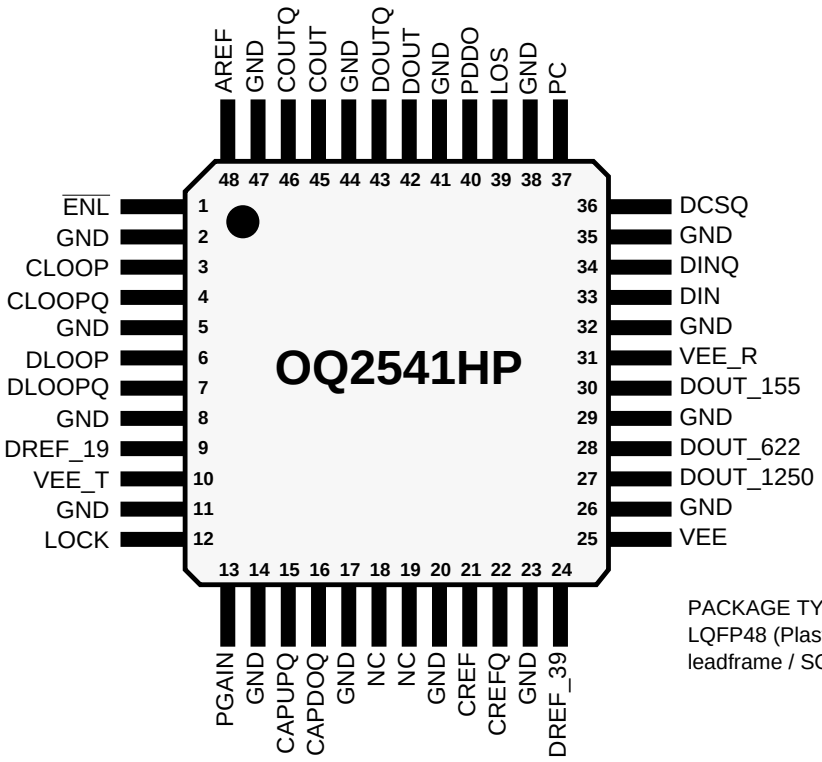
PINNING

SYMBOL	PIN	DESCRIPTION	TYPE(1)
$\overline{ENL}$	1	enable loop mode	I
GND	2	ground	S
CLOOP	3	non-inverting clock output in loop mode	O
CLOOPQ	4	inverting clock output in loop mode	O
GND	5	ground	S
DLOOP	6	non-inverting data output in loop mode	O
DLOOPQ	7	inverting data output in loop mode	O
GND	8	ground	S
DREF_19	9	enable frequency divider 2: f_{ref} = 19 MHz	I
VEE_T	10	supply voltage in clock conversion mode	S
GND	11	ground	S
LOCK	12	lock detect	O
PGAIN	13	proportional gain of phase detector	I
GND	14	ground	S
CAPUPQ	15	external loop filter capacitor	I
CAPDOQ	16	external loop filter capacitor return	I
GND	17	ground	S
n.c.	18	not connected	–
n.c.	19	not connected	–
GND	20	ground	S
CREF	21	non-inverting reference clock input	I
CREFQ	22	inverting reference clock input	I
GND	23	ground	S
DREF_39	24	enable frequency divider 2: f_{ref} = 39 MHz	I
V_{EE}	25	negative power supply	S
GND	26	ground	S
DOUT_1250	27	enable frequency divider 1: f_{out} = 1250 MHz	I
DOUT_622	28	enable frequency divider 1: f_{out} = 622 MHz	I
GND	29	ground	S
DOUT_155	30	enable frequency divider 1: f_{out} = 155 MHz	I
VEE_R	31	supply voltage in data & clock recovery mode	S
GND	32	ground	S
DIN	33	non-inverting data input	I
DINQ	34	inverting data input	I
GND	35	ground	S
DCSQ	36	DC sense for offset control	O
PC	37	power controller output	A
GND	38	ground	S

SYMBOL	PIN	DESCRIPTION	TYPE(1)
LOS	39	loss of signal	O
PDDO	40	phase detector output	O
GND	41	ground	S
DOUT	42	non-inverting data output	O
DOUT Q	43	inverting data output	O
GND	44	ground	S
COUT	45	non-inverting clock output	O
COUTQ	46	inverting clock output	O
GND	47	ground	S
AREF	48	output amplitude adjustment	I

Note

1. Pin type abbreviations: O = output, I = input, S = power supply, A = analog function.



PACKAGE TYPE / NUMBER:
LQFP48 (Plastic) with modified leadframe / SOT 313-2

PREPARING THE DEMO BOARD FOR OPERATION

!! WARNING: ALL RF INPUT AND OUTPUT IC PINS ARE **NOT ESD PROTECTED**. HANDLE THE DEMONSTRATION BOARD ACCORDING TO STANDARD ESD HANDLING PROCEDURES!

The IC can be operated in clock conversion mode or in data & clock recovery mode. Depending on the functional mode prepare the board as follows:

Clock conversion mode (CC):	mount R5	&	do not mount R3
Data & clock recovery mode (DCR):	mount R3	&	do not mount R5

!! WARNING: R3 AND R5 SHOULD NOT BE MOUNTED SIMULTANEOUSLY. THIS CAN DAMAGE THE IC!

Adjust the supply voltages to their nominal values before connecting the power cable to the board, i.e. V_{EE} = -4.5V and V_{CC} = 5V.

Unless mentioned otherwise, all RF connections have to be terminated with 50Ω.

JUMPER TABLES

Several IC settings can be selected by means of jumpers, according to the tables below, where ‘0’ indicates an open jumper and ‘1’ indicates a closed jumper.

Normal mode vs. loop mode

FUNCTIONAL MODE	J1(VCC)	J2(GND)	J3(VEE)	DOUT(Q)	COUT(Q)	DLOOP(Q)	CLOOP(Q)
DCR	1	0	0	ENabled	ENabled	DISabled	DISabled
DCR	0	1	0	DISabled	DISabled	ENabled	ENabled
DCR	0	0	1	ENabled	ENabled	ENabled	ENabled
CC	1	0	0	n.a.	ENabled	n.a.	DISabled
CC	0	1	0	n.a.	DISabled	n.a.	ENabled
CC	0	0	1	n.a.	ENabled	n.a.	ENabled

Division factor of frequency divider 1, bit rate selection in DCR mode

DIVISION FACTOR	BIT RATE	DOUT_155 (J4)	DOUT_622 (J6)	DOUT_1250 (J7)
1	STM16	GND	GND	GND
2		GND	GND	V_{EE}
4	STM4	GND	V_{EE}	V_{EE}
16	STM1	V_{EE}	V_{EE}	V_{EE}

Division factor of frequency divider 2, reference frequency selection

DIVISION FACTOR	DREF_19 (J5)	DREF_39 (J8)
4	GND	GND
64	GND	V_{EE}
128	V_{EE}	V_{EE}

Clock conversion modes

CONVERSION	DOUT_155	DOUT_622	DOUT_1250	DREF_19	DREF_39
622.08→ 2488.32 MHz	GND	GND	GND	GND	GND

FUNCTIONAL TEST: DCR MODE

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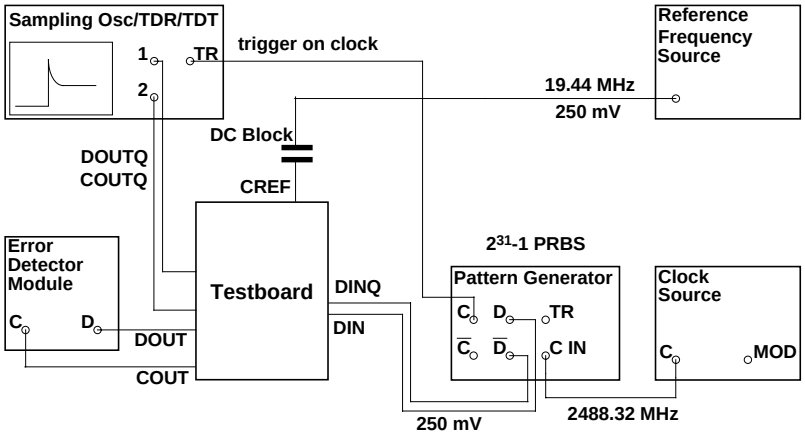
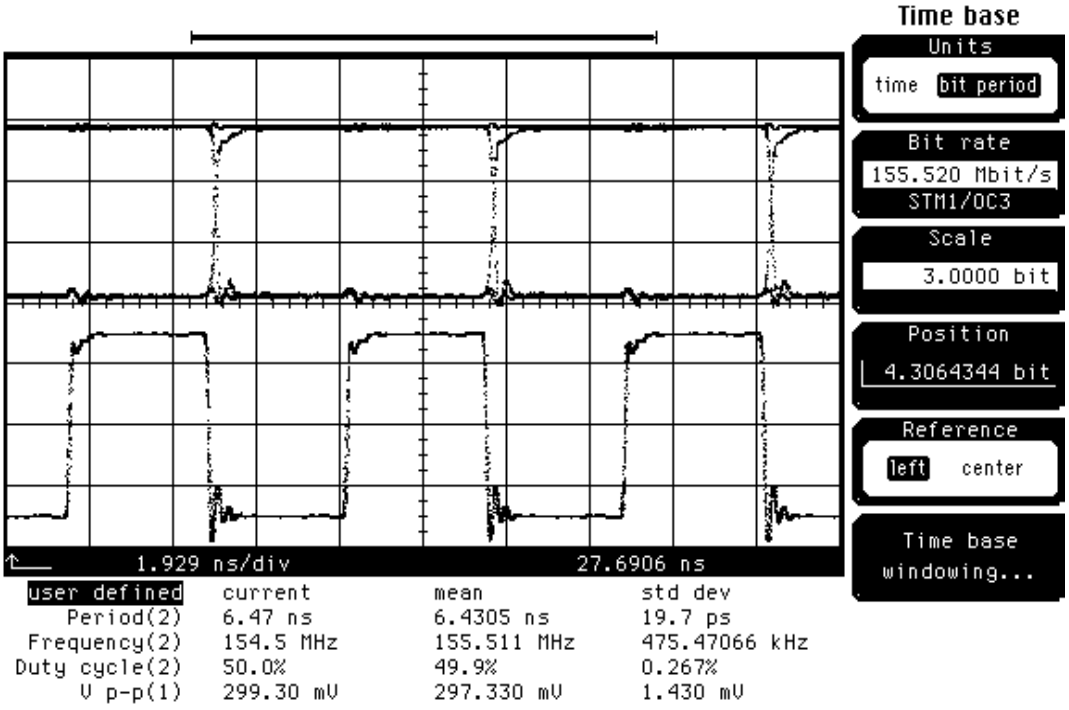
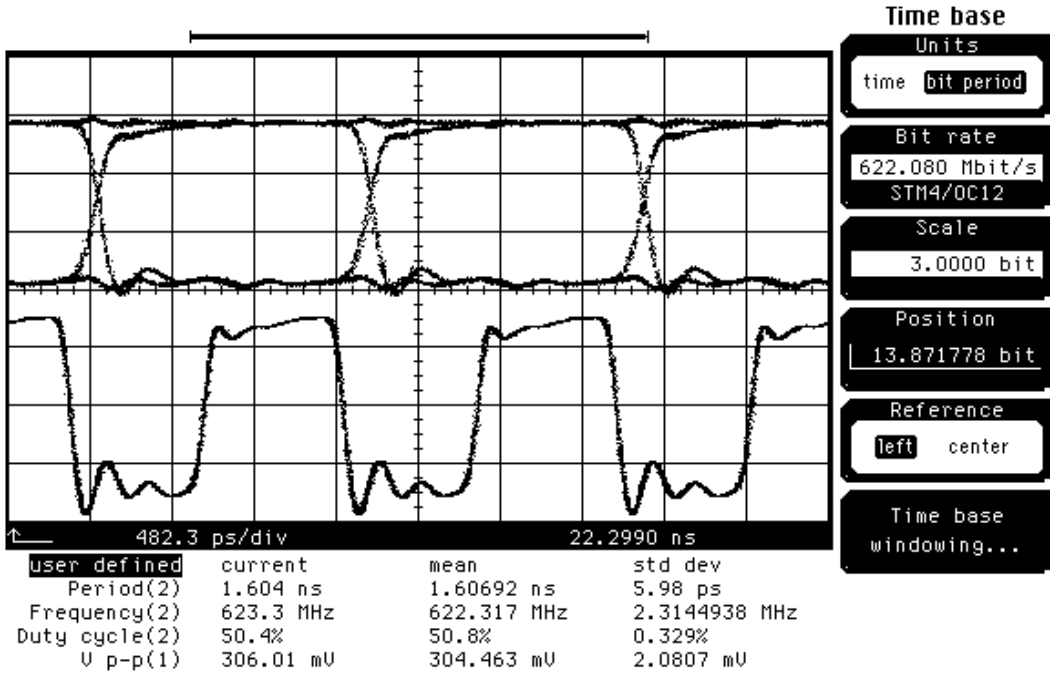
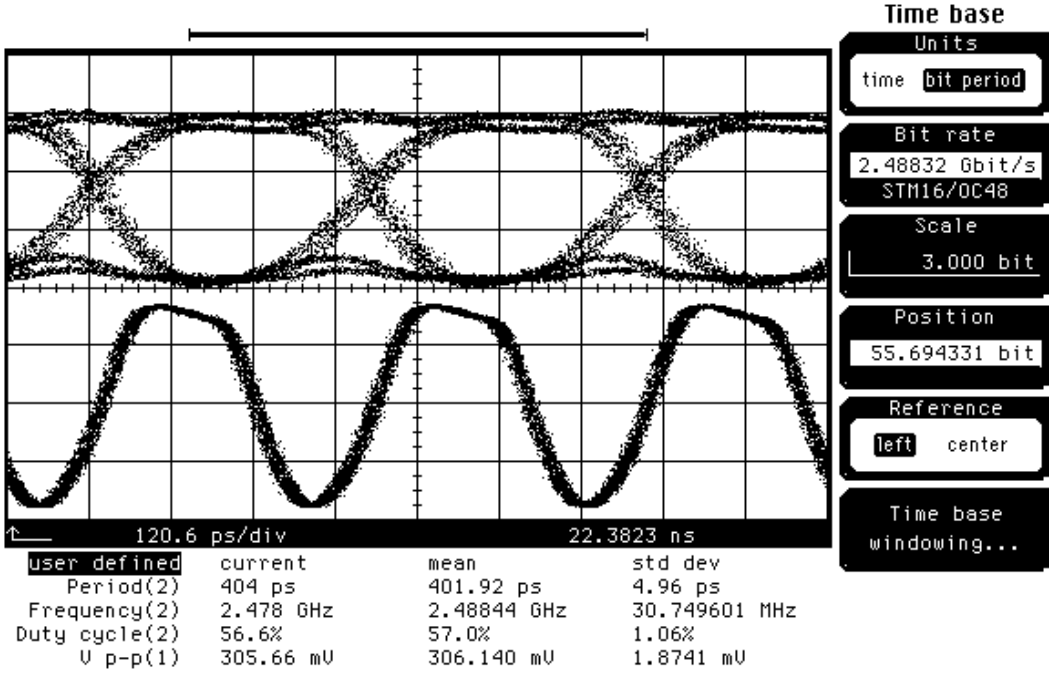


Above:Functional test setup: Data &clock conversion mode
Below: Data eye diagram (upper) and recovered clock (lower) for an STM1 (155 Mb/s) application
Next Page: Recovered data and clock for an STM4 (155 Mb/s upper plot) and an STM16 (2.5 Gb/s lower plot) application





user defined	current	mean	std dev
Period(2)	1.604 ns	1.60692 ns	5.98 ps
Frequency(2)	623.3 MHz	622.317 MHz	2.3144938 MHz
Duty cycle(2)	50.4%	50.8%	0.329%
V p-p(1)	306.01 mV	304.463 mV	2.0807 mV



user defined	current	mean	std dev
Period(2)	404 ps	401.92 ps	4.96 ps
Frequency(2)	2.478 GHz	2.48844 GHz	30.749601 MHz
Duty cycle(2)	56.6%	57.0%	1.06%
V p-p(1)	305.66 mV	306.140 mV	1.8741 mV

FUNCTIONAL TEST: CC MODE

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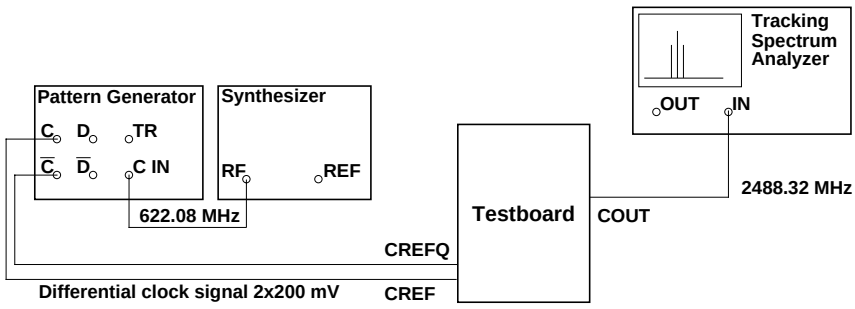

Above: Functional test setup: Clock conversion mode

Below: Typical clock conversion output for an STM16 application