

Speed+us™ Unity Gain Stable, Wideband VOLTAGE LIMITING AMPLIFIER

FEATURES

- HIGH LINEARITY NEAR LIMITING
- FAST RECOVERY FROM OVERDRIVE: 2.4ns
- LIMITING VOLTAGE ACCURACY: $\pm 15\text{mV}$
- -3dB BANDWIDTH ($G = +1$): 530MHz
- SLEW RATE: $1000\text{V}/\mu\text{s}$
- $\pm 5\text{V}$ AND 5V SUPPLY OPERATION
- HIGH GAIN VERSION: OPA689

DESCRIPTION

The OPA688 is a wideband, unity gain stable voltage feedback op amp that offers bipolar output voltage limiting. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to $\pm 15\text{mV}$. The op amp operates linearly to within 30mV of the output limit voltages.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 2.4ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to

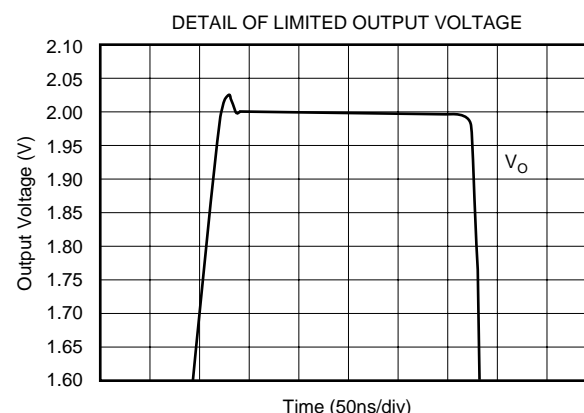
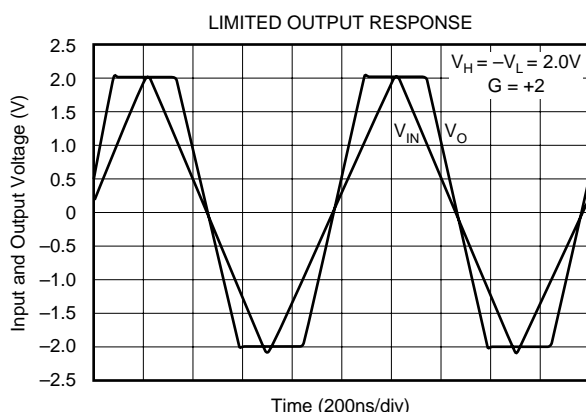
APPLICATIONS

- FAST LIMITING ADC INPUT BUFFER
- CCD PIXEL CLOCK STRIPPING
- VIDEO SYNC STRIPPING
- HF MIXER
- IF LIMITING AMPLIFIER
- AM SIGNAL GENERATION
- NON-LINEAR ANALOG SIGNAL PROCESSING
- COMPARATOR

the input, gives the specified limiting accuracy for any gain, and allows the OPA688 to be used in all standard op amp applications.

Non-linear analog signal processing will benefit from the OPA688's sharp transition from linear operation to output limiting. The quick recovery time supports high speed applications.

The OPA688 is available in an industry standard pinout in 8-pin PDIP and SO-8 packages. For higher gain, or transimpedance applications requiring output limiting with fast recovery, consider the OPA689.



SPECIFICATIONS— $V_S = \pm 5V$

G = +2, $R_L = 500\Omega$, $R_F = 402\Omega$, $V_H = -V_L = 2V$ (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA688U, P						TEST LEVEL ⁽²⁾
		TYP	GUARANTEED ⁽¹⁾					
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 1)								
Small Signal Bandwidth	V _O < 0.2Vp-p G = +1, R _F = 25Ω	530	—	—	—	MHz	Typ	C
	G = +2	260	150	140	135	MHz	Min	B
	G = –1	230	—	—	—	MHz	Typ	C
Gain-Bandwidth Product (G ≥ +5)	V _O < 0.2Vp-p	290	175	170	160	MHz	Min	B
Gain Peaking	G = +1, R _F = 25Ω, V _O < 0.2Vp-p	11	—	—	—	dB	Typ	C
0.1dB Gain Flatness Bandwidth	V _O < 0.2Vp-p	50	—	—	—	MHz	Typ	C
Large Signal Bandwidth	V _O = 4Vp-p, V _H = –V _L = 2.5V	145	100	95	90	MHz	Min	B
Step Response:								
Slew Rate	4V Step, V _H = –V _L = 2.5V	1000	800	770	650	V/μs	Min	B
Rise/Fall Time	0.2V Step	1.2	2.6	2.7	3	ns	Max	B
Settling Time: 0.05%	2V Step	7	—	—	—	ns	Typ	C
Spurious Free Dynamic Range	f = 5MHz, V _O = 2Vp-p	66	62	58	53	dB	Min	B
Differential Gain	NTSC, PAL, R _L = 500Ω	0.02	—	—	—	%	Typ	C
Differential Phase	NTSC, PAL, R _L = 500Ω	0.01	—	—	—	°	Typ	C
Input Noise:								
Voltage Noise Density	f ≥ 1MHz	6.3	7.2	7.8	8	nV/√Hz	Max	B
Current Noise Density	f ≥ 1MHz	2.0	2.5	2.9	3.6	pA/√Hz	Max	B
DC PERFORMANCE (V_{CM} = 0)								
Open Loop Voltage Gain (A _{OL})	V _O = ±0.5V	54	48	46	45	dB	Min	A
Input Offset Voltage		±2	±6	±7	±9	mV	Max	A
Average Drift		—	—	±14	±14	μV/°C	Max	B
Input Bias Current ⁽³⁾		+6	±12	±13	±20	μA	Max	A
Average Drift		—	—	–60	–90	nA/°C	Max	B
Input Offset Current		±0.3	±2	±3	±4	μA	Max	A
Average Drift		—	—	±10	±10	nA/°C	Max	B
INPUT								
Common-Mode Rejection	Input Referred, V _{CM} = ±0.5V	57	50	49	47	dB	Min	A
Common-Mode Input Range ⁽⁴⁾		±3.3	±3.2	±3.2	±3.1	V	Min	A
Input Impedance								
Differential-Mode		0.4 1	—	—	—	MΩ pF	Typ	C
Common-Mode		1 1	—	—	—	MΩ pF	Typ	C
OUTPUT								
Output Voltage Range	V _H = –V _L = 4.3V R _L ≥ 500Ω	±4.1	±3.9	±3.9	±3.8	V	Min	A
Current Output, Sourcing	V _O = 0	105	90	85	80	mA	Min	A
Sinking	V _O = 0	–85	–70	–65	–60	mA	Min	A
Closed-Loop Output Impedance	G = +1, R _F = 25Ω, f < 100kHz	0.2	—	—	—	Ω	Typ	C
POWER SUPPLY								
Operating Voltage, Specified		±5	—	—	—	V	Typ	C
Maximum		—	±6	±6	±6	V	Max	C
Quiescent Current, Maximum		15.8	17	19	20	mA	Max	A
Minimum		15.8	14	12.8	11	mA	Min	A
Power Supply Rejection Ratio +PSR (Input Referred)	+V _S = 4.5V to 5.5V	65	58	57	55	dB	Min	A
OUTPUT VOLTAGE LIMITERS								
Default Limit Voltage	Pins 5 and 8							
Minimum Limiter Separation (V _H – V _L)	Limiter Pins Open	±3.3	±3.0	±3.0	±2.9	V	Min	A
Maximum Limit Voltage		200	200	200	200	mV	Min	B
		—	±4.3	±4.3	±4.3	V	Max	B
Limiter Input Bias Current Magnitude ⁽⁵⁾	V _O = 0							
Maximum		54	61	64	66	μA	Max	A
Minimum		54	44	43	41	μA	Min	A
Average Drift		—	—	40	45	nA/°C	Max	B
Limiter Input Impedance		2 1	—	—	—	MΩ pF	Typ	C
Limiter Feedthrough ⁽⁶⁾	f = 5MHz	–60	—	—	—	dB	Typ	C
DC Performance in Limit Mode	V _{IN} = ±2V							
Limiter Offset	(V _O – V _H) or (V _O – V _L)	±15	±35	±40	±40	mV	Max	A
Op Amp Input Bias Current Shift ⁽³⁾		3	—	—	—	μA	Typ	C
AC Performance in Limit Mode								
Limiter Small Signal Bandwidth	V _{IN} = ±2V, V _O < 0.02Vp-p	450	—	—	—	MHz	Typ	C
Limiter Slew Rate ⁽⁷⁾		100	—	—	—	V/μs	Typ	C
Limited Step Response								
Overshoot	2x Overdrive V _{IN} = 0 to ±2V Step	250	—	—	—	mV	Typ	C
Recovery Time	V _{IN} = ±2V to 0V Step	2.4	2.8	3.0	3.2	ns	Max	B
Linearity Guardband ⁽⁸⁾	f = 5MHz, V _O = 2Vp-p	30	—	—	—	mV	Typ	C

SPECIFICATIONS— $V_S = \pm 5V$ (CONT)

$G = +2$, $R_L = 500\Omega$, $R_F = 402\Omega$, $V_H = -V_L = 2V$ (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA688U, P						TEST LEVEL ⁽²⁾
		TYP	GUARANTEED ⁽¹⁾					
		+25°C	+25°C	0°C to +70°C	−40°C to +85°C	UNITS	MIN/ MAX	
THERMAL CHARACTERISTICS								
Temperature Range	Specification: P, U	−40 to +85	—	—	—	°C	Typ	C
Thermal Resistance	Junction-to-Ambient							
P 8-Pin DIP		100	—	—	—	°C/W	Typ	C
U 8-Pin SO-8		125	—	—	—	°C/W	Typ	C

NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3, Figure 1 and Figure 8. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when $V_{IN} = 0$. (7) V_H slew rate conditions are: $V_{IN} = +2V$, $G = +2$, $V_L = -2V$, $V_H = \text{step between } 2V \text{ and } 0V$. V_L slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid ($f = 5\text{MHz}$, $V_O = 0V_{DC} \pm 1V_{p-p}$) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

SPECIFICATIONS— $V_S = +5V$

$G = +2$, $R_L = 500\Omega$ tied to $V_{CM} = 2.5V$, $R_F = 402\Omega$, $V_L = V_{CM} - 1.2V$, $V_H = V_{CM} + 1.2V$ (Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA688U, P						TEST LEVEL ⁽²⁾
		TYP	GUARANTEED ⁽¹⁾					
		+25°C	+25°C	0°C to +70°C	−40°C to +85°C	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 2)								
Small Signal Bandwidth	V _O < 0.2Vp-p							
	G = +1, R _F = 25Ω	515	—	—	—	MHz	Typ	C
	G = +2	240	110	105	100	MHz	Min	B
	G = −1	190	—	—	—	MHz	Typ	C
Gain-Bandwidth Product (G ≥ +5)	V _O < 0.2Vp-p	275	130	125	120	MHz	Min	B
Gain Peaking	G = +1, R _F = 25Ω, V _O < 0.2Vp-p	10	—	—	—	dB	Typ	C
0.1dB Gain Flatness Bandwidth	V _O < 0.2Vp-p	50	—	—	—	MHz	Typ	C
Large Signal Bandwidth	V _O = 2Vp-p	240	110	105	100	MHz	Min	B
Step Response:								
Slew Rate	2V Step	1000	800	770	650	V/μs	Min	B
Rise/Fall Time	0.2V Step	2.3	2.6	2.7	3	ns	Max	B
Settling Time: 0.05%	1V Step	12	—	—	—	ns	Typ	C
Spurious Free Dynamic Range	f = 5MHz, V _O = 2Vp-p	64	60	56	51	dB	Min	B
Input Noise:								
Voltage Noise Density	f ≥ 1MHz	6.3	7.2	7.8	8	nV/√Hz	Max	B
Current Noise Density	f ≥ 1MHz	2.0	2.5	2.9	3.6	pA/√Hz	Max	B
DC PERFORMANCE								
Open Loop Voltage Gain (A _{OL})	V _{CM} = 2.5V	54	48	46	45	dB	Min	A
Input Offset Voltage	V _O = ±0.5V	±2	±6	±7	±9	mV	Max	A
Average Drift		—	—	±14	±14	μV/°C	Max	B
Input Bias Current ⁽³⁾		+6	±12	±13	±20	μA	Max	A
Average Drift		—	—	−60	−90	nA/°C	Max	B
Input Offset Current		±0.3	±2	±3	±4	μA	Max	A
Average Drift		—	—	±10	±10	nA/°C	Max	B

SPECIFICATIONS— $V_S = +5V$ (CONT)

$G = +2$, $R_L = 500\Omega$ tied to $V_{CM} = 2.5V$, $R_F = 402\Omega$, $V_L = -1.2V$, $V_H = +1.2V$ (Figure 2 for AC performance only), unless otherwise noted.

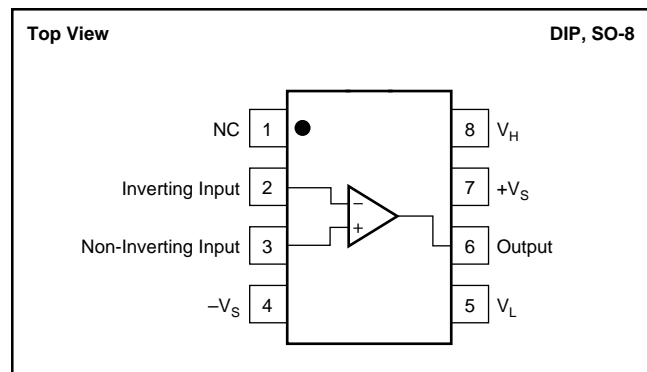
PARAMETER	CONDITIONS	OPA688U, P						TEST LEVEL ⁽²⁾
		TYP	GUARANTEED ⁽¹⁾					
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	
INPUT								
Common-Mode Rejection	Input Referred, V _{CM} = ±0.5V	55	48	47	45	dB	Min	A
Common-Mode Input Range ⁽⁴⁾		V _{CM} ±0.8	V _{CM} ±0.7	V _{CM} ±0.7	V _{CM} ±0.6	V	Min	A
Input Impedance		0.4 1	—	—	—	MΩ pF	Typ	C
Differential-Mode Common-Mode		1 1	—	—	—	MΩ pF	Typ	C
OUTPUT								
Output Voltage Range	V _H = V _{CM} +1.8V, V _L = V _{CM} –1.8V	V _{CM} ±1.6	V _{CM} ±1.4	V _{CM} ±1.4	V _{CM} ±1.3	V	Min	A
Current Output, Sourcing	R _L ≥ 500Ω	70	60	55	50	mA	Min	A
Sinking	V _O = 2.5V	–60	–50	–45	–40	mA	Min	A
Closed-Loop Output Impedance	V _O = 2.5V G = +1, R _F = 25Ω, f < 100kHz	0.2	—	—	—	Ω	Typ	C
POWER SUPPLY								
Operating Voltage, Specified	Single Supply Operation	+5	—	—	—	V	Typ	C
Maximum		—	+12	+12	+12	V	Max	A
Quiescent Current, Maximum		13	15	15	16	mA	Max	A
Minimum		13	11	10	9	mA	Min	A
Power Supply Rejection Ratio +PSR (Input Referred)	V _S = 4.5V to 5.5V	65	—	—	—	dB	Typ	C
OUTPUT VOLTAGE LIMITERS								
Default Limiter Voltage	Pins 5 and 8	V _{CM} ±0.9	V _{CM} ±0.6	V _{CM} ±0.6	V _{CM} ±0.6	V	Min	A
Minimum Limiter Separation (V _H – V _L)	Limiter Pins Open	200	200	200	200	mV	Min	B
Maximum Limit Voltage		—	V _{CM} ±1.8	V _{CM} ±1.8	V _{CM} ±1.8	V	Max	B
Limiter Input Bias Current Magnitude ⁽⁵⁾	V _O = 2.5V							
Maximum		35	60	70	80	μA	Max	A
Minimum		35	0	0	0	μA	Min	A
Average Drift		—	—	30	50	nA/°C	Max	B
Limiter Input Impedance		2 1	—	—	—	MΩ pF	Typ	C
Limiter Feedthrough ⁽⁶⁾	f = 5MHz	–60	—	—	—	dB	Typ	C
DC Performance in Limit Mode	V _{IN} = V _{CM} ±1.2V							
Limiter Voltage Accuracy	(V _O – V _H) or (V _O – V _L)	±15	±35	±40	±40	mV	Max	A
Op Amp Bias Current Shift ⁽³⁾		5	—	—	—	μA	Typ	C
AC Performance in Limit Mode								
Limiter Small Signal Bandwidth	V _{IN} = V _{CM} ±1.2V, V _O < 0.02Vp-p	300	—	—	—	MHz	Typ	C
Limiter Slew Rate ⁽⁷⁾		20	—	—	—	V/μs	Typ	C
Limited Step Response	2x Overdrive							
Overshoot	V _{IN} = V _{CM} to V _{CM} ±1.2V Step	55	—	—	—	mV	Typ	C
Recovery Time	V _{IN} = V _{CM} ±1.2V to V _{CM} Step	15	—	—	—	ns	Max	C
Linearity Guardband ⁽⁸⁾	f = 5MHz, V _O = 2Vp-p	30	—	—	—	mV	Max	C
THERMAL CHARACTERISTICS								
Temperature Range	Specification: P, U	–40 to +85	—	—	—	°C	Typ	C
Thermal Resistance	Junction-to-Ambient							
P 8-Pin DIP		100	—	—	—	°C/W	Typ	C
U 8-Pin SO-8		125	—	—	—	°C/W	Typ	C

NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) I_{VH} (V_H bias current) is negative, and I_{VL} (V_L bias current) is positive, under these conditions. See Note 3, Figures 2, and Figure 8. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when $V_{IN} = 0$. (7) V_H slew rate conditions are: $V_{IN} = V_{CM} + 0.4V$, $G = +2$, $V_L = V_{CM} - 1.2V$, $V_H =$ step between $V_{CM} + 1.2V$ and V_{CM} . V_L slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid ($f = 5MHz$, $V_O = V_{CM} \pm 1V_{p-p}$) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 6.5V$
Internal Power Dissipation	See Thermal Characteristics
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Limiter Voltage Range	$\pm(V_S - 0.7V)$
Storage Temperature Range: P, U	$-40^{\circ}C$ to $+125^{\circ}C$
Lead Temperature (DIP, soldering, 10s)	$+300^{\circ}C$
(SO-8, soldering, 3s)	$+260^{\circ}C$
Junction Temperature	$+175^{\circ}C$

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE/ORDERING INFORMATION

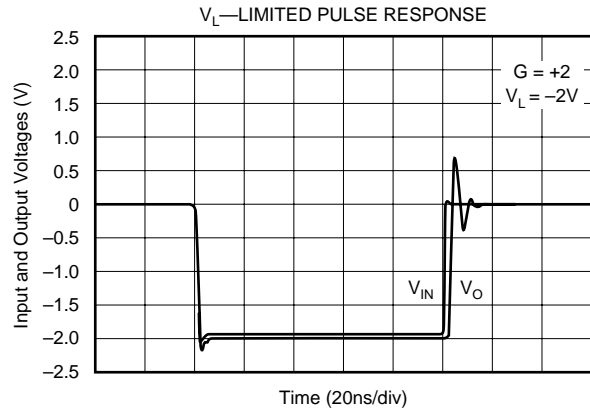
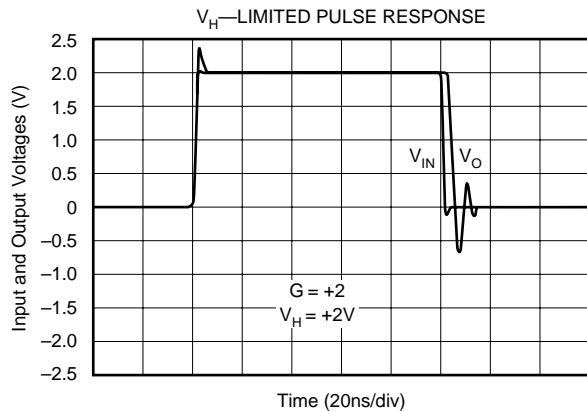
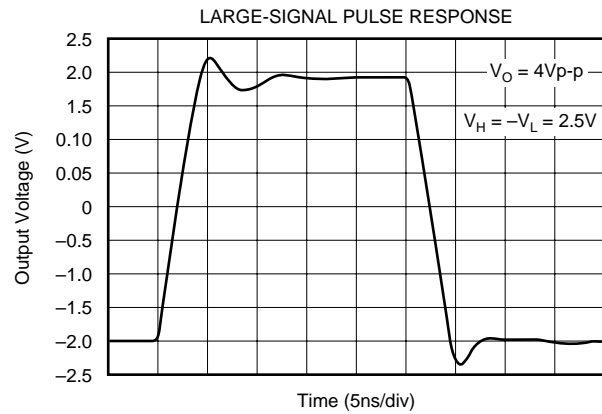
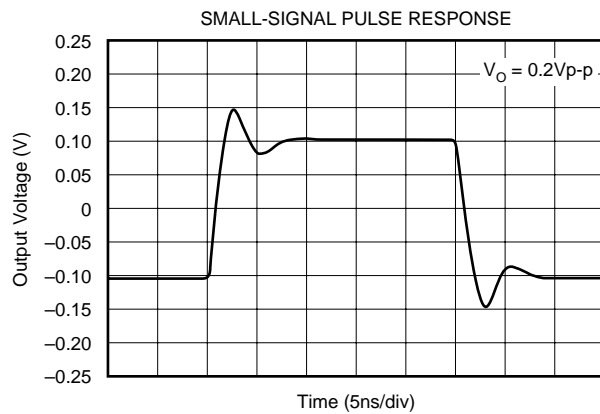
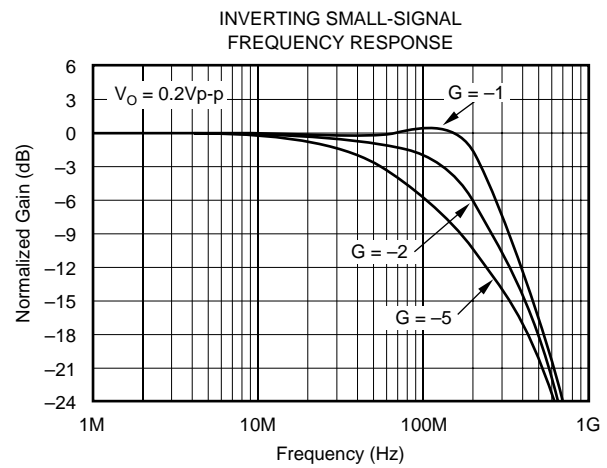
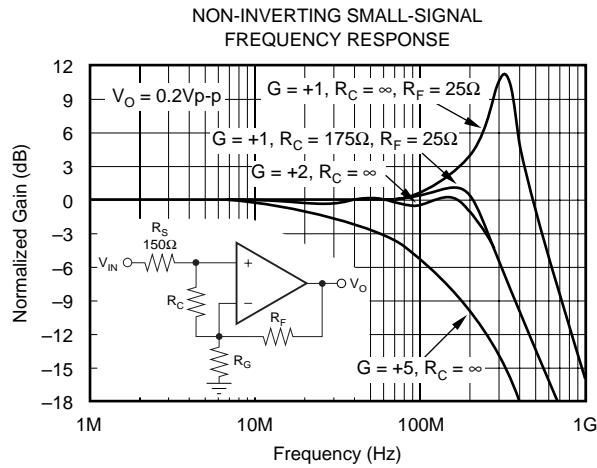
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA
OPA688P	8-Pin Plastic DIP	006	$-40^{\circ}C$ to $+85^{\circ}C$	OPA688P	OPA688P	Rails
OPA688U	SO-8 Surface Mount	182	$-40^{\circ}C$ to $+85^{\circ}C$	OPA688U	OPA688U	Rails
"	"	"	"	"	OPA688U/2K5	Rails

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of OPA688U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

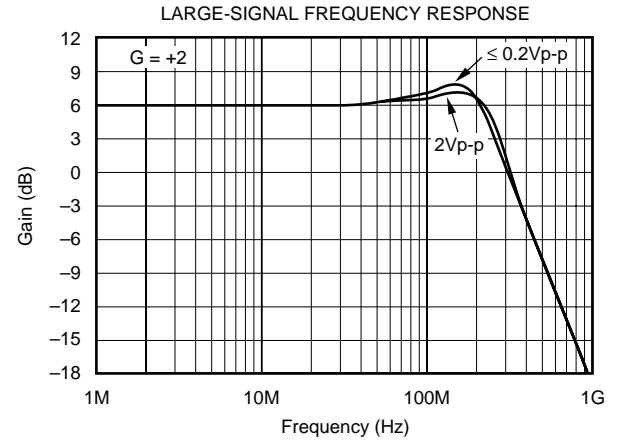
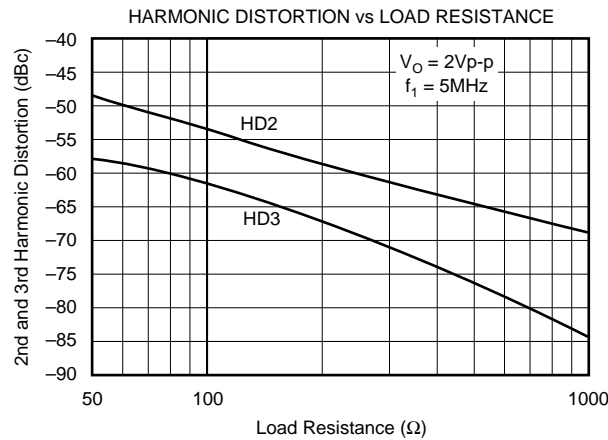
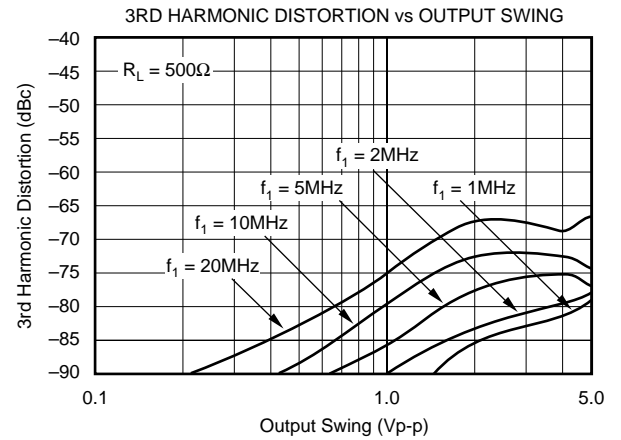
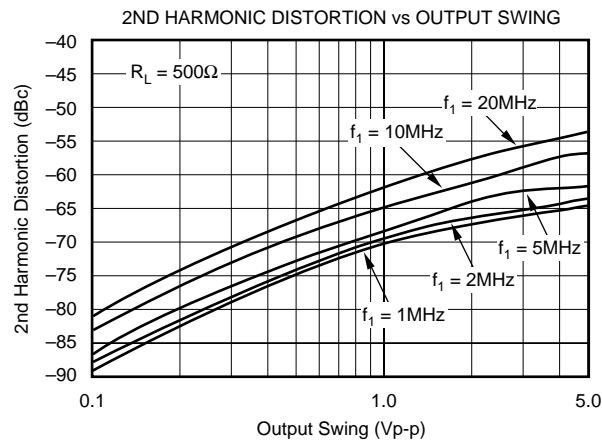
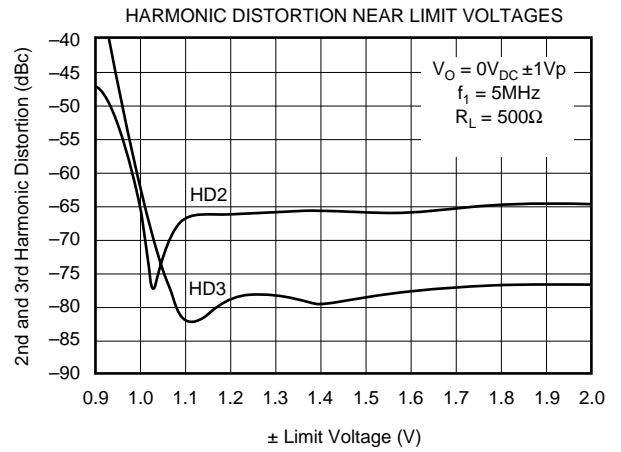
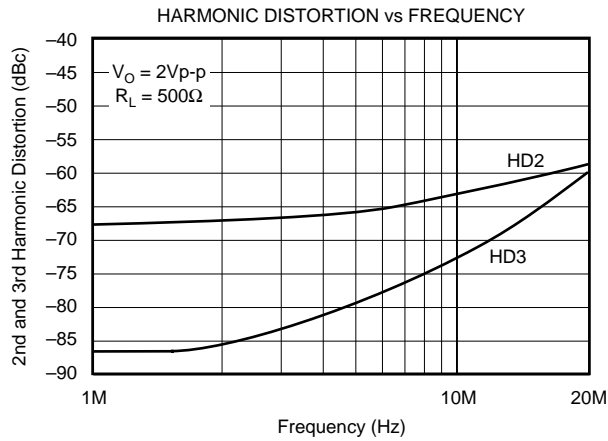
TYPICAL PERFORMANCE CURVES— $V_S = \pm 5V$

$G = +2$, $R_L = 500\Omega$, $R_F = 402\Omega$, $V_H = -V_L = 2V$ (Figure 1 for AC performance only), unless otherwise noted.



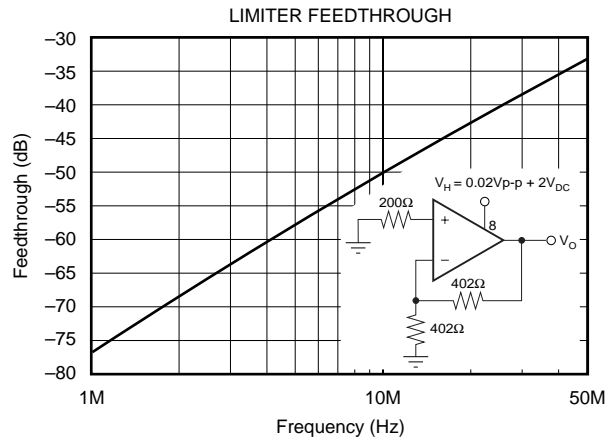
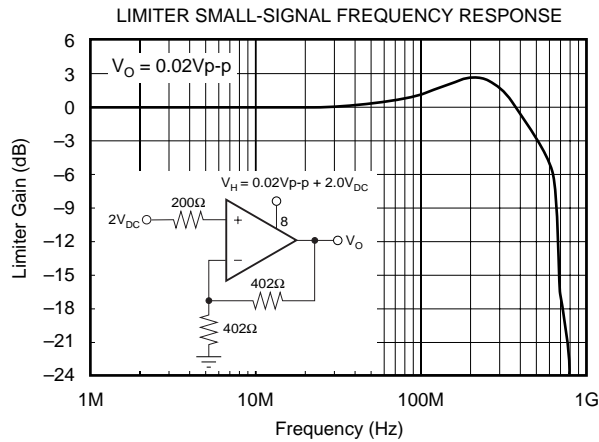
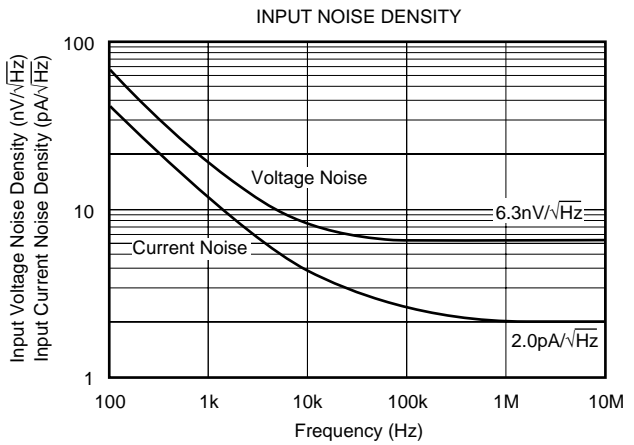
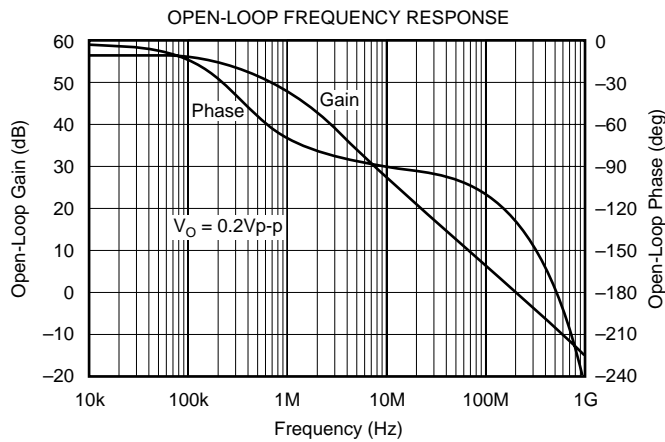
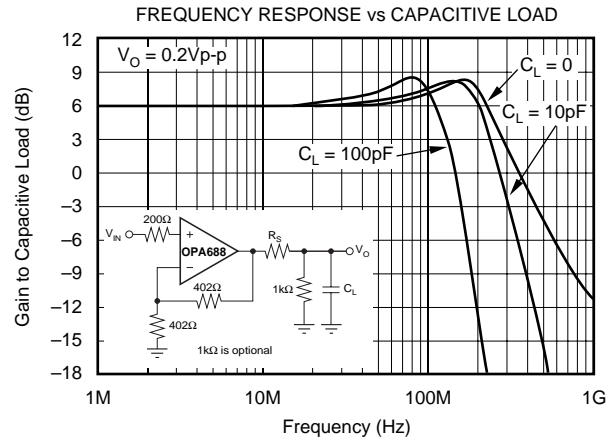
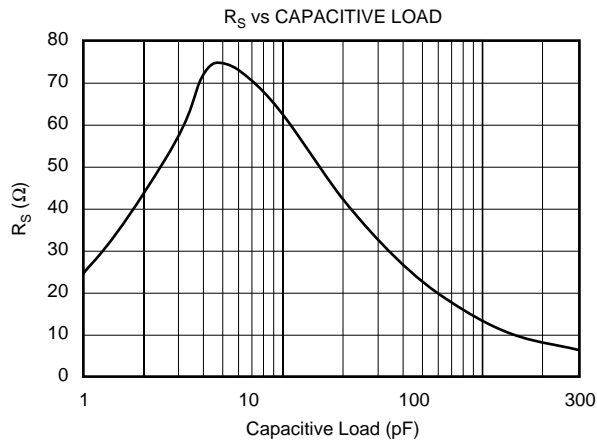
TYPICAL PERFORMANCE CURVES— $V_S = \pm 5V$ (CONT)

$G = +2$, $R_L = 500\Omega$, $R_F = 402\Omega$, $V_H = -V_L = 2V$ (Figure 1 for AC performance only), unless otherwise noted.



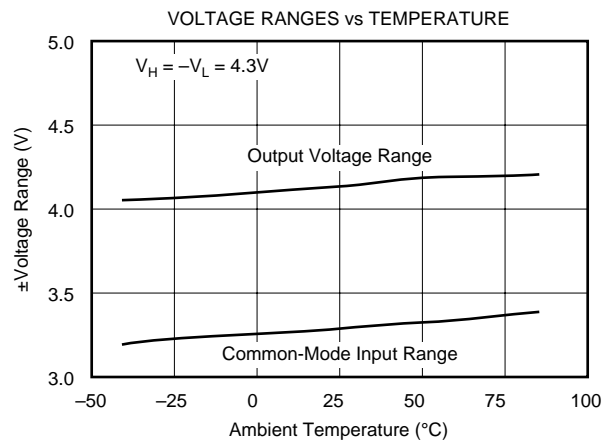
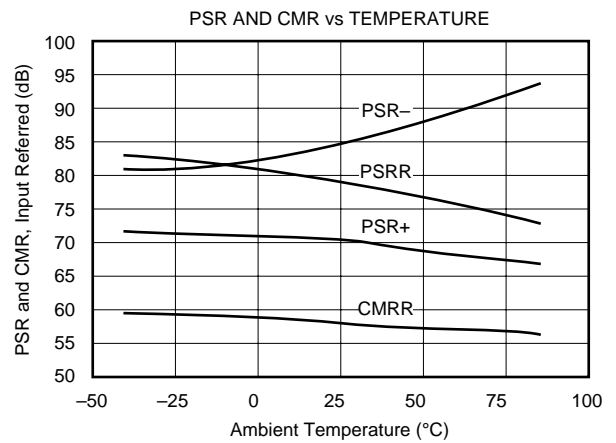
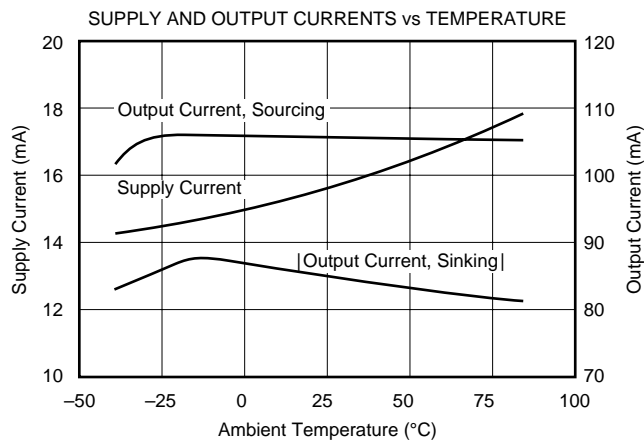
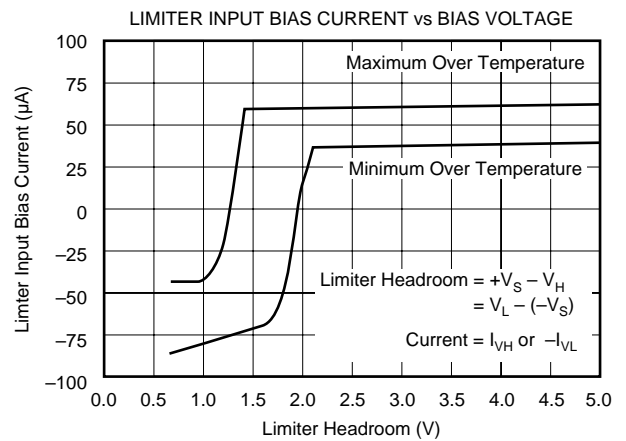
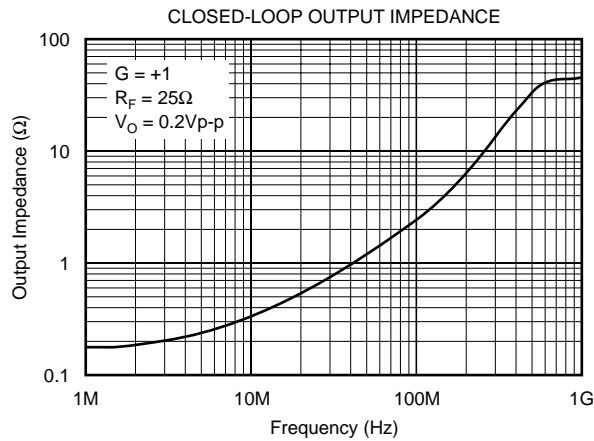
TYPICAL PERFORMANCE CURVES— $V_S = \pm 5V$ (CONT)

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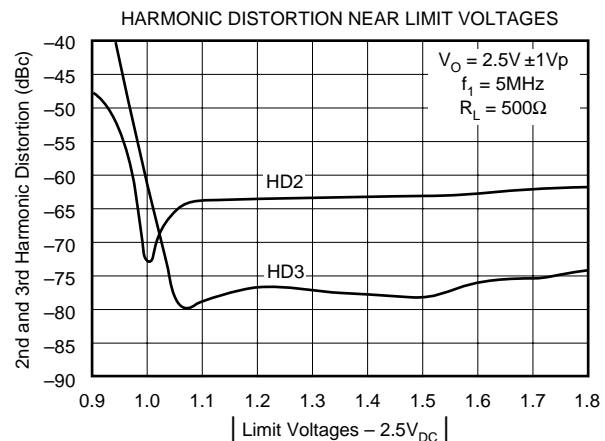
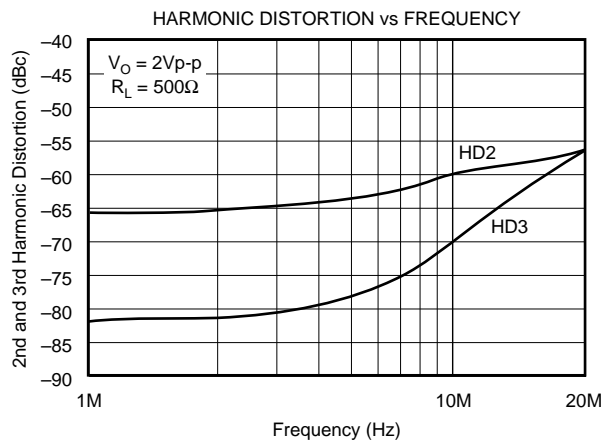
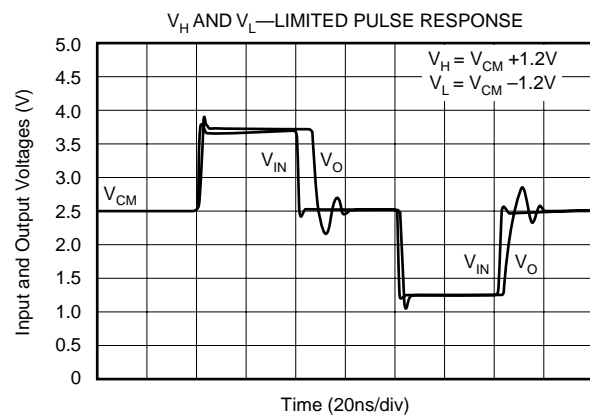
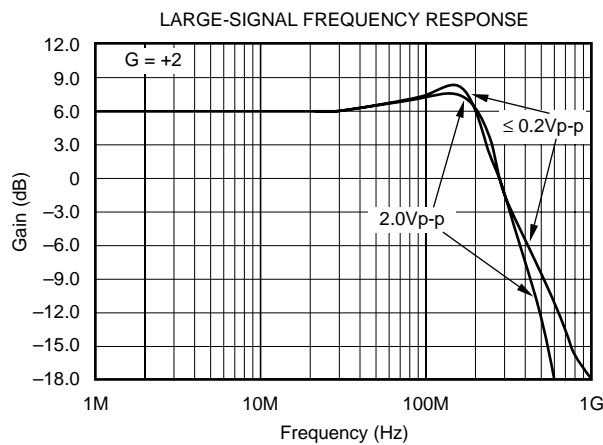
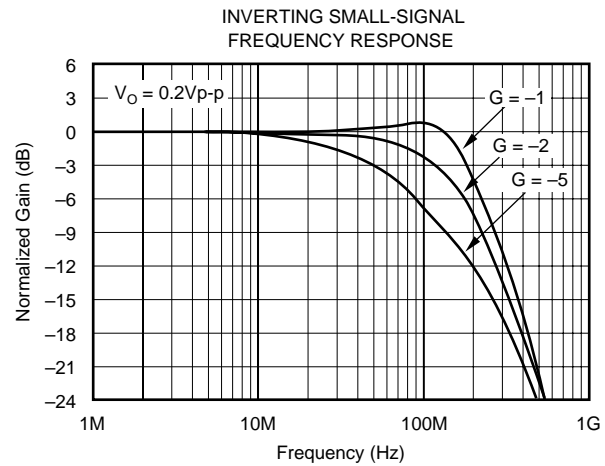
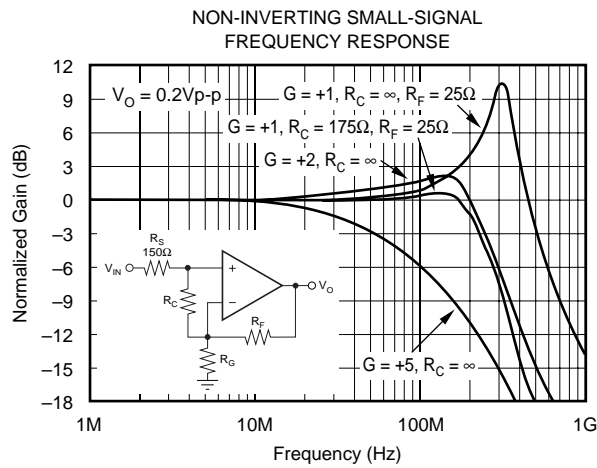
TYPICAL PERFORMANCE CURVES— $V_S = \pm 5V$ (CONT)

$G = +2$, $R_L = 500\Omega$, $R_F = 402\Omega$, $V_H = -V_L = 2V$ (Figure 1 for AC performance only), unless otherwise noted.



TYPICAL PERFORMANCE CURVES— $V_S = +5V$

$G = +2$, $R_F = 402\Omega$, $R_L = 500\Omega$ tied to $V_{CM} = 2.5V$, $V_L = V_{CM} - 1.2V$, $V_H = V_{CM} + 1.2V$, (Figure 2 for AC performance only), unless otherwise noted.



TYPICAL APPLICATIONS

DUAL SUPPLY, NON-INVERTING AMPLIFIER

Figure 1 shows a non-inverting gain amplifier for dual supply operation. This circuit was used for AC characterization of the OPA688, with a 50Ω source, which it matches, and a 500Ω load. The power supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown.

SINGLE SUPPLY, NON-INVERTING AMPLIFIER

Figure 2 shows an AC coupled, non-inverting gain amplifier for single supply operation. This circuit was used for AC characterization of the OPA688, with a 50Ω source, which

it matches, and a 500Ω load. The power supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown. Notice that the single supply circuit can use 3 resistors to set V_H and V_L , where the dual supply circuit usually uses 4 to reference the limit voltages to ground.

LIMITED OUTPUT, ADC INPUT DRIVER

Figure 3 shows a simple ADC driver that operates on single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive.

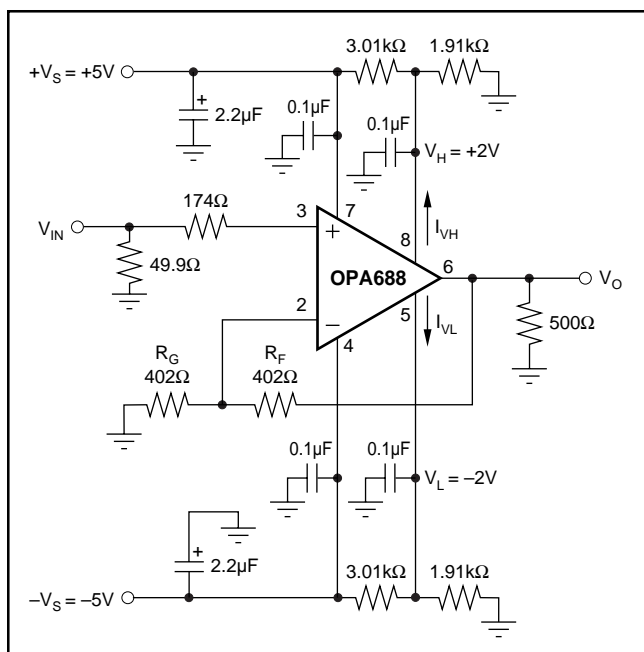


FIGURE 1. DC-Coupled, Dual Supply Amplifier.

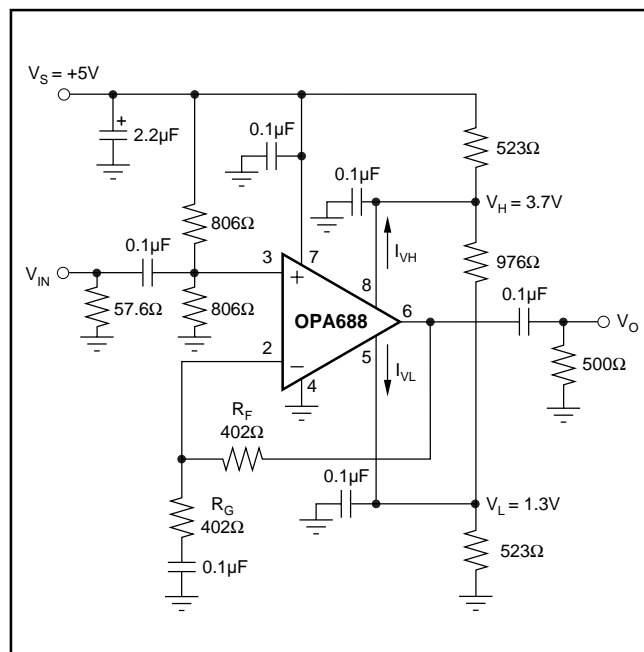


FIGURE 2. AC-Coupled, Single Supply Amplifier.

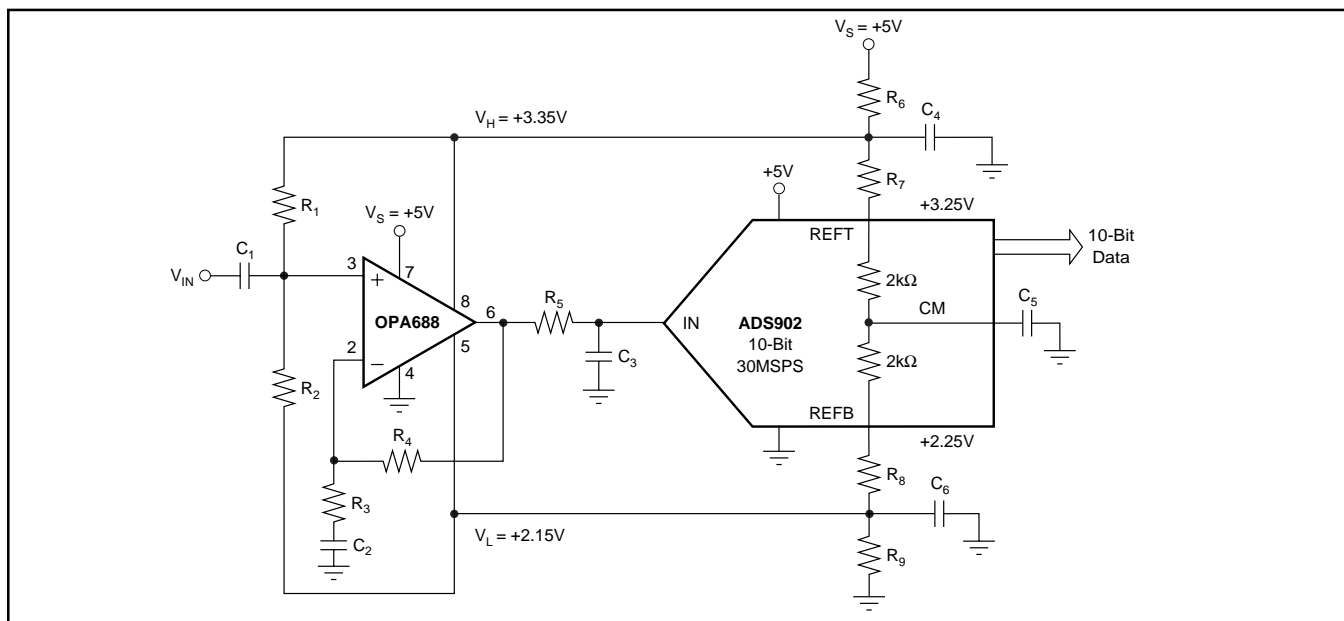


FIGURE 3. Single Supply, Limiting ADC Input Driver.

The recommended component values are:

$$\begin{aligned} R_1 &= R_2 = 210\Omega & R_3 &= R_4 = 402\Omega \\ R_5 &= 24.9\Omega & R_6 &= 536\Omega \\ R_7 &= R_8 = 402\Omega & R_9 &= 698\Omega \\ C_3 &= 100\text{pF} \\ C_1 &= C_2 = C_4 = C_5 = C_6 = 0.1\mu\text{F} \end{aligned}$$

PRECISION HALF WAVE RECTIFIER

Figure 4 shows a half wave rectifier with outstanding precision and speed. V_H (pin 8) will default to a voltage between 3.1 and 3.8V if left open, while the negative limit is set to ground.

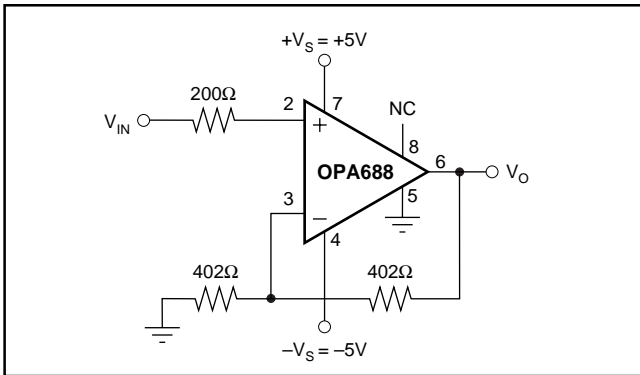


FIGURE 4. Precision Half Wave Rectifier.

VERY HIGH SPEED SCHMITT TRIGGER

Figure 5 shows a very high speed Schmitt trigger. The output levels are precisely defined, and the switching time is exceptional. The output voltage swings between $\pm 2V$.

UNITY-GAIN BUFFER

Figure 6 shows a unity-gain voltage buffer using the OPA688. The feedback resistor (R_F) isolates the output from any board inductance between pins 2 and 6. We recommend that $R_F \geq 24.9\Omega$ for unity-gain buffer applications. R_C is an optional compensation resistor that may reduce the peaking typically seen at $G = +1$. Choosing $R_C = R_S + R_F$ gives a unity gain buffer with approximately the $G = +2$ frequency response.



Figure 7 shows a DC restorer using the OPA688 and OPA660. The OPA660's OTA amplifier is used as a current conveyor (CCII) in this circuit, with a current gain of 1.0. When V_O tries to go below ground, CCII charges C_1 through D_1 , which restores the output back to ground. D_1 adds a propagation delay to the restoration process, which then has an exponential decay with time constant $R_1 C_1 / G$ ($G = +2 =$ the OPA688 gain). When the signal is above ground, it decays to ground with a time constant of $R_2 C_1$. The OPA688 output recovers very quickly from overdrive.

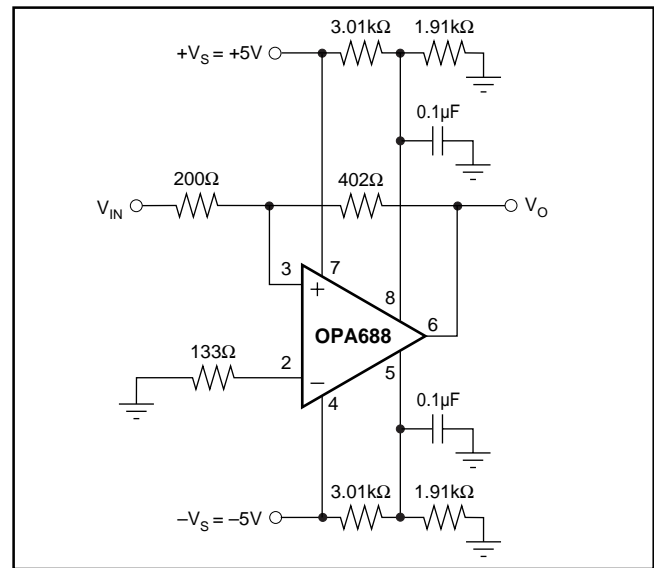


FIGURE 5. Very High Speed Schmitt Trigger.

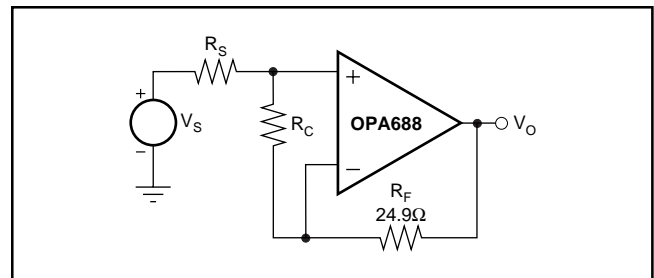


FIGURE 6. Unity-Gain Buffer.

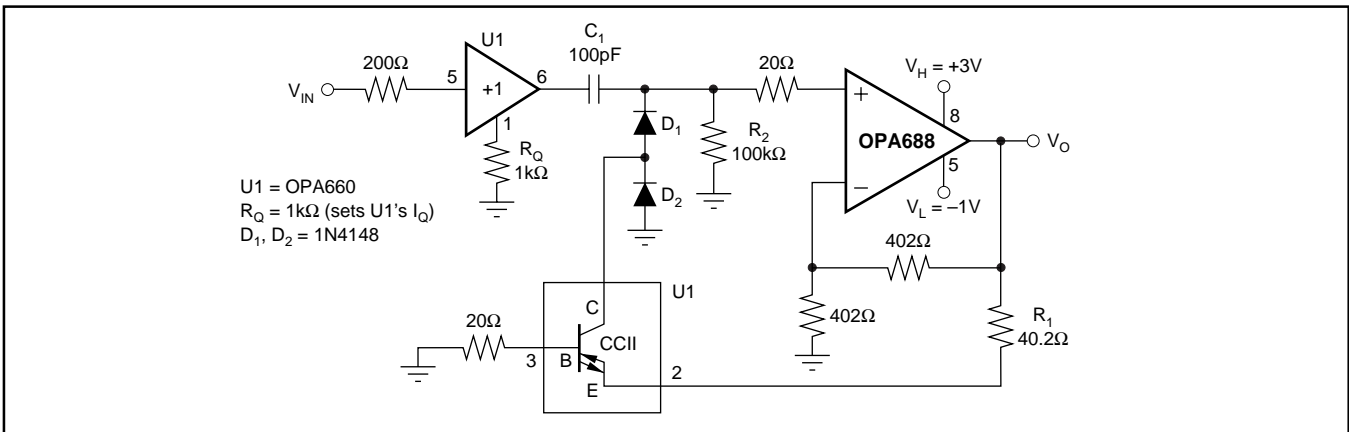


FIGURE 7. DC Restorer.

DESIGN-IN TOOLS

APPLICATIONS SUPPORT

The Burr-Brown Applications Department is available for design assistance at 1-800-548-6132 (US/Canada only). The Burr-Brown Internet web page (<http://www.burr-brown.com>) has the latest data sheets and other design aids.

DEMONSTRATION BOARDS

Two PC boards will be available to assist in the initial evaluation of circuit performance of the OPA688 in both package styles. These are available as an unpopulated PCB with descriptive documentation. See the demonstration board literature for more information. The summary information for these boards is shown below:

DEMONSTRATION BOARD	PACKAGE	PRODUCT	LITERATURE REQUEST NUMBER
DEM-OPA688P DEM-OPA688U	8-Pin DIP SO-8	OPA688P OPA688U	MKT-350 MKT-351

Contact the Burr-Brown Application Department for availability of these boards.

SPICE MODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for high speed active devices, like the OPA688, where parasitic capacitance and inductance can have a major effect on frequency response.

SPICE models will be available through the Burr-Brown web page, or on a disk (call our Application Department). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or differential gain and phase characteristics. These models do not distinguish between the AC performance of different package types.

OPERATING INFORMATION

THEORY OF OPERATION

The OPA688 is a voltage feedback op amp that is unity-gain stable. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain.

The limiters have a very sharp transition from the linear region of operation to output limiting. This allows the limiter voltages to be set very near (<100mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

CIRCUIT LAYOUT

Achieving optimum performance with the high frequency OPA688 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

a) **Minimize parasitic capacitance to any ac ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.

b) **Provide a high quality power supply.** Use linear regulators and power planes to provide power to the supply pins. Place high frequency 0.1μF decoupling capacitors < 0.2" away from the power pins. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2μF to 6.8μF) high frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.

c) **Place external components close** to the OPA688. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.

d) **Use high frequency components** to minimize parasitic elements. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wirewound resistors for high frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances.

Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use RF type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2μF to 6.8μF) should be tantalum for better high frequency and pulse performance.

e) **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2pF parasitic parallel capacitance. For resistors > 1.5kΩ, this adds a pole and/or zero below 500MHz.

Make sure that the output loading is not too heavy. The recommended 402Ω feedback resistor is a good starting point in your design.

f) **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the R_S vs *Capacitive Load* plot. Parasitic loads < 2pF may not need the isolation resistor.

g) **When long traces are necessary**, use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50 Ω transmission line is not required on board—a higher characteristic impedance will help reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This will isolate the source from the reactive load presented by the line, but the frequency response will be degraded.

Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors will alter the transmission line match, and can cause unwanted signal reflections and reactive loading.

h) **Do not use sockets** for high speed parts like the OPA688. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board. If socketing for DIP prototypes is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

POWER SUPPLIES

The OPA688 is nominally specified for operation using either $\pm 5V$ supplies or a single +5V supply. The maximum specified total supply voltage of 12V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow design of non-standard or single supply operation circuits. Figure 2 shows one approach to single-supply operation.

ESD PROTECTION

ESD damage has been known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA688.

OUTPUT LIMITERS

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L , the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L .

Because the limiters act on the output, their accuracy does not change with gain. The transition from the linear region of operation to output limiting is very sharp—the desired output signal can safely come to within 30mV of V_H or V_L with no onset of non-linearity.

The limiter voltages can be set to within 0.7V of the supplies ($V_L \geq -V_S + 0.7V$, $V_H \leq +V_S - 0.7V$). They must also be at least 200mV apart ($V_H - V_L \geq 0.2V$).

When pins 5 and 8 are left open, V_H and V_L go to the Default Voltage Limit; the minimum values are in the spec table. Looking at Figure 8 for the zero bias current case will show the expected range of (V_S – default limit voltages) = headroom.

When the limiter voltages are more than 2.1V from the supplies ($V_L \geq -V_S + 2.1V$ or $V_H \leq +V_S - 2.1V$), you can use simple resistor dividers to set V_H and V_L (see Figure 1). Make sure you include the Limiter Input Bias Currents (Figure 8) in the calculations (i.e., $I_{VL} \approx -50\mu A$ out of pin 5, and $I_{VH} \approx +50\mu A$ out of pin 8). For good limiter voltage accuracy, run at least 1mA quiescent bias current through these resistors.

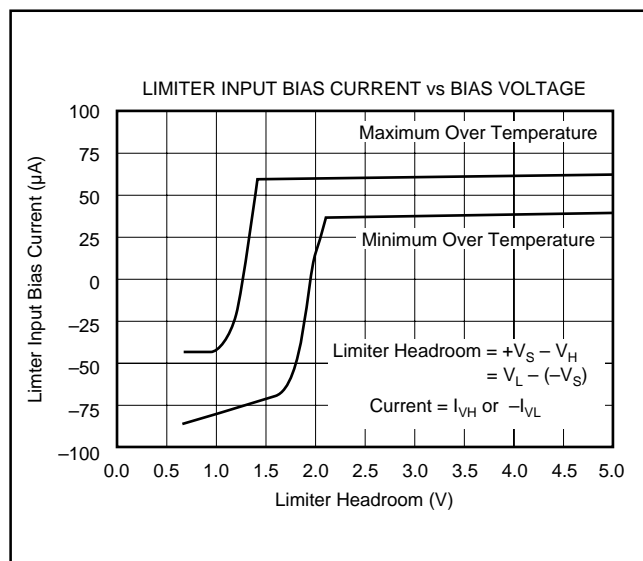


FIGURE 8. Limiter Bias Current vs Bias Voltage.

When the limiter voltages need to be within 2.1V of the supplies ($V_L \leq -V_S + 2.1V$ or $V_H \geq +V_S - 2.1V$), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This will typically be the case for single supply operation ($V_S = +5V$). Figure 2 runs 2.5mA through the resistive divider that sets V_H and V_L . This keeps errors due to I_{VH} and $I_{VL} < \pm 1\%$ of the target limit voltages.

The limiters' DC accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L , can contribute large errors (e.g., $\pm 5\%$). Using a more accurate source, and bypassing pins 5 and 8 with good capacitors, will improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.

Other error sources also contribute, but should have little impact on the limiters' DC accuracy:

- Reduce offsets caused by the Limiter Input Bias Currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path DC errors as contributing to uncertainty in the useable output swing.
- The Limiter Offset Voltage only slightly degrades limiter accuracy.

Figure 9 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages.

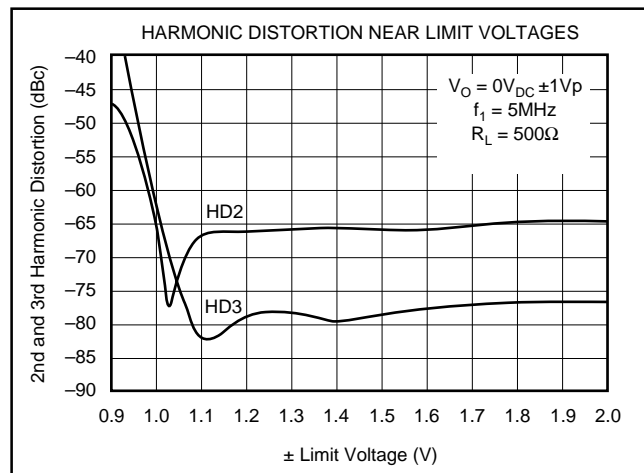


FIGURE 9. Harmonic Distortion Near Limit Voltages.

OFFSET VOLTAGE ADJUSTMENT

The circuit in Figure 10 allows offset adjustment without degrading offset drift with temperature. Use this circuit with caution since power supply noise can inadvertently couple into the op amp.

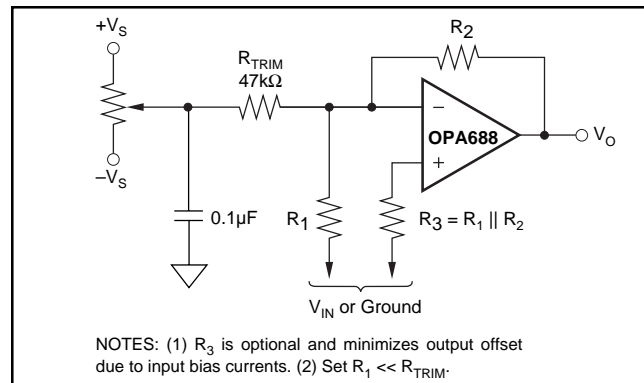


FIGURE 10. Offset Voltage Trim.

Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both DC input bias currents using R_3 . This minimizes the output offset voltage caused by the input bias currents.

OUTPUT DRIVE

The OPA688 has been optimized to drive 500Ω loads, such as A/D converters. It still performs very well driving 100Ω loads; the specifications are shown for the 500Ω load. This makes the OPA688 an ideal choice for a wide range of high frequency applications.

Many high speed applications, such as driving A/D converters, require op amps with low output impedance. As shown in the *Output Impedance vs Frequency* performance curve, the OPA688 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain decreases with frequency.

THERMAL CONSIDERATIONS

The OPA688 will not require heat-sinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at a maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2 / (4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage, and not in the load, that determines internal power dissipation.

The operating junction temperature is: $T_J = T_A + P_D \theta_{JA}$, where T_A is the ambient temperature.

For example, the maximum T_J for a OPA688U with $G = +2$, $R_{FB} = 402\Omega$, $R_L = 100\Omega$, and $\pm V_S = \pm 5V$ at the maximum $T_A = +85^\circ C$ is calculated as:

$$P_{DQ} = (10V \cdot 20mA) = 200mW$$

$$P_{DL} = \frac{(5V)^2}{4 \cdot (100\Omega || 804\Omega)} = 70mW$$

$$P_D = 200mW + 70mW = 270mW$$

$$T_J = 85^\circ C + 270mW \cdot 125^\circ C / W = 119^\circ C$$

CAPACITIVE LOADS

Capacitive loads, such as the input to ADCs, will decrease the amplifier's phase margin, which may cause high frequency peaking or oscillations. Capacitive loads $\geq 2pF$ should be isolated by connecting a small resistor in series

with the output as shown in Figure 11. Increasing the gain from +2 will improve the capacitive drive capabilities due to increased phase margin.

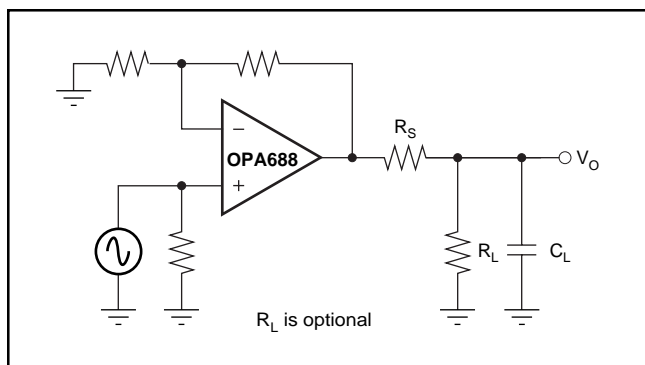


FIGURE 11. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if they are properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

FREQUENCY RESPONSE COMPENSATION

The OPA688 is internally compensated to be unity-gain stable, and has a nominal phase margin of 60° at a gain of +2. Phase margin and peaking improve at higher gains. Recall that an inverting gain of -1 is equivalent to a gain of +2 for bandwidth purposes (i.e., noise gain = 2).

Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a wide bandwidth at high gains, cascade several op amps, or use the high gain optimized OPA689.

In applications where a large feedback resistor is required, such as photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The

bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high gain applications, use a three resistor “Tee” network to reduce the RC time constants set by the parasitic capacitances. Be careful to not increase the noise generated by this feedback network too much.

PULSE SETTLING TIME

The OPA688 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an A/D converter, use the recommended R_S in the R_S vs *Capacitive Load* plot. Extremely fine scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics when recovering from overdrive are very good.

DISTORTION

The OPA688’s distortion performance is specified for a 500Ω load, such as an A/D converter. Driving loads with smaller resistance will increase the distortion as illustrated in Figure 12. Remember to include the feedback network in the load resistance calculations.

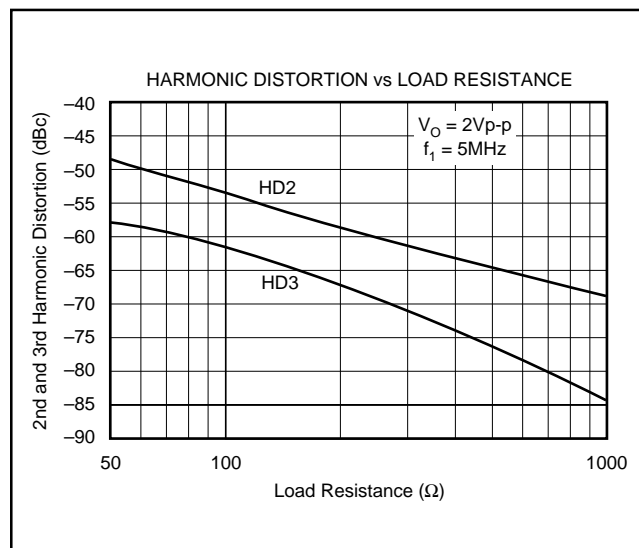


FIGURE 12. 5MHz Harmonic Distortion vs Load Resistance.