Addressable peripheral drivers — NE590/591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has eight Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has eight open-collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin plastic or Cerdip package.

The NE591 has eight open-emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5V V_{CC} supply. The device is packaged in an 18-pin plastic or Cerdip package.

FEATURES

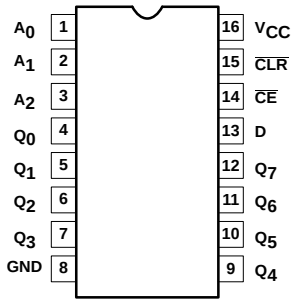
- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 54/74LS259

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

PIN CONFIGURATIONS

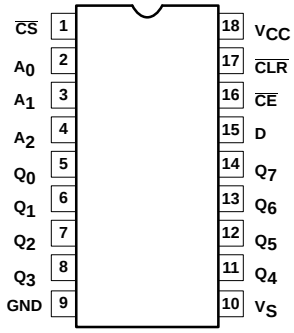
N Package



TOP VIEW

NE590

N Package



TOP VIEW

NE591

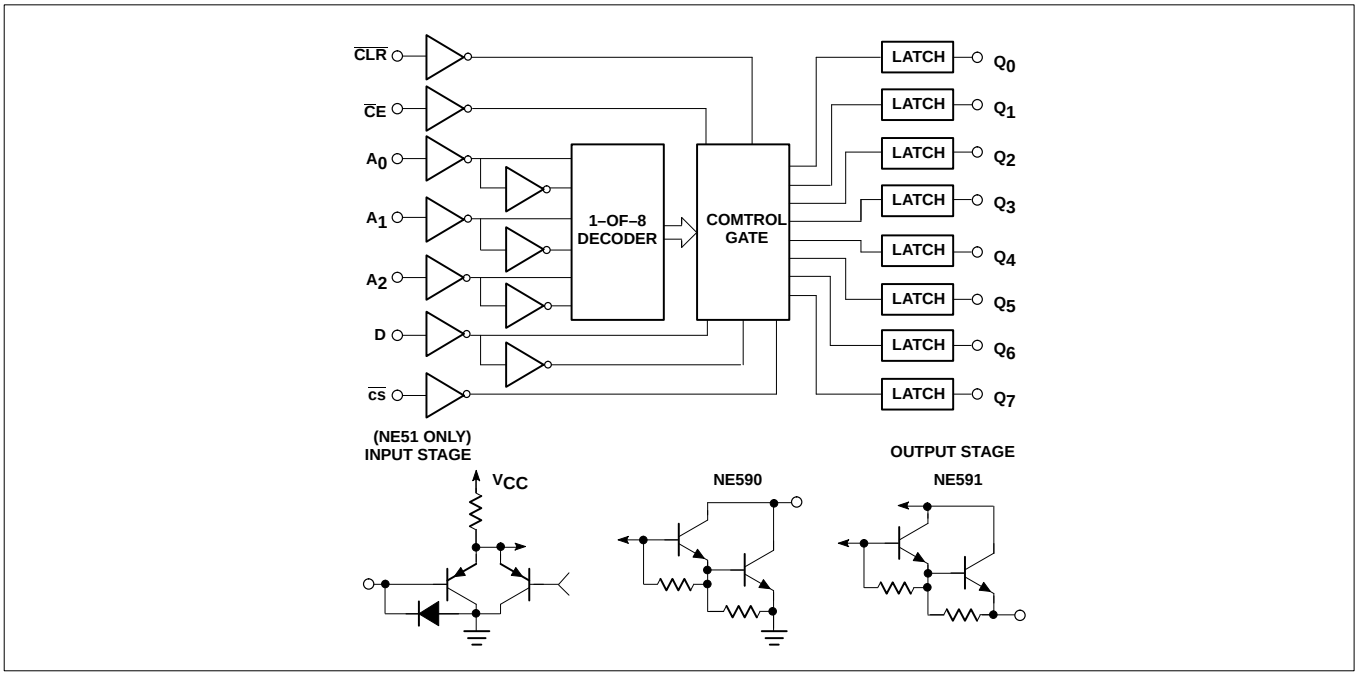
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE590N	0406C
18-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE591N	0406C

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open-collector Darlington outputs. The NE591 has open emitter-follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
-	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
-	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

BLOCK DIAGRAM



TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CL}$ $\overline{R}$	$\overline{C}$ $\overline{E}$	D	A 0	A 1	A_2	Q 0	Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						Addressable Latch
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"OFF" output state
H=High voltage level/"ON" output state

TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
$\overline{CL}$ $\overline{R}$	$\overline{C}$ $\overline{E}$	$\overline{C}$ $\overline{S}$	D	A 0	A 1	A_2	Q 0	Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1} →								
H	H	L	X	X	X	X	Q_{N-1} →								Memory
H	L	H	X	X	X	X	Q_{N-1} →								
H	L	L	L	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	L	H	Q_{N-1} →							
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						Addressable Latch
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	L	H	H	H	Q_{N-1} →							L	
H	L	L	H	H	H	H	Q_{N-1} →							H	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"OFF" output state
H=High voltage level/"ON" output state

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage		V
	NE590	0 to +7	
	NE591	0 to V_{CC}	
V_S	Source bus voltage NE591 only	-0.5 to +7	V
V_S-V_{CC}	Source/supply differential voltage NE591 only	-5 to +2	V
I_{OUT}	Output current		
	Each output	300	mA
	All outputs	1000	
P_D	Maximum power dissipation T_A=25°C (still air)		
	NE590[1] N package	1450	mW
	NE591[2] N package	1690	
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	165	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	300	°C

NOTES:
1. Derate above 25°C at the following rates: N package at 11.6mW/°C
2. Derate above 25°C at the following rates: N package at 13.5mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=4.75 to 5.25V, 0°C ≥ T_A ≤ 70°C unless otherwise specified. [1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	
	Output voltage					
V_{OL}	Low (NE590 only)	I_{OL}=250mA, T_A=25°C		1.0	1.3	
		Over temperature			1.5	V
V_{OH}	High (NE591 only)	I_{OH}=-250mA, V_{CC}=V_S=5V	2.9			
	Input current					
I_{IH}	High	V_{IN}=V_{CC}		0.1	10	
I_{IL}	Low	V_{IN}=0V				
	$\overline{CE}$ input			-25	-60	µA
	All other inputs			-15	-50	
I_{OH}	Leakage current	V_{OUT}=5.25V		10	250	µA
	Supply current[3]	V_S=V_{CC}=5V				
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					mA
	NE590			15	50	
	NE591			30	50	
P_D	Power dissipation	No output load			350	mW

NOTES:
1. All typical values are at V_{CC}=5V and T_A=25°C
2. For the NE591 V_S=V_{CC} in all tests.
3. Supply current for the NE591 is measured with no output load.

SWITCHING CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TO	FROM	NE590			NE591			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Propagation delay time									
t_{PLH}	Low-to-High[1]	Output	$\overline{CE}$		65	150		50	80	ns
t_{PHL}	High-to-Low[1]				115	230		70	120	
t_{PLH}	Low-to-High[2]	Output	Data		65	130		45	70	ns
t_{PHL}	High-to-Low[2]				120	240		65	100	
t_{PLH}	Low-to-High[3]	Output	Address		100	200		45	80	ns
t_{PHL}	High-to-Low[3]				130	260		75	140	
t_{PLH}	Low-to-High[4]	Output	$\overline{CLR}$		65	130				ns
t_{PHL}	High-to-Low[4]							45	140	
t_{PLH}	Low-to-High[1]	Output	$\overline{CS}$					40	80	ns
t_{PHL}	High-to-Low[1]							70	120	
Switching setup requirements										
$t_{S(H)}$		Chip enable	High data	210			100			ns
$t_{S(L)}$		Chip enable	Low data	210			100			ns
$t_{S(A)}$		Chip enable	Address	30			30			ns
$t_{H(H)}$		Chip enable	High data	40			10			ns
$t_{H(L)}$		Chip enable	Low data	30			10			ns
$t_{S(CS)}$		Chip enable	Low chip select				100			ns
$t_{PW(E)}$	Chip enable pulse width[1]			120			120			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

FUNCTIONAL DESCRIPTION

These peripheral drivers have latched outputs which hold the input data until cleared. The NE590 has active-Low, open-collector outputs, while the NE591 has active-High, uncommitted (open) emitter outputs. All outputs are cleared when power is first applied.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the “D” input High to turn on the selected input, or by holding it Low to turn off, holding the $\overline{CLR}$ input High, and bringing the $\overline{CE}$ input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the $\overline{CLR}$, $\overline{CE}$, and “D” inputs Low. For NE591, $\overline{CS}$ must be brought Low any time CE is Low if any outputs are to be changed.

Demultiplexer Operation

By bringing the $\overline{CLR}$ and $\overline{CE}$ inputs Low and the “D” input High, the addressed output will remain on and all other outputs will be off. This condition will remain only as long as the output is addressed. For the NE591, the $\overline{CS}$ input must also be Low.

High Current Outputs

The obvious advantage of these devices over the 9334 and N74LS259 (which provide a similar function) is the fact that the NE590 and NE591 are capable of output currents of 250mA at each of their eight outputs. It should be noted, however, that the load power dissipation would be over 2.5W if all 8 outputs were to carry their full rated load current at one time. Since the total power dissipation is limited by the package to 1W, and since the power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$t_R = \theta_{JA} \times P$$
$$t_J = t_A + t_R$$

where

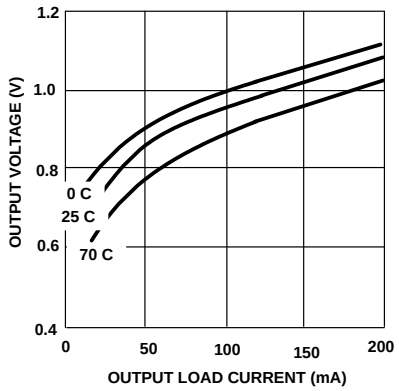
θ_{JA} is die junction to ambient thermal resistance.
P_D is total power dissipation
t_R is junction temperature rise above ambient
t_j is die junction temperature
t_A is ambient (surrounding medium) temperature

For example, if we are using the NE590 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 250mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

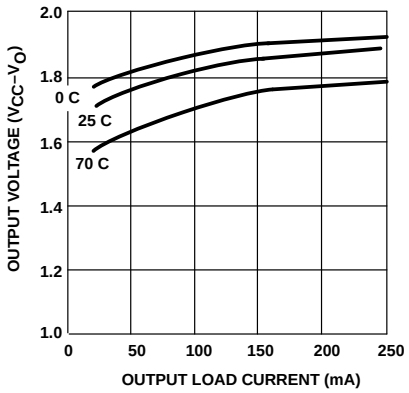
Plastic t_R=83×0.7235=60°C
Plastic t_J=50+60=100°C
Cerdip t_R=100×0.7235=72.40°C
Cerdip t_J=50+72.4=122.4°C

Thus we find that t_J for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

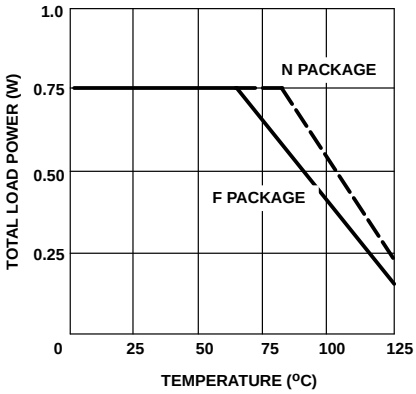
TYPICAL PERFORMANCE CHARACTERISTICS



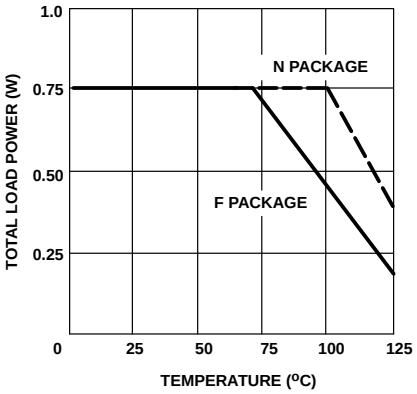
Output Voltage vs Load Current (NE590)



Output Voltage Drop vs Load Current (NE591)

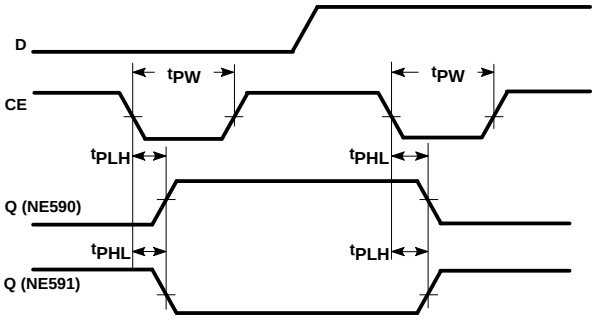


Total Load Power vs Temperature (NE590)



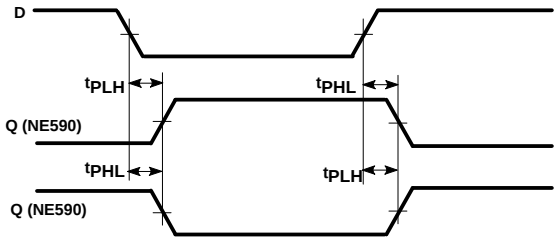
Total Load Power vs Temperature (NE591)

TIMING DIAGRAMS



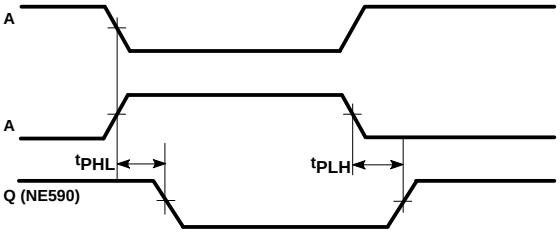
NOTE:
Other inputs $\overline{CLR}$ = H, $\overline{CS}$ = L, A = Stable

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width



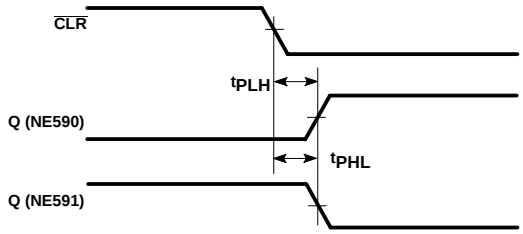
NOTE:
Other inputs $\overline{CE}$ $\overline{CS}$ = L, $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Data-to-Output



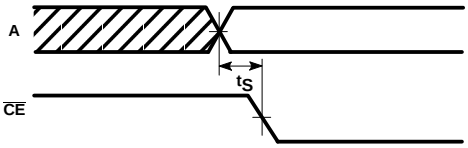
NOTE:
Other inputs $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

Turn-On and Turn-Off Delays, Address-to-Output



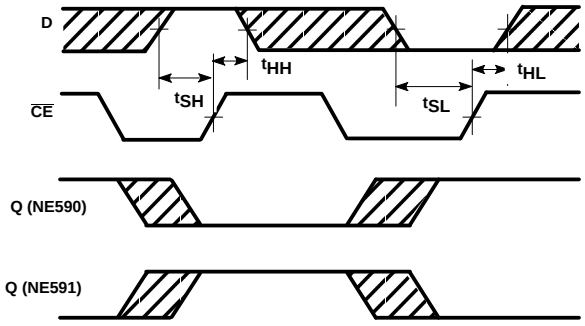
NOTE:
Other inputs $\overline{CS}$ = H, $\overline{CE}$ = H

Turn-On and Turn-Off Delays, Clear-to-Output



NOTE:
Other inputs $\overline{CLR}$ = H, CS = L

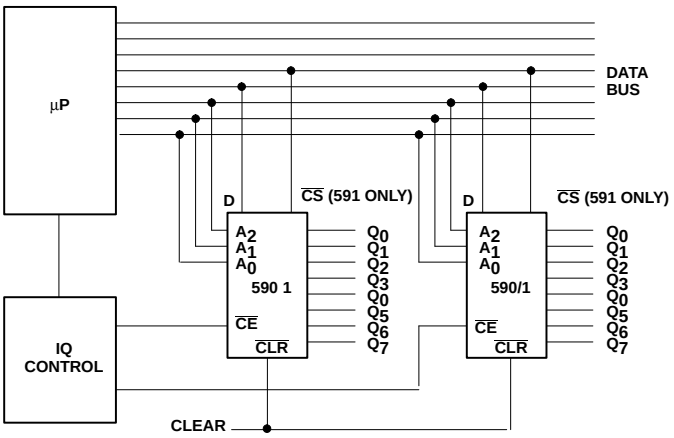
Set-Up Time, Address-to-Enable



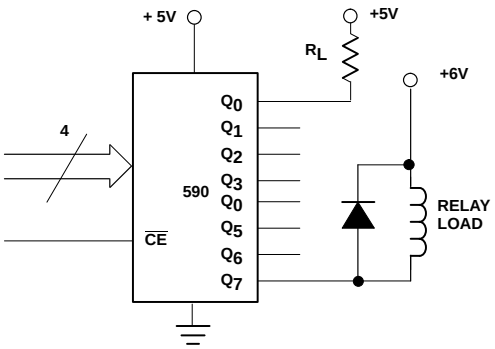
NOTE:
Other inputs $\overline{CLR}$ = H, $\overline{CS}$ = L, A = Stable

Set-Up and Hold Time, Data-to-Enable

TYPICAL APPLICATIONS

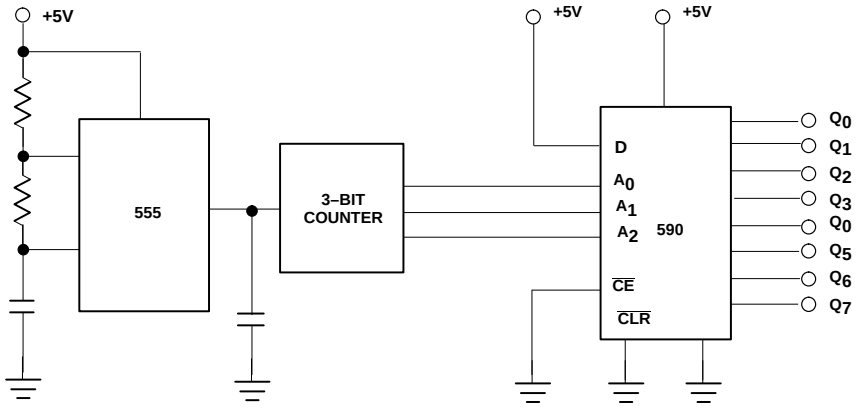


Turn-On and Turn-Off Delays, Address-to-Output



NE590 Driving Simple Loads

NOTE:
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.



NE590 Operating in Demultiplex Mode