Audio processor - filter and control section   NE/SA5751

DESCRIPTION

The NE/SA5751 is a high performance low power CMOS audio signal processing system. The NE/SA5751 subsystems include complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, a digitally controlled volume control with 30dB range (in 2dB steps), audio path mute switches, a programmable DTMF generator, power- down circuitry for low current standby, power-on reset capability, and an I^2C interface. When the SA5751 is used with an SA5750 (companding function), the complete audio processing system of an AMPs or TACs cellular telephone is easily implemented.

FEATURES

- Low power
- High performance
- 5V supply
- Built-in programmable DTMF generator
- Built-in digitally controlled volume control
- Built-in peak-deviation limit
- I^2C Bus controlled
- Power-on reset
- Power-down capability

BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5750

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

NOTE:
Figure 1. Pin Configurations
1. Available in SOL (large surface mount) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5751N	SOT248-1
28-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE5751D	SOT136-1
24-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5751N	SOT248-1
28-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5751D	SOT136-1

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PIN DESCRIPTIONS

PIN NO.		SYMBOL	DESCRIPTION
	(1)	NC	Not connected
1	(2)	NC	Not connected
2	(3)	V_{REF}	Reference voltage
3	(4)	$TXBF_{IN}$	Transmit bandpass filter input
4	(5)	$TXBF_{OUT}$	Transmit bandpass filter output
5	(6)	$PREMP_{IN}$	Pre-emphasis input
6	(7)	V_{DD}	Positive supply
7	(8)	$DEMP_{OUT}$	De-emphasis output
8	(9)	VC_{IN}	Volume control input
9	(10)	VC_{OUT1}	Volume control output 1
10	(11)	VC_{OUT2}	Volume control output 2
11	(12)	MUTET	TX analog voice path mute input
12	(13)	MUTER	RX analog voice path mute input
	(14)	NC	Not connected
	(15)	NC	Not connected
13	(16)	VOX_{CTL}	Vox control output
14	(17)	$RXBF_{IN}$	Receive bandpass filter input
15	(18)	SA1	Serial bus address
16	(19)	SCL	Serial clock line
17	(20)	SDA	Serial data line
18	(21)	CLK_{IN}	Clock input
19	(22)	GND	Ground
20	(23)	TXS_{OUT}	Transmit summer output
21	(24)	TXS_{IN}	Transmit summer input
22	(25)	$TXDTMF_{OUT}$	Transmit DTMF output
23	(26)	$TXLF_{OUT}$	Transmit low-pass filter output
24	(27)	NC	Not connected
	(28)	NC	Not connected

NOTE:
1. Callouts are for N package; those in parentheses are for the D (SOL) package.

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BLOCK DIAGRAM
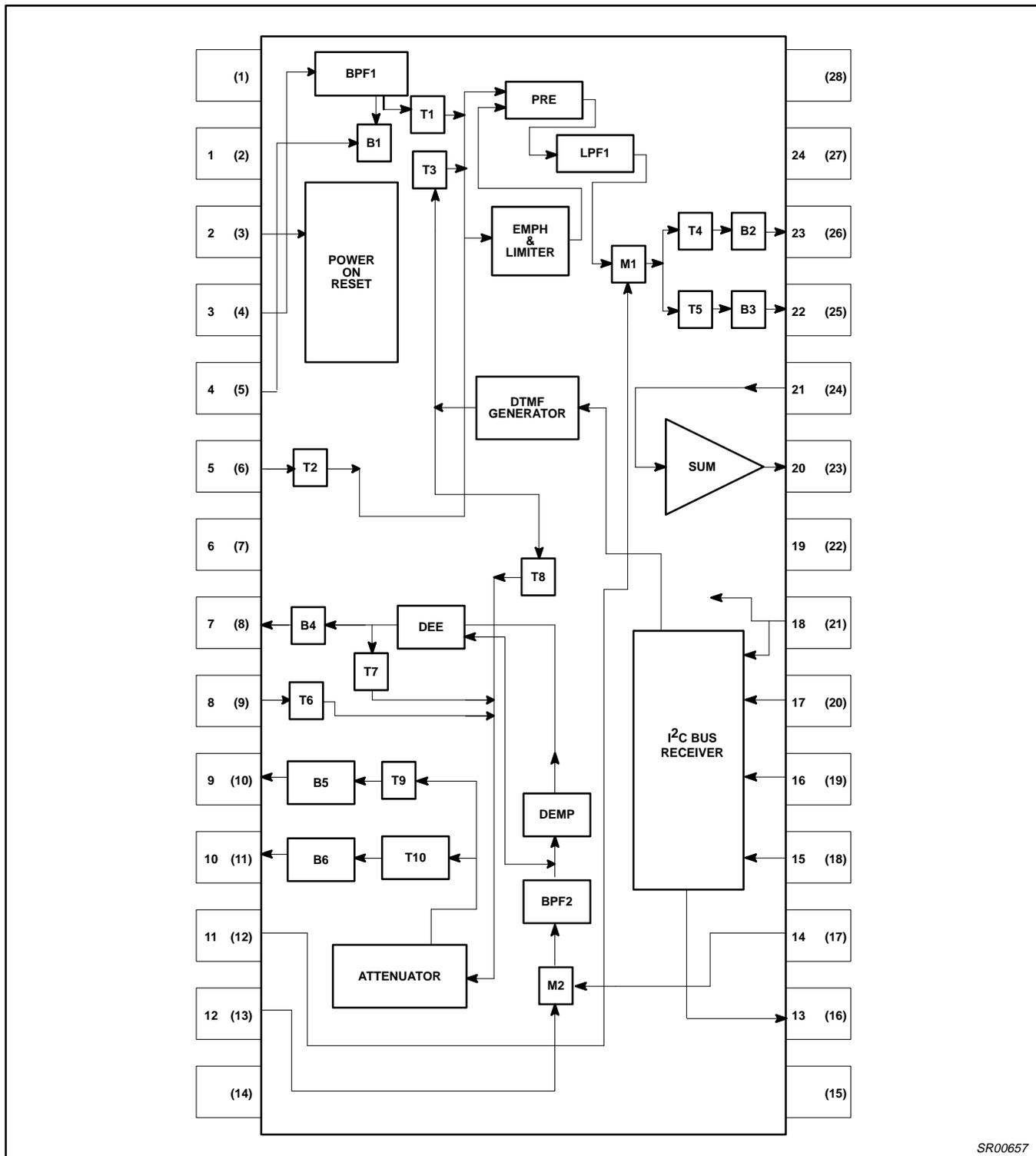
Figure 2. Block Diagram

NOTES:
1. T1 to T10 represent the signal path switches.
2. M1 and M2 represent the mute switches.
3. PRE and DEE represent the bypass switches for pre-emphasis and de-emphasis, respectively.
4. B1 to B6 represent the output buffers.

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[1]	6	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5751	0 to 70	°C
	SA5751	-40 to +85	°C

NOTE:
1. Voltage applied to any pin -0.3 to V_{DD} +0.3V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V, unless otherwise specified. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage range		4.75	5.0	5.25	V
I_{DD}	Supply current	Operating Standby		2.7 0.9	5.0 2.0	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V. See test circuit, Figure 6. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		500		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-0.5	0	0.5	dB
	RX BPF gain with de-emphasis	f = 100Hz		-31	-29	dBm0
	RX BPF gain with de-emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.0	-10.0	-9.0	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-68	-50	dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		170		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	DEMP$_{OUT}$ output impedance	f = 1kHz		40		Ω
	DEMP$_{OUT}$ output swing (1%)	2.3kΩ to V_{REF}; f = 1kHz	V_{DD} -3	3.5		V_{P-P}
	VC$_{OUT1}$ ouput swing (1%)	50kΩ toV_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC$_{OUT2}$ output swing (1%)	50kΩ to V_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC$_{OUT1}$ noise	VC$_{IN}$ grounded C - message		25		μV_{RMS}
	VC$_{OUT2}$ noise	VC$_{IN}$ grounded C - message		25		μV_{RMS}
	Mute threshold off		0		0.8	V
	Mute threshold on		2.0		5.0	V
	CLK1, 2 high		4.0		5.0	V
	CLK1, 2 low		0		1.0	V
	TX BPF anti alias rejection			40		dB
	TX BPF input impedance	f = 3kHz		500		KΩ

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AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX BPF noise	300 - 3000kHz		90		μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dB
	TX LPF gain with pre-emphasis	f = 1kHz, 20dBV		12.06		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-39		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-51		dBm0
	TX overall gain	1kHz	11.3	11.8	12.5	dB
	TX overall gain	100Hz		-47	-45	dBm0
	TX overall gain	300Hz	-11	-10.4	-9	dBm0
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF output impedance	f = 1kHz		360		Ω
	TX BPF output swing (1%THD)	50kΩ to V_{REF} f = 1kHz		4.5		V_{P-P}
	TX BPF dynamic range			90		dB
	PREMP$_{IN}$ input impedance	f = 3kHz		500		kΩ
	Summing op amp					
	Slew rate	C_L = 15pF		0.75		V/μs
	Output impedance	Unity gain; f = 3kHz		40		Ω
	Output swing (1% THD)	1kHz, 5kΩ load (25°C)		4.3		V_{P-P}
	Volume control accuracy	-30dB to 0dB	-1	0	+1	dB
	Analog switches					
	Insertion loss			60		dB
	On time transition	MUTET, MUTER 0.8V ->2.0V		3		μs
	Off time transition	MUTET, MUTER 2.0V ->0.8V		0.25		μs

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are high. Data transfer may be initiated only when the bus is not busy.

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

Due to the variety of different devices which can be connected to the I²C bus, the levels of the logical "0" and "1" are not fixed and depend on the appropriate level of V_{DD}. For the typical supply voltage of 5V which is chosen here, logical "1" and logical "0" are, however, fixed respectively on maximum input LOW voltage, 1.5V and minimum input HIGH voltage, 3.0V.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock's cycle. If it does not remain HIGH, it may be interrupted as a control signal.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition S. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

SYSTEM CONFIGURATIONS
A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master"; and devices which are controlled by the master are the "slaves".

ACKNOWLEDGE
The number of data bytes transferred between the start and the stop condition from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must be taken into account.

I^{2}C BUS DATA CONFIGURATIONS
The NE5751 is always a slave receiver in the I^{2}C bus configuration (R/W bit-0). The slave address consists of seven bits in the serial mode where the least significant bit is selectable by hardware on input A0 and the other more significant bits are internally fixed.

POWER ON RESET
In order to avoid undefined states of the NE5751 when the power is switched on, a power on reset is supplied. The reset is active when Pin V_{REF} is held below 0.8V. The reset is off when Pin V_{REF} is above 2.0V. Pin V_{REF} is normally at 2.5V generated by a resistive divider from V_{DD}. Nominal impedance is 20kΩ. In a typical application a capacitor is connected to Pin V_{REF} to improve power supply rejection. The time delay of the network resets the internal registers when power is first applied. The signal paths are off in the reset condition. The NE5751 must be programmed via the I^{2}C bus for normal operation. The Power Down mode is defined only when all register values are zero.

CONTROL REGISTERS

Register Map
The address register is as follows:

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	SA1	0

SA1 is controlled by serial bus address pin.

Signal Path Register

MSB							LSB
T10	T9	T8	T6	VOX$_{EN}$	T4	T3T5	T2

T2   is the transmission gate between Pin PREEMP$_{IN}$ and the emphasis input.

T3T5   connects the output of the DTMF generator to the emphasis input and connects the output of the XMT LPF to Pin TXDTMF$_{OUT}$.

T4   connects the output of the XMT LPF to Pin TXLF$_{OUT}$.

VOX$_{EN}$ enables the VOX function of NE5750.

T6   connects Pin VC$_{IN}$ to the volume control.

T8   connects the output of the DTMF generator to the volume control.

T9   enables VC$_{OUT1}$.

T10   enables VC$_{OUT2}$.

Volume Control and Test Register

MSB							LSB
PDW	T1T7	DEE	PRE	V1	V2	V3	V4

V4   is volume control bit 4. This is the MSB. A zero is 16dB attenuation.

V3   is volume control bit 3. A zero is 8dB attenuation.

V2   is volume control bit 2. A zero is 4dB attenuation.

V1   is volume control bit 1. A zero is 2dB attenuation.

PRE   is the bypass for the pre-emphasis.

DEE   is the bypass for the de-emphasis.

T1T7   is the bypass for the compressor and expandor.

PDW   is the control for power down mode.

This mode is defined only when all register values are reset to zero.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

$$\text{High Frequency} = 1200\text{kHz}/6/\text{HD}$$
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

$$\text{Low Frequency} = 1200\text{kHz}/12/\text{LD}$$
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading the two DTMF registers before 96ms have elapsed.

Single tones can be obtained by loading 0, 1 or 2 into one of the registers to silence it.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during operation.

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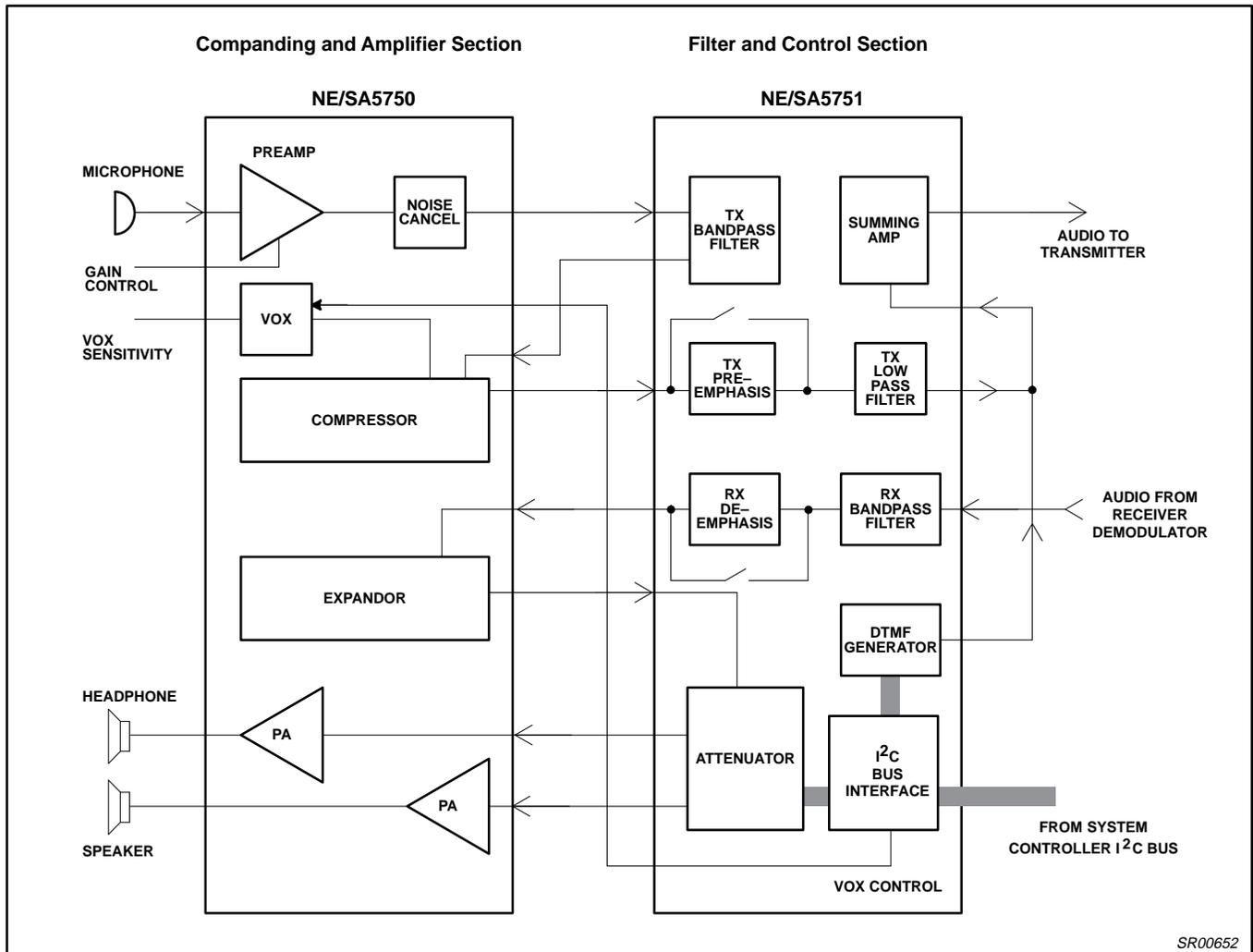
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Figure 3. Typical Configuration of Audio Processor (APROC) System Chip Set

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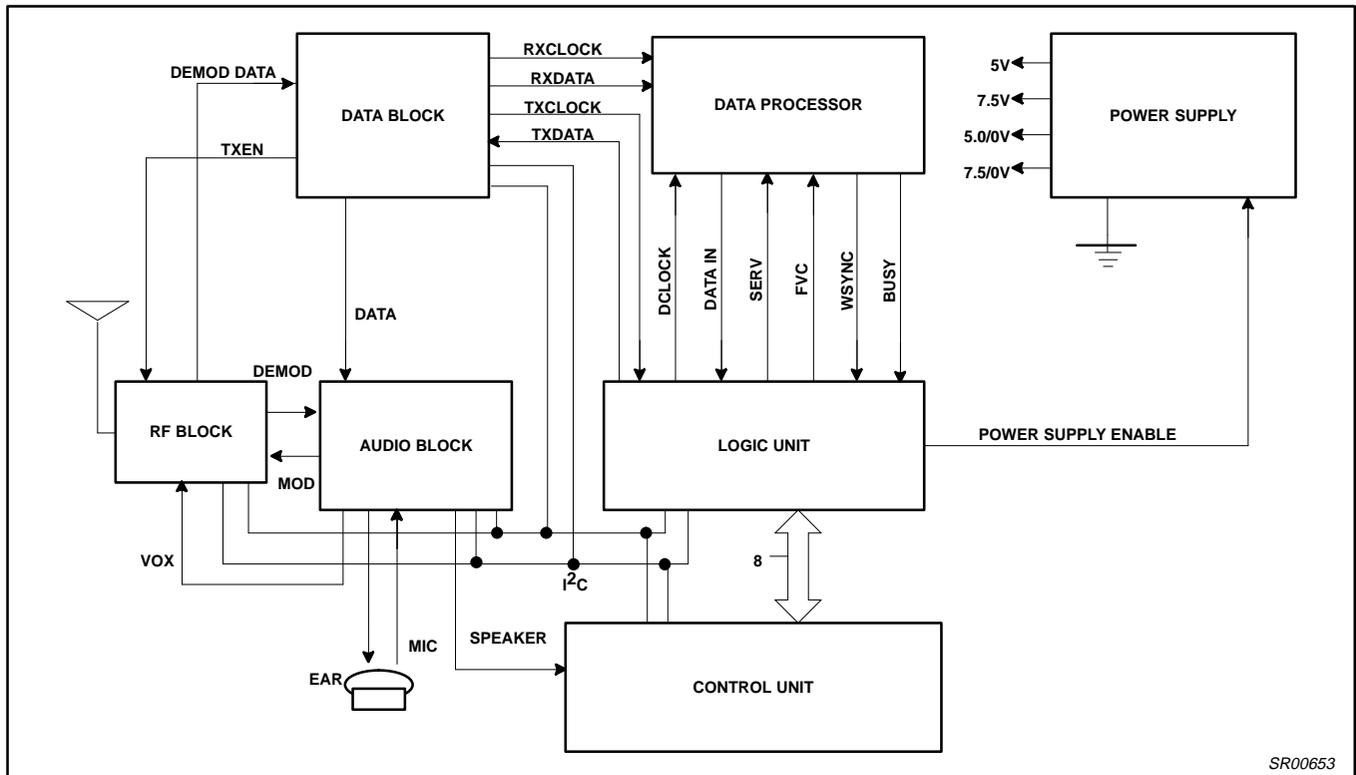
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Figure 4. Cellular Radio System
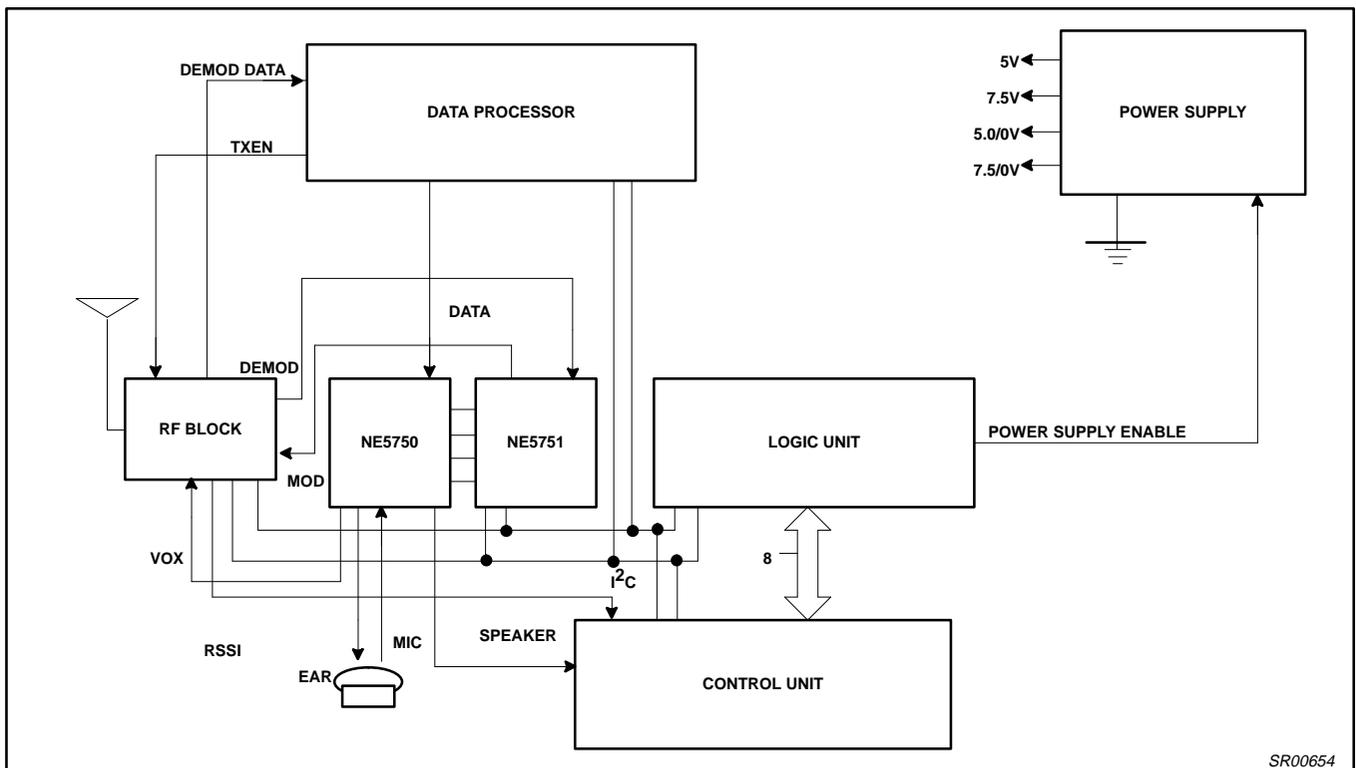
Figure 5. APROC Application Diagram
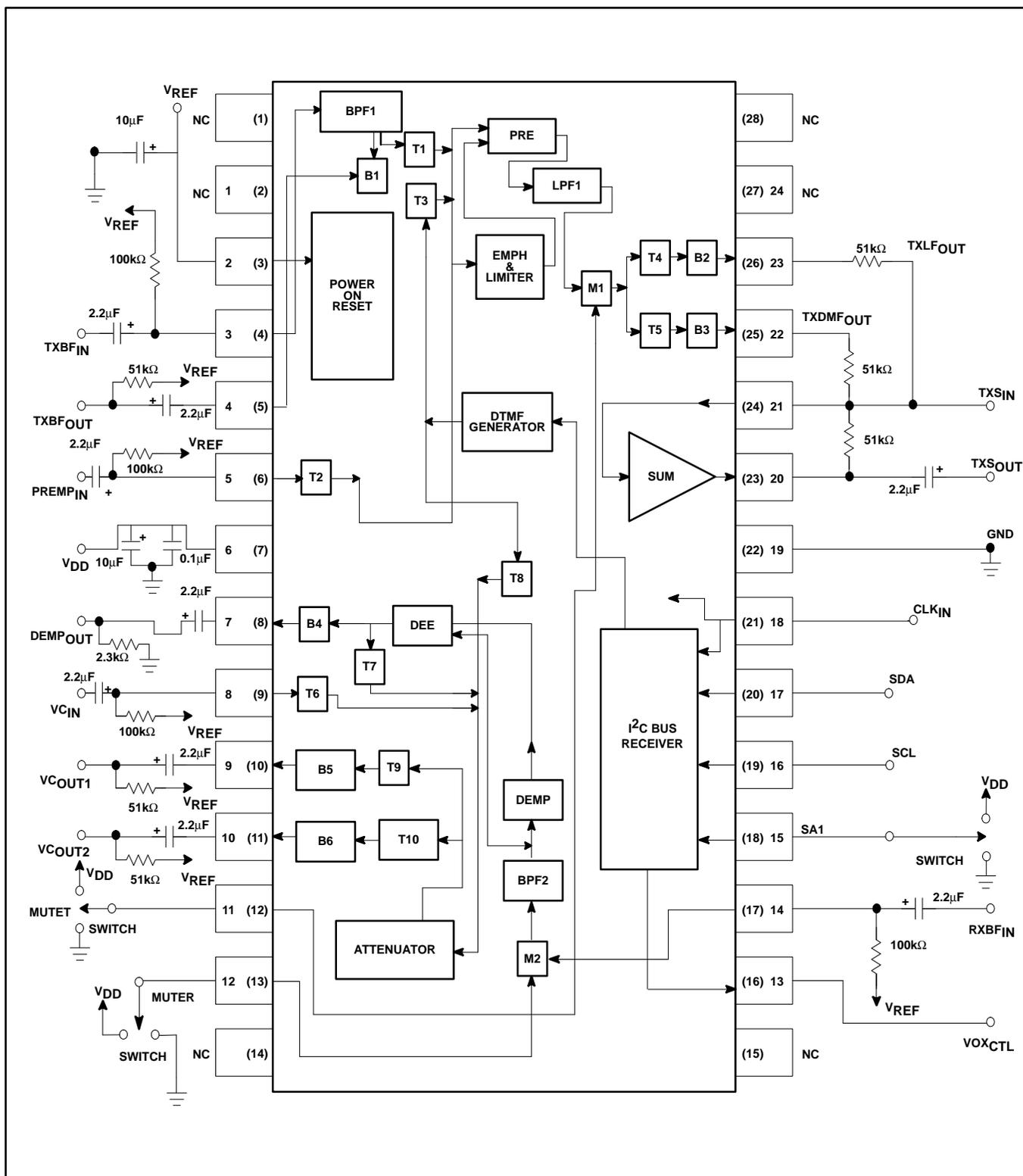
Figure 6. NE/SA5751 Test and Application Circuit

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PERFORMANCE CHARACTERISTIC
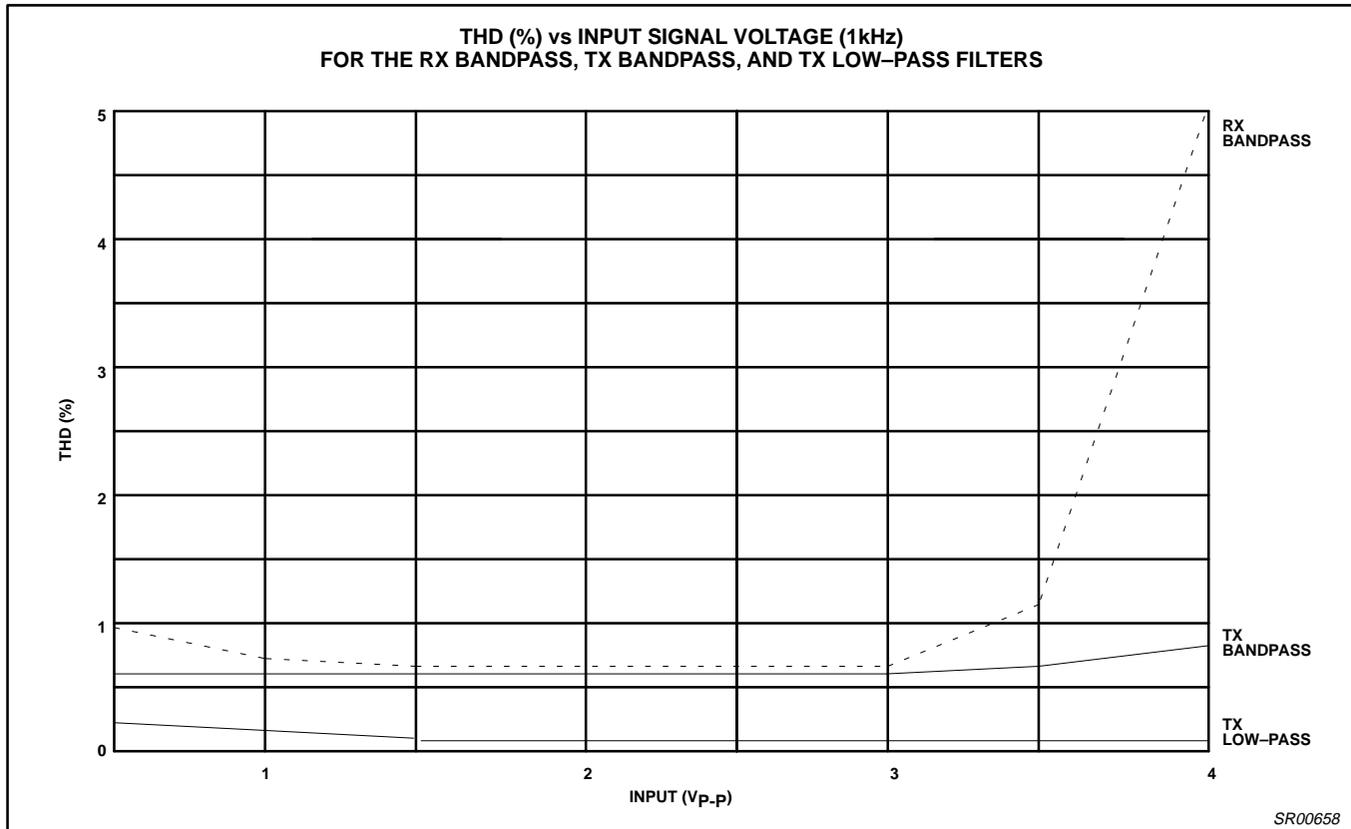
Figure 7. Performance Characteristics