APPLICATION NOTE

A Wideband hybrid coupled amplifier (470 – 860 MHz) with 2 balanced transistors BLV57

NCO8101

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CONTENTS

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1 ABSTRACT

For application in TV transposers in band 4 and 5 (470 – 860 MHz) a wideband linear power amplifier has been designed with two balanced transistors BLV57 coupled by means of 3 dB –90° hybrids. The class-A DC-setting of the transistors is $I_C = 2 \times 850$ mA and $V_{CE} = 25$ V. The main properties of the two prototypes are:

Table 1

470 – 860 MHz	UNIT	AMPLIFIER 2	AMPLIFIER 3
Gain (P_i = 1 mW)	dB	9.3 ±0.5	9 ±0.5
Return losses input	dB	≥17	≥16
Return losses output	dB	≥19	≥19
P_o at 1 dB gain compression	W	≥28	≥28
P_o at –55 dB intermod. (3-tone, –7, –8 and –16 dB)	W	≥17.5	≥17.5
Cross modulation at P_o = 15 W	%	≤9.4	≤8.8

2 INTRODUCTION

For application in TV transposers for band 4 and 5 (470 – 860 MHz) a wideband linear power amplifier has been designed with two transistors BLV57 in class-A. The BLV57 is a balanced transistor (two identical chips) in a single envelope with a ceramic cap (SOT-161).

3 DESIGN OF THE AMPLIFIER

3.1 General remarks

The schematic line-up of the complete amplifier is given in Fig.1.

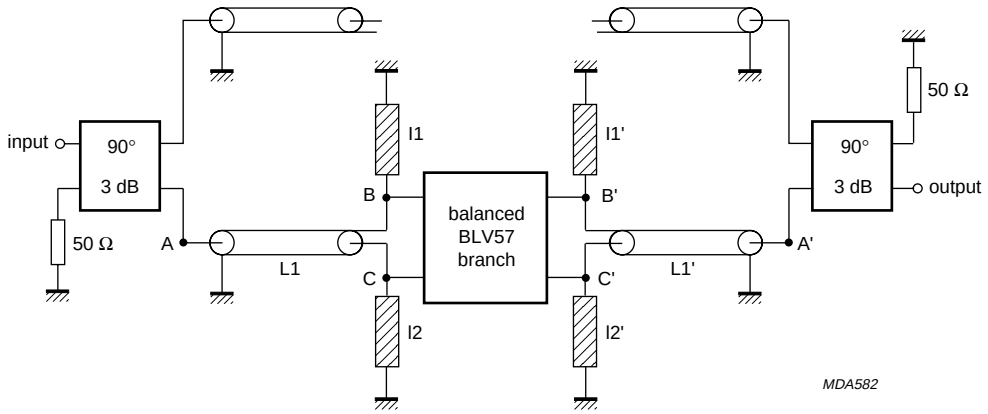

Fig.1 Schematic line-up of the complete amplifier.

The amplifier consists of 2 balanced circuits, both equipped with a BLV57 and coupled in parallel by means of a wideband 3 dB –90° coaxial hybrid at the input and output. Each BLV57 has 2 input circuits (one for each chip) connected to a coax balun (L1 and L1') which splits a 50 Ω unbalanced port (A) in two 25 Ω ports (B and C). The phase-shift between B and C is 180°. The baluns (L1 and L1') are 50 Ω semi-rigid coax cables, soldered over the whole length atop a transmission line (l_1 or l_1') of 2 mm width. To maintain circuit symmetry another shorted stub (l_2 or l_2') with the same length has been added. For the amplifier a printed-circuit board has been applied of PTFE fibreglass with an ε_r = 2.74, copper clad on both sides with a thickness of $^1/_{32}$ inch. To get a good contact between upper and lower side, rivets have been used at several places and copper straps have been soldered at the edges of the board.

3.2 Bias circuit

Each transistor has its own bias unit to obtain a stable DC-setting (see Fig.4). This bias unit enables the adjustment of the base current of each chip of the BLV57 by means of potentiometer R_8, to obtain equal collector currents. The potentiometer R_1 adjusts both base currents simultaneous. After an accurate measurement of the values of resistors R_{12} and R_{13} the collector currents of the BLV57, and the difference between them, can be determined easily by measuring the voltage-drop over these resistors. The supply voltage of this bias unit is 28 V. Figure 5 shows the positive copy of the printed-circuit board and the lay-out of the bias unit.

3.3 Some properties of the BLV57

For class-A operation the BLV57 is specified at $I_C = 2 \times 850$ mA and V_{CE} = 25 V. The typical gain, input and load impedance of a half BLV57 (one chip) are given in Table 2.

Table 2

FREQUENCY (MHz)	GAIN (dB)	INPUT IMPEDANCE (Ω)	LOAD IMPEDANCE (Ω)
470	13.13	1.11 + j 2.62	9.75 + j 6.52
507	12.57	1.13 + j 2.88	9.00 + j 6.29
547	12.02	1.14 + j 3.17	8.26 + j 5.99
590	11.49	1.16 + j 3.47	7.52 + j 5.60
636	10.98	1.18 + j 3.80	6.80 + j 5.14
686	10.49	1.21 + j 4.16	6.10 + j 4.60
739	10.03	1.25 + j 4.55	5.44 + j 3.99
797	9.60	1.30 + j 5.00	4.80 + j 3.29
860	9.20	1.37 + j 5.50	4.20 + j 2.52

3.4 Output network

The 25 Ω of the balun has to be transformed into the optimum load for the half transistor (one chip), which is given in Table 2. This is done by means of an L – C output network. The circuit has been calculated according to Ref. 1 and submitted to a computer optimization program. Because the BLV57 is a balanced transistor with two identical chips, there are two identical output circuits with a virtual ground between them. Figure 2 shows the calculated output circuit connected to the balun, described in Section 3.1. Two capacitors of 2.2 pF and a resistor of 12 Ω prevent oscillation at higher frequencies.

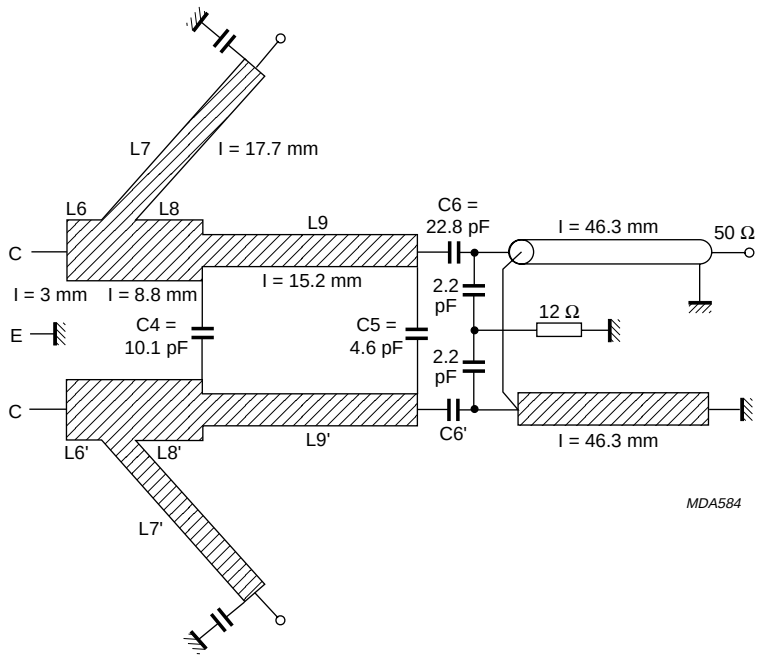

Fig.2 Calculated output circuit.

The stripline L_6 (width 3 mm) is the soldering place for the collector lead. The transistor is biased through the stripline L_7 (width 2 mm). This stripline has been connected to L_6 and L_8 at a distance of 3 mm from the transistor. L_8 is a stripline with a width of 3 mm and L_9 with a width of 1.5 mm. C_4 consists of a chip capacitor in parallel with a film dielectric trimmer. C_5 is a film dielectric trimmer and C_6 is a chip capacitor.

3.5 Input network

In the frequency range of 470 – 860 MHz the gain of a half BLV57 (one chip) varies about 4 dB (see Table 2). To decrease this gain slope an appropriate mismatch at the lower frequencies is necessary. The increasing insertion losses of the network approximately compensate the increasing gain at the lower frequencies. This method is described in Ref. 2. For the same reason as described in Section 3.4 there are two identical input circuits with a virtual ground between them. Figure 3 shows the calculated input circuit after computer optimization connected to the coaxial balun, described in Section 3.1.

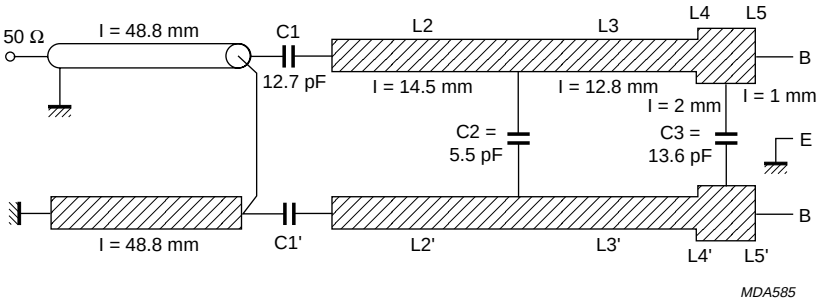

Fig.3

The striplines L_4 and L_5 (width 3 mm) form together the soldering place of the base lead. The width of the striplines L_2 and L_3 is 1.5 mm. The capacitors C_1, C_2, and C_3 are chip capacitors. The circuit of a complete branch (see Fig.1) is given in Fig.6.

4 ADJUSTMENT OF THE AMPLIFIER

4.1 Output circuit

To obtain the highest possible output power it is essential that the transistor is given that load admittance which gives the least distortion in the used frequency range. Therefore, for tuning, the transistor has to be replaced by a dummy consisting of a resistor and a capacitor in parallel to represent the complex conjugate of the optimum load admittance. The value of this dummy (soldered between the connection points of both collectors) has been calculated on

39 Ω//8.2 pF. With the help of this dummy the output circuit has to be adjusted for good return losses at the output of L_{10} by tuning the capacitors C_{10} and C_{17} and by shifting the capacitors C_{13} and C_{14} on L_7 and L_{17} (see Fig.6). The position of the capacitors C_{13} and C_{14} on the striplines determines the value of L_7 and L_{17}. A typical curve of the return losses at the output of L_{10} after tuning is given in Fig.7.

4.2 Input circuit

Before tuning the input circuit, the dummy has to be replaced by the transistor, with a DC-adjustment of $I_C = 2 \times 850$ mA and $V_{CE} = 25$ V. To decrease the gain-slope of the branch the input circuit has a mismatch at lower frequencies (see Section 3.5). To achieve a sufficient flat gain the capacitance of C_1, C_2, C_3, and C_4 and also the position of C_3 and C_4 (see Fig.6) can be optimized in a sweep set-up under small signal conditions (P_i = 1 mW). A typical gain curve of a balanced branch (one BLV57) and the corresponding return losses are given in Figs 9 to 11. It is obvious that the worse return losses at the lower frequencies are produced by the mismatch of the input circuit.

5 THE HYBRID COUPLED AMPLIFIER

In the previous section the adjustment of a balanced branch with one BLV57 has been discussed. The gain is made flat at the cost of impermissibly high return losses. Therefore, in practice, two wideband branches are coupled in parallel by means of two wideband 3 dB –90° coaxial hybrids. The properties of these hybrids reduce the return losses to at least 16 dB. The reflected power of the balanced branches is absorbed by a 50 Ω resistance at the isolated port (see Fig.1). Figure 12 gives a positive copy of the printed-circuit board of the complete amplifier. It also shows the lay-out of this complete amplifier.

6 MEASURED PERFORMANCE

6.1 Small signal gain and return losses

Figures 13 to 15 show the gain and return losses as a function of the frequency, measured under small signal conditions. Results:

Table 3

470 – 860 MHz	UNIT	AMPLIFIER 2		AMPLIFIER 3	
		MIN.	MAX.	MIN.	MAX.
Gain	dB	8.8	9.8	8.5	9.5
Return losses input	dB	17	30.5	16	30
Return losses output	dB	17	39	18	40

6.2 Gain compression

Figures 16 and 17 show the measured P_o versus P_i curves at 600 MHz, which is the most critical frequency in the range. Gain compression of 1 dB occurs at an output power of about 28 W for both amplifiers.

6.3 Intermodulation

In Fig.18 the output power ($P_{o\ sync}$) is given as a function of the frequency at three intermodulation levels. It has been measured according the 3-tone test method (vision carrier: –8 dB, sound carrier: –7 dB and sideband signal: –16 dB). Zero dB corresponds to the peak sync. level. The minimum output power at –60 dB intermodulation amounts to 12.4 W for amplifier 2 and 12.2 W for amplifier 3.

6.4 Cross modulation

Figure 19 shows the cross modulation as a function of the frequency at two $P_{o\ sync}$ levels. It is a 2-tone measurement (vision carrier: 0 dB and sound carrier: −7 dB). The amplitude of the vision carrier is changed from white level (−20 dB) to peak sync level (0 dB). The observed change of the voltage amplitude of the sound carrier is called cross modulation. It is expressed as a percentage of the amplitude of the sound carrier (vision carrier at white level). It has been measured with a spectrum analyser operating in linear mode. At a $P_{o\ sync}$ level of 15 W the cross modulation of amplifier 2 varies from 3.4 to 9.4% and of the amplifier 3 from 4.1 to 8.8%.

7 CONCLUSIONS

It is possible to build a linear power amplifier with excellent performance with two transistors BLV57. The main properties of the two prototypes are shown in Table 4.

Table 4

BAND 4/5	UNIT	AMPLIFIER 2	AMPLIFIER 3
Gain (P_i = 1 mW)	dB	9.3 ±0.5	9 ±0.5
Return losses input	dB	≥17	≥16
Return losses output	dB	≥19	≥19
P_o at 1 dB gain compression	W	≥28	≥28
$P_{o\ sync}$ at −55 dB intermod. (3-tone, −7, −8 and −16 dB)	W	≥17.5	≥17.5
cross modulation at P_o = 15 W	%	≤9.4	≤8.8

8 REFERENCES

Ref.1
G.L. Matthaei.
Tables of Chebychev impedance transforming networks of low pass filter form.
Proc. of the IEEE, August 1964.

Ref.2
O. Pitzalis Jr. and R.A. Gibson.
Tables of impedance matching networks which approximate prescribed attenuation versus frequency slopes.
IEEE transactions on microwave theory and techniques, vol. MTT 119, no. 4, April 1971.

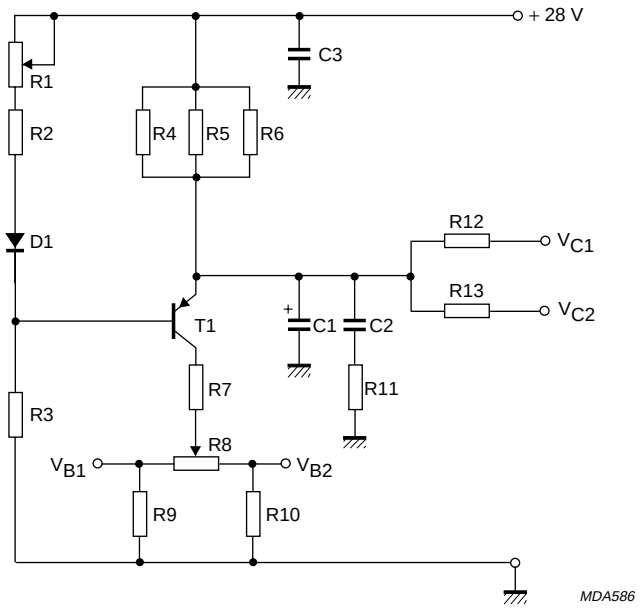

Fig.4 Bias circuit.

Table 5 Parts list of bias circuit (Fig.4)

C_1 = 10µF	63 V electrolytic capacitor	2222 030 28109
C_2 = 470 nF	metallised film capacitor	4322 352 45474
C_3 = 100 nF	metallised film capacitor	2222 352 45104
R_1 = 100 Ω	cermet potentiometer	2122 350 00066
R_2 = 120 Ω	CR 25 type	2322 211 13121
R_3 = 1500 Ω	CR 25 type	2322 211 13152
$R_4 = R_5 = R_6$ = 4.7 Ω	enamelled wire-wound	2322 330 22478
R_7 = 82 Ω	enamelled wire-wound	2322 330 22829
R_8 = 20 Ω	cermet potentiometer	2122 350 00057
$R_9 = R_{10}$ = 39 Ω	CR 25 type	2322 211 13399
R_{11} = 10 Ω	CR 25 type	2322 211 13109
$R_{12} = R_{13}$ = 0.15 Ω	wire-wound PM 10 type	2322 326 51157
D_1 = BY 206		
T_1 = BD 140		

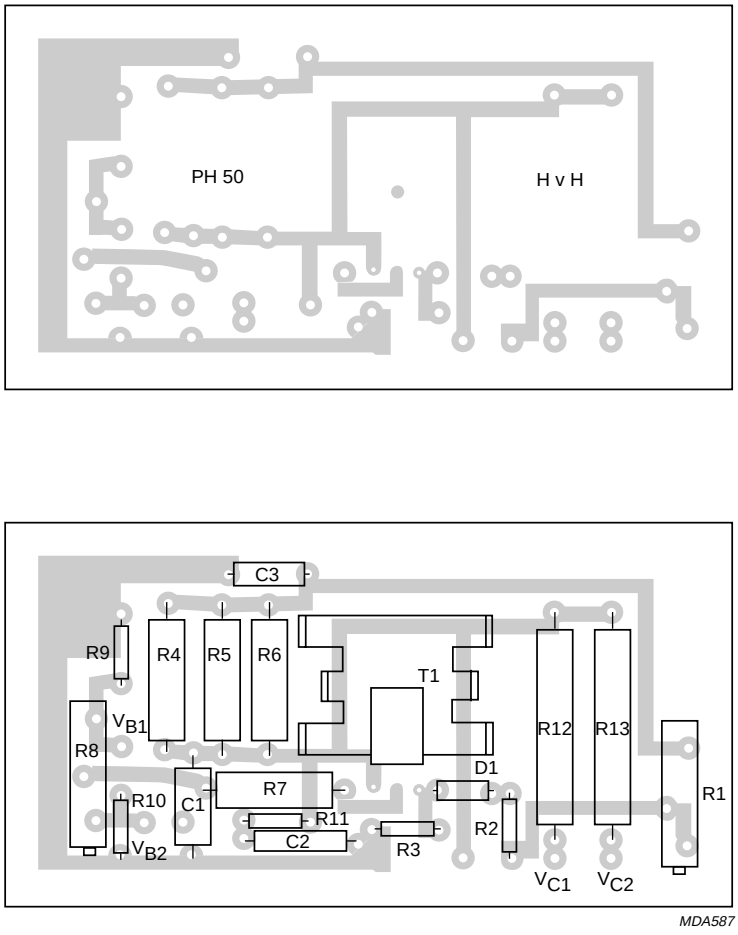

Fig.5 Printed-circuit board lay-out of the bias unit.

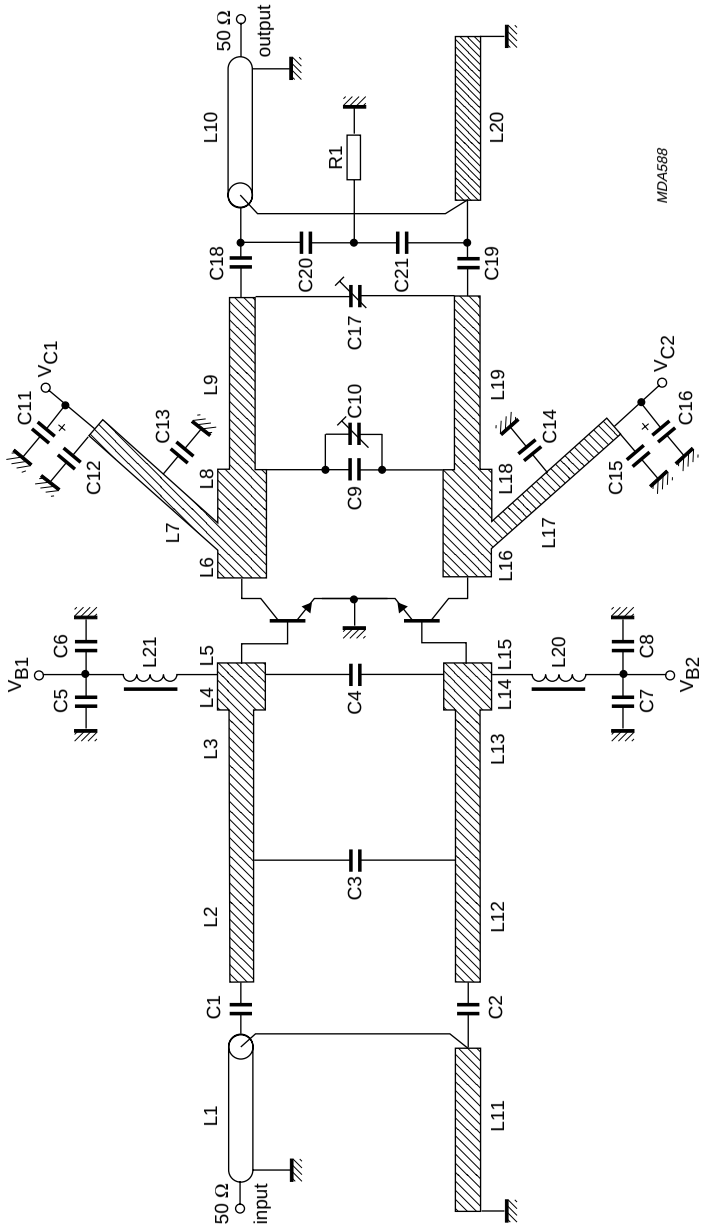

Fig.6 Circuit of a BLV57 branch.

Table 6 List of components BLV57 branch

$C_1 = C_2$ = 10 pF chip capacitor	Philips NPO	2222 851 13109
C_3 = 3.9 pF chip capacitor	Johanson	no. 500 R 15 N 3R9 CA
C_4 = 12 pF chip capacitor	Philips NPO	2222 851 13129
$C_5 = C_7 = C_{12} = C_{15}$ = 100 nF chip capacitor	Philips NPO	2222 855 48104
$C_6 = C_8$ = 100 pF chip capacitor	Philips NPO	2222 852 13101
C_9 = 8.2 pF chip capacitor	ATC	8R2J
$C_{10} = C_{17}$ = 1 – 3.5 pF film dielectric trimmer	Philips	2222 809 05001
$C_{11} = C_{16}$ = 6.8 μF, 40 V, electrolytic capacitor	Philips	2222 030 37688
$C_{13} = C_{14}$ = 110 pF chip capacitor	ATC	111J
$C_{18} = C_{19}$ = 22 pF chip capacitor	Philips NPO	2222 851 13229
$C_{20} = C_{21}$ = 2.2 pF chip capacitor	Johanson	no. 500 R 15 N 2R2 BA
L_1 = 49 mm semi-rigid coax, 2.2 mm ∅	Z_C = 50 Ω	PTFE dielectric, soldered on 2 mm stripline
$L_2 = L_{12}$ = stripline	Z_C = 57 Ω	14.5 × 1.5 mm
$L_3 = L_{13}$ = stripline	Z_C = 57 Ω	12.8 × 1.5 mm
$L_4 = L_{14}$ = stripline	Z_C = 36 Ω	2 × 3 mm
$L_5 = L_{15}$ = stripline	Z_C = 36 Ω	1 × 3 mm
$L_6 = L_{16}$ = stripline	Z_C = 36 Ω	3 × 3 mm
$L_7 = L_{17}$ = stripline	Z_C = 48 Ω	17.7 × 2 mm
$L_8 = L_{18}$ = stripline	Z_C = 36 Ω	8.8 × 3 mm
$L_9 = L_{19}$ = stripline	Z_C = 57 Ω	15.2 × 1.5 mm
L_{10} = 46 mm semi-rigid coax, 2.2 mm ∅	Z_C = 50 Ω	PTFE dielectric, soldered on 2 mm stripline
L_{11} = stripline	Z_C = 50 Ω	49 × 2 mm
L_{20} = stripline	Z_C = 50 Ω	46 × 2 mm
$L_{21} = L_{22}$ = 470 nH micro choke		4322 057 04771
R = 12 Ω	CR 25 type,	2322 211 13129

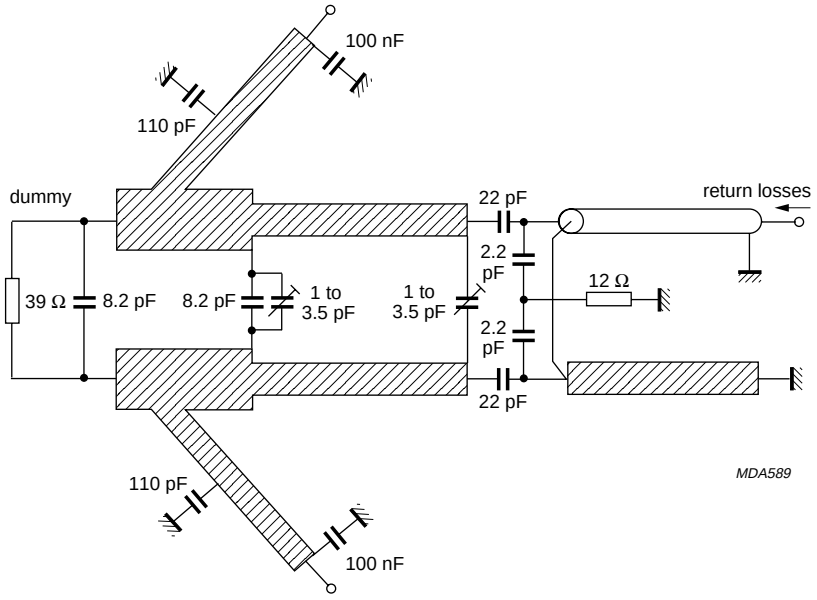

Fig.7 Tuning circuit of the output.

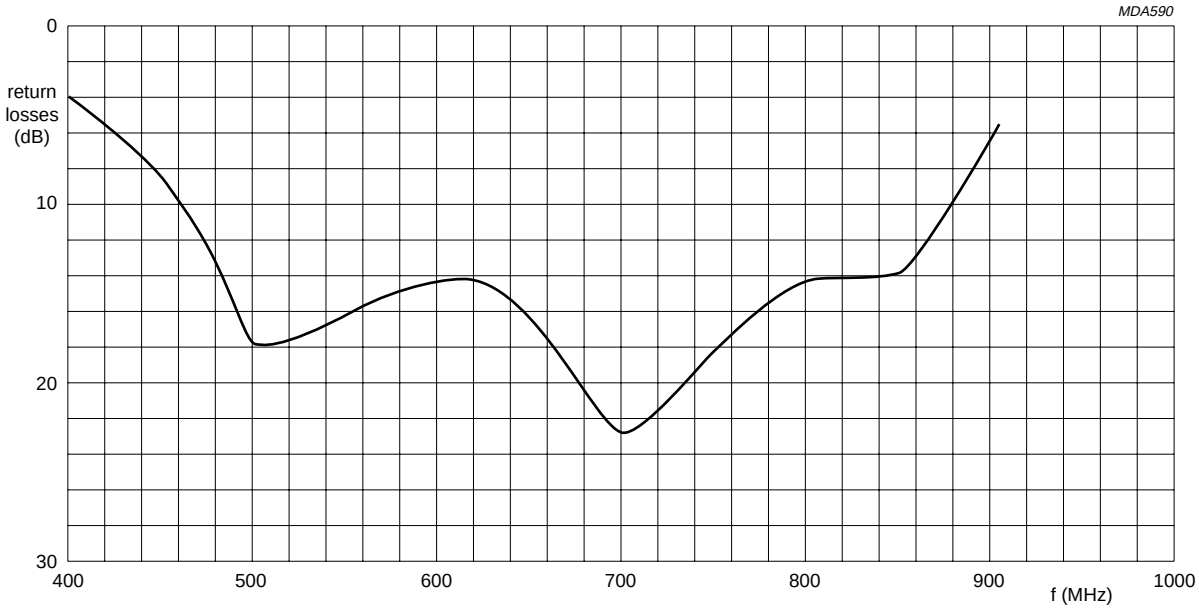

Fig.8 Tuning of the output circuit.

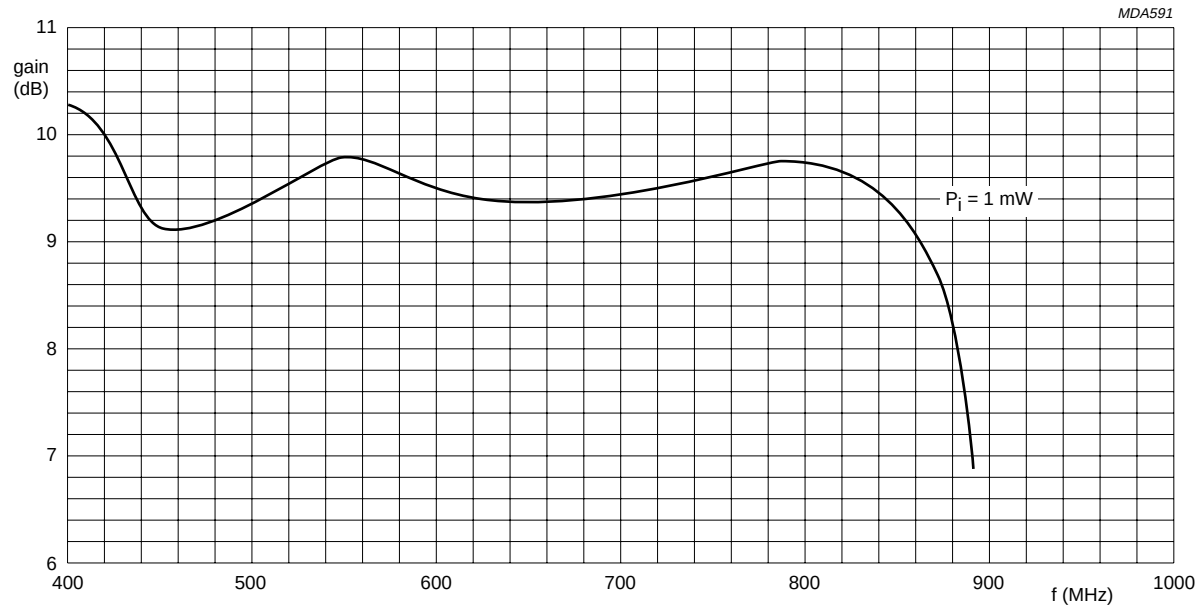

Fig.9 Gain of a BLV57 branch.

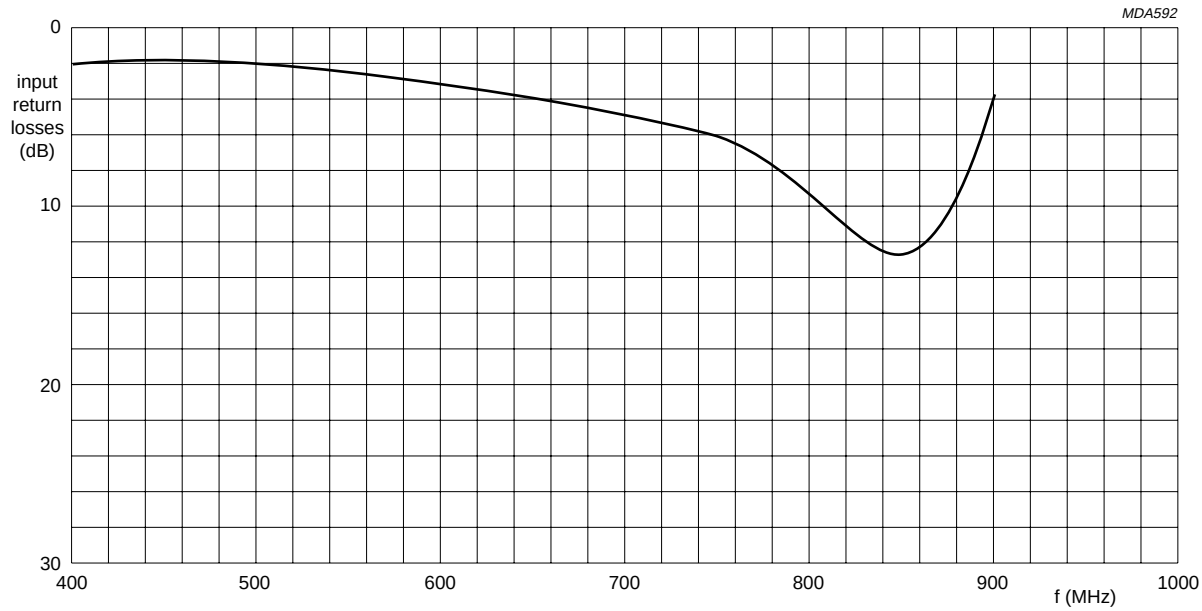

Fig.10 Return losses of a BLV57 branch.

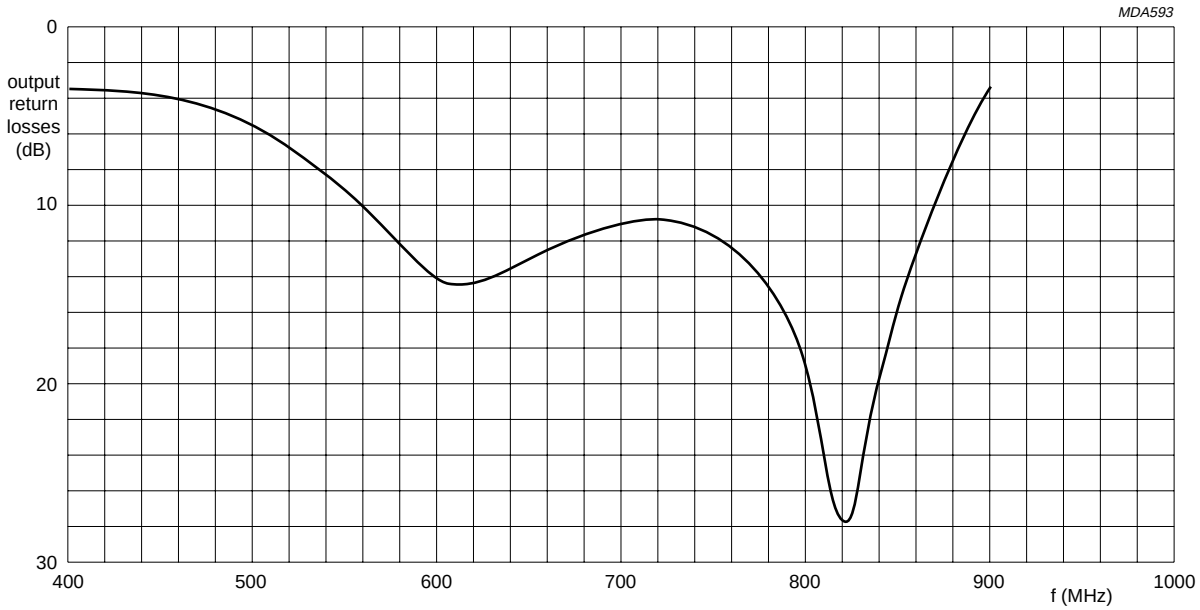

Fig.11 Return losses of a BLV57 branch.

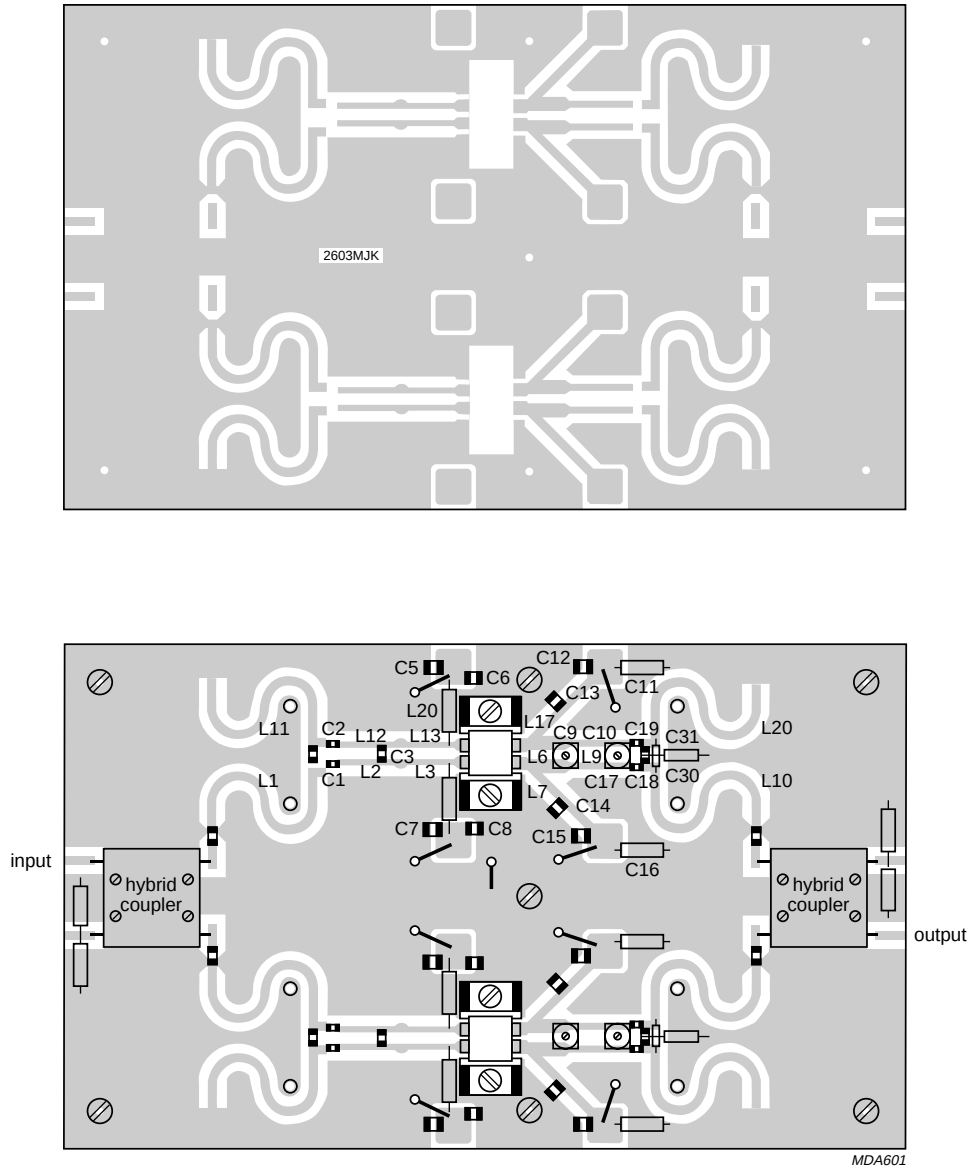

Fig.12 printed-circuit board and lay-out of the BLV57 amplifier.

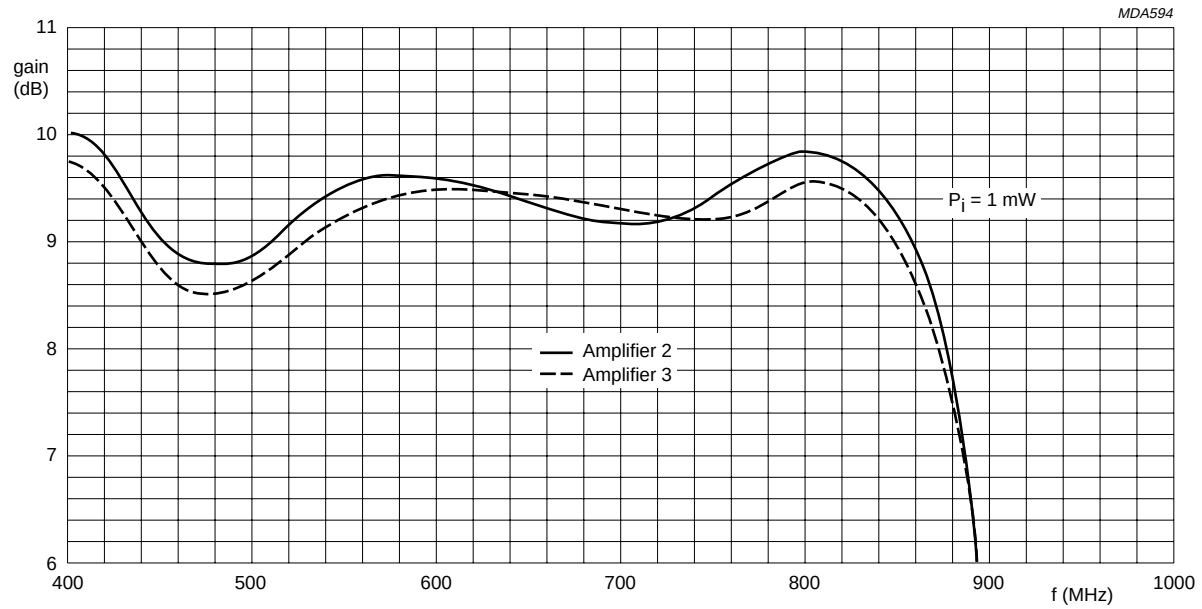

Fig.13 Gain of the BLV57 amplifier.

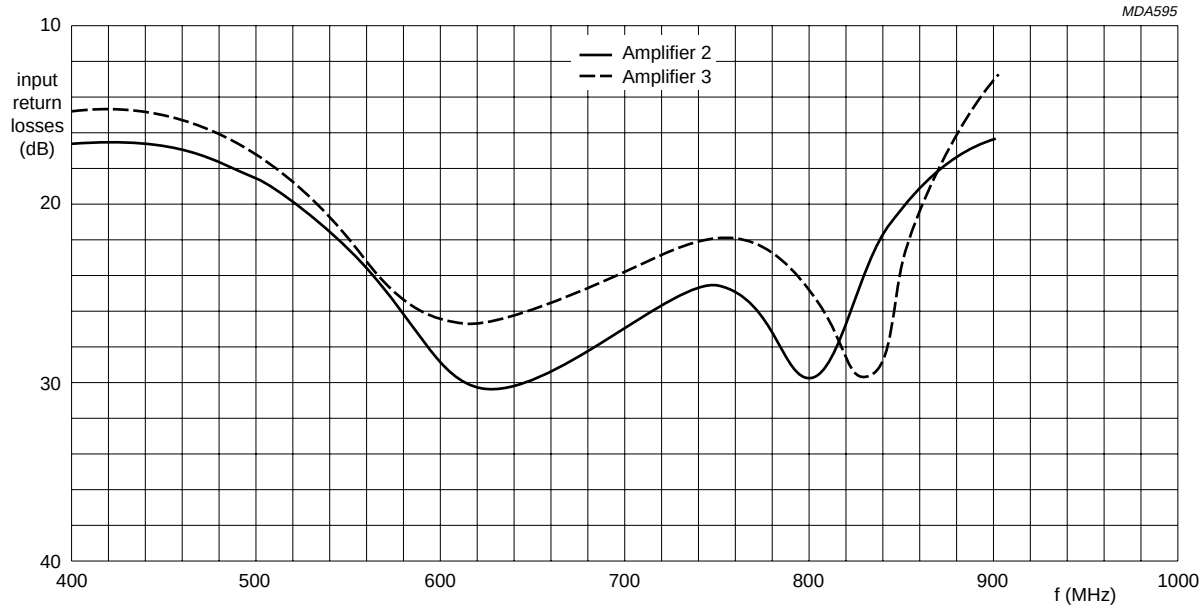

Fig.14 Return losses of the BLV57 amplifier.

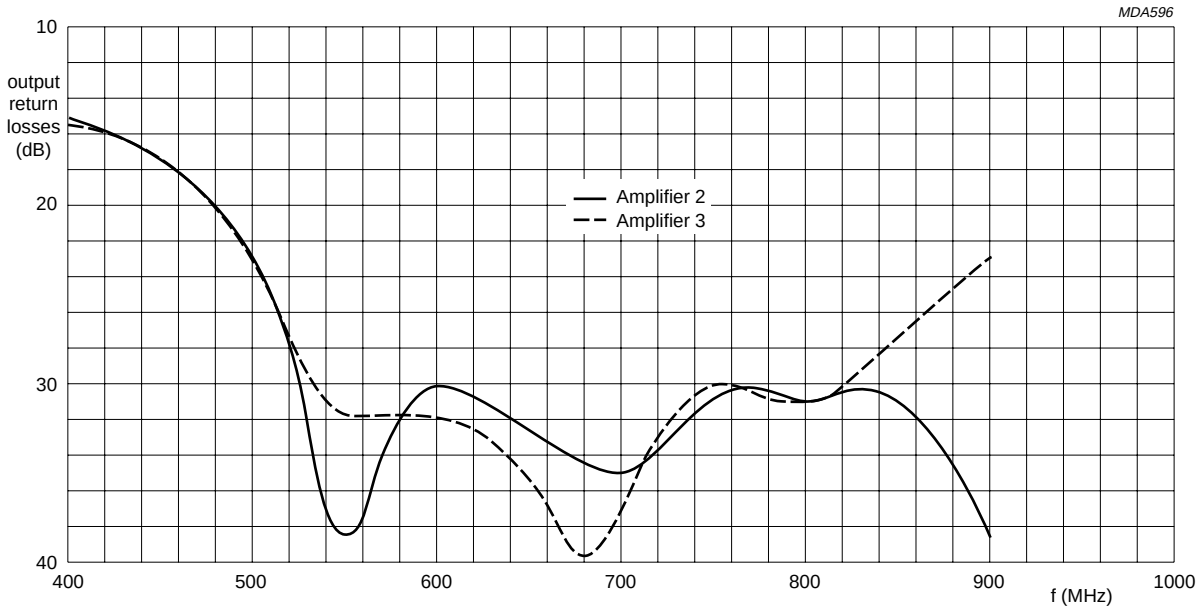

Fig.15 Return losses of the BLV57 amplifier.

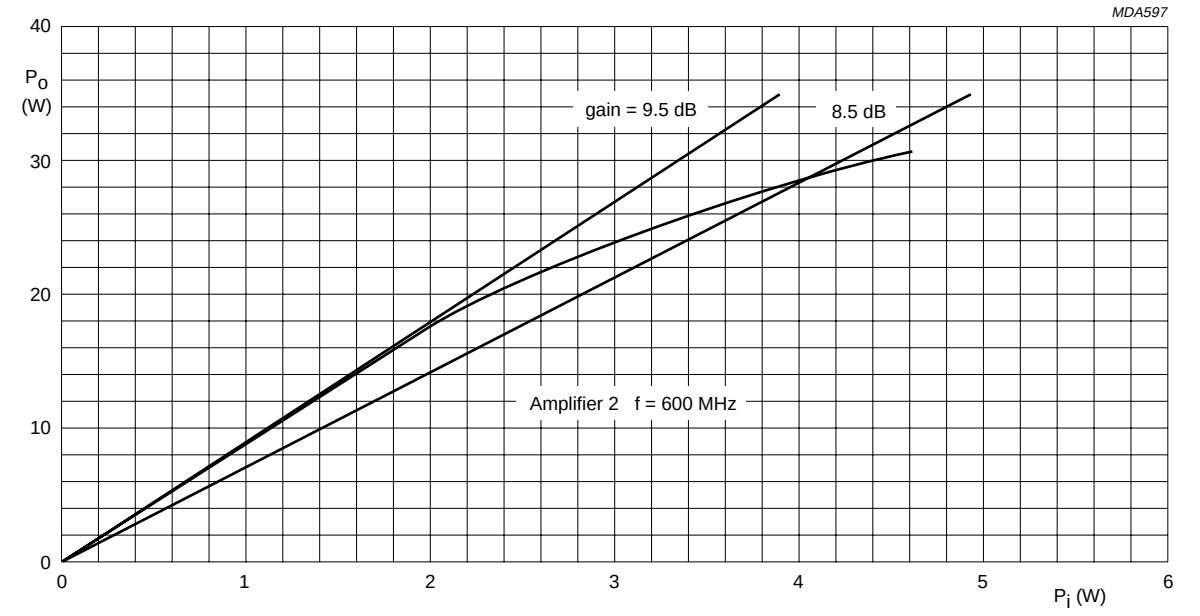

Fig.16 Gain compression of the BLV57 amplifier.

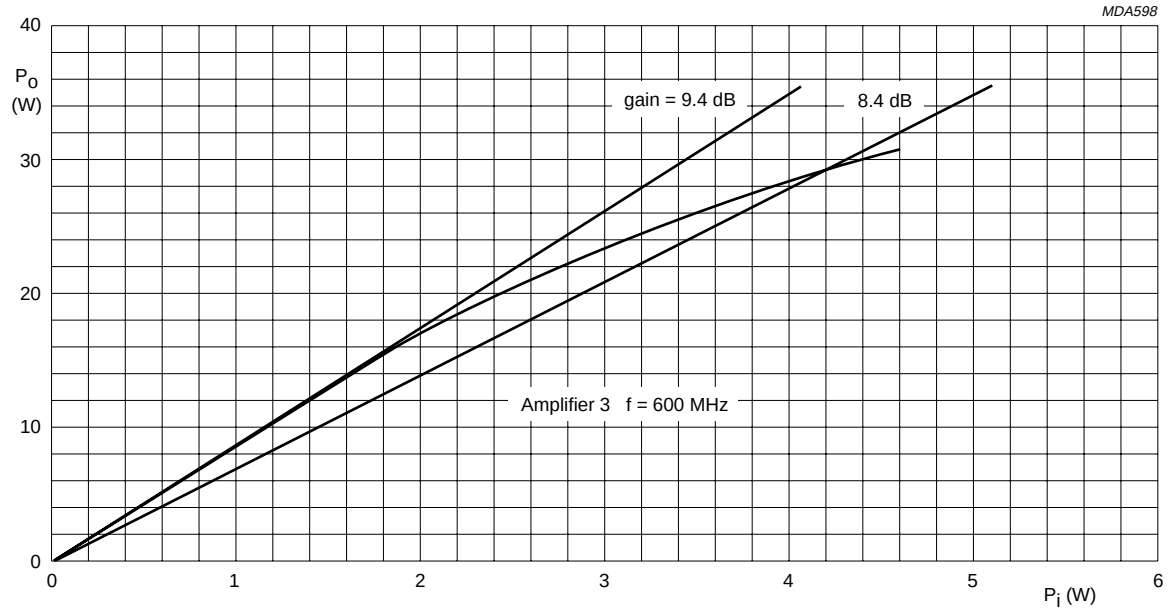

Fig.17 Gain compression of the BLV57 amplifier.

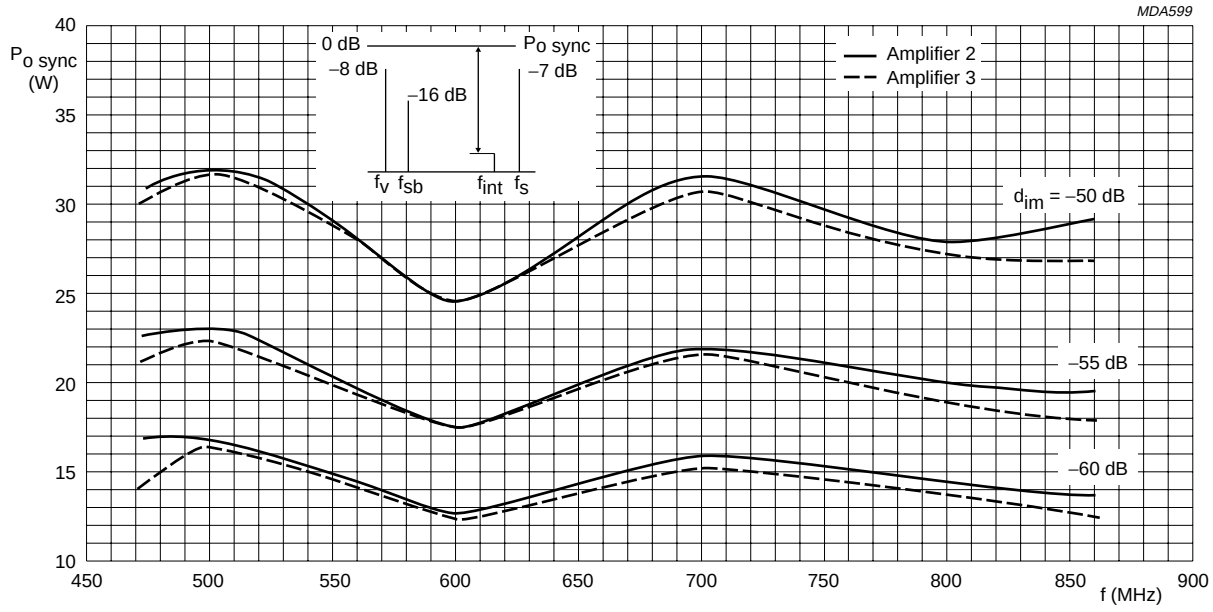

Fig.18 Output power $P_{o\ sync}$ of the BLV57 amplifier.

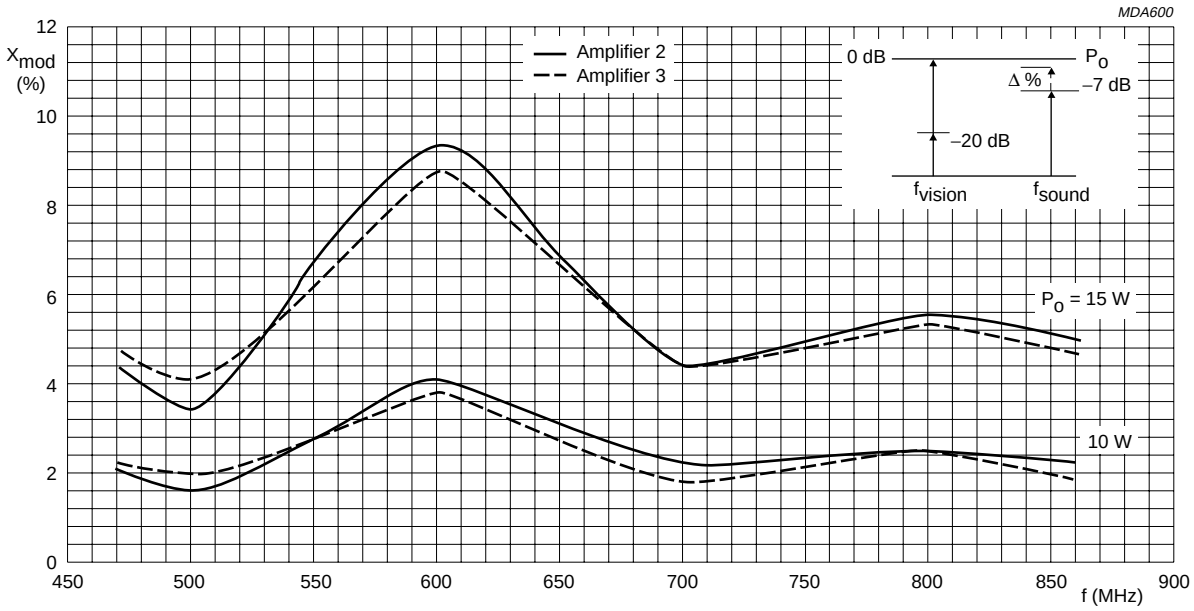

Fig.19 Cross modulation of the BLV57 amplifier.

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