

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

The SN54/74LS390 and SN54/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- Dual Versions of LS290 and LS293
- LS390 has Separate Clocks Allowing ÷2, ÷2.5, ÷5
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects



SN54/74LS390 SN54/74LS393

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

LOW POWER SCHOTTKY



| PIN NAME | ES | LOADIN | G (Note a) |
|-----------------|---|----------|--------------|
| | | HIGH | LOW |
| CP | Clock (Active LOW going edge) Input to +16 (LS393) | 0.5 U.L. | 1.0 U.L. |
| CP ₀ | Clock (Active LOW going edge) Input to ÷2 (LS390) | 0.5 U.L. | 1.0 U.L. |
| CP ₁ | Clock (Active LOW going edge) Input to ÷5 (LS390) | 0.5 U.L. | 1.5 U.L. |
| MR | Master Reset (Active HIGH) Input | 0.5 U.L. | 0.25 U.L. |
| $Q_0 - Q_3$ | Flip-Flop outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |
| NOTES. | | | |

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

FUNCTIONAL DESCRIPTION

Each half of the SN54/74LS393 operates in the Modulo 16 binary sequence, as indicated in the ÷ 16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the LS390 contains a $\div 5$ section that is independent except for the common MR function. The $\div 5$

section operates in 4.2.1 binary sequence, as shown in the $\div 5$ Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a $\div 10$ function <u>having</u> a 50% duty cycle output, con<u>nect</u> the input signal to CP₁ and connect the Q₃ output to the CP₀ input; the Q₀ output provides the desired 50% duty cycle output. If the input frequency is connected to CP₀ and the Q₀ output is connected to CP₁, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.



FAST AND LS TTL DATA

SN54/74LS390 BCD TRUT<u>H TABLE</u> (Input on CP₀; Q₀ CP₁)

| · | | U, | .0 | 17 | _ | | | | |
|-------------|----|----------------|----------------|----------------|---|--|--|--|--|
| COUNT | | OUTPUTS | | | | | | | |
| COUNT | Q3 | Q ₂ | Q ₁ | Q ₀ | | | | | |
| 0 | L | L | L | L | - | | | | |
| 1 | | L | L | н | | | | | |
| 2 | L | L | н | L | | | | | |
| 3 | L | L | н | н | | | | | |
| 3 4 5 | | Н | L | L | | | | | |
| 5 | L | Н | L | н | | | | | |
| 6 | L | н | Н | L | | | | | |
| 7 | L | н | н | н | | | | | |
| 8 | н | L | L | L | | | | | |
| 9 | Н | L | L | н | | | | | |

SN54/74LS390 ÷5 TRUTH TABLE (Input on CP₁)



 $\begin{array}{c} \text{SN54/74LS390} \div 10 \text{ (50\% @ } \text{Q}_{0}\text{)} \\ \text{TRUTH TABLE} \\ \text{(Input on CP}_{1}, \text{Q}_{3} \text{ to CP}_{0}\text{)} \end{array}$

| · · | | | - | ••• | | | |
|-------|----|----------------|----------------|----------------|----------|--|--|
| COUNT | | OUTPUTS | | | | | |
| COUNT | Q3 | Q ₂ | Q ₁ | Q ₀ | | | |
| 0 | L | L | L | L | - | | |
| 1 | L | L | Н | L | | | |
| 2 | L | н | L | L | | | |
| 3 | L | н | н | L | | | |
| 4 | н | L | L | L | | | |
| 5 | L | L | L | н | | | |
| 6 | L | L | Н | Н | | | |
| 7 | L | н | L | н | | | |
| 8 | L | н | н | н | | | |
| 9 | Н | L | L | н | | | |

SN54/74LS393 TRUTH TABLE

| COUNT | | | | | |
|----------------------|-------------|----------------|----------------|------------------|---|
| COUNT | Q3 | Q ₂ | Q ₁ | Q ₀ | |
| 0 1 2 3 | | | | L H L H | • |
| 4 5 6 7 | | Т I I I | LLHH | L H L | |
| 8 9 10 11 | ΗΗΗ | L L L | LLHH | L H L H | |
| 12 13 14 15 | Ξ ΞΞ | тттт | | L H L H | |

H = HIGH Voltage Level L = LOW Voltage Level

GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Тур | Max | Unit |
|----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| Vcc | Supply Voltage | 54 74 | 4.5 4.75 | 5.0 5.0 | 5.5 5.25 | V |
| Т _А | Operating Ambient Temperature Range | 54 74 | -55 0 | 25 25 | 125 70 | °C |
| IOH | Output Current — High | 54, 74 | | | -0.4 | mA |
| IOL | Output Current — Low | 54 74 | | | 4.0 8.0 | mA |

| | | | | Limits | | | | |
|-----------------|--------------------------|---------------------|-----|--------|------|------|---|-------------------------------------|
| Symbol | Parameter | | Min | Тур | Max | Unit | Test Conditions | |
| VIH | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input All Inputs | t HIGH Voltage for |
| Mar | | 54 | | | 0.7 | v | | t LOW Voltage for |
| VIL | Input LOW Voltage | 74 | | | 0.8 | | All Inputs | |
| VIK | Input Clamp Diode Volta | age | | -0.65 | -1.5 | V | $V_{CC} = MIN, I_{IN} = -18 \text{ mA}$ | |
| M | | 54 | 2.5 | 3.5 | | V | $V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$ or V _{IL} per Truth Table | |
| VOH | Output HIGH Voltage | 74 | 2.7 | 3.5 | | V | | |
| M | | 54, 7 | 4 | 0.25 | 0.4 | V | $I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$ | |
| VOL | Output LOW Voltage | 74 | | 0.35 | 0.5 | V | I _{OL} = 8.0 mA | VIN = VIL or VIH per Truth Table |
| I | | - | | | 20 | μΑ | V _{CC} = MAX, V _{IN} | = 2.7 V |
| ΙΗ | Input HIGH Current | | | | 0.1 | mA | V _{CC} = MAX, V _{IN} | = 7.0 V |
| | | MR | | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V | |
| ۱ _{IL} | Input LOW Current | CP, CP ₀ | | | -1.6 | mA | | |
| | | CP ₁ | | | -2.4 | mA | | |
| los | Short Circuit Current (N | ote 1) | -20 | | -100 | mA | V _{CC} = MAX | |
| ICC | Power Supply Current | | | | 26 | mA | V _{CC} = MAX | |

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$)

| | | | Limits | | | | |
|--------------------------------------|--|-----------|--------|----------|----------|------|------------------------|
| Symbol | Parameter | | Min | Тур | Max | Unit | Test Conditions |
| fMAX | M <u>axi</u> mum Clock Freq CP ₀ to Q ₀ | uency | 25 | 35 | | MHz | |
| fMAX | M <u>axi</u> mum Clock Freq CP ₁ to Q ₁ | uency | 20 | | | MHz | |
| ^t PLH ^t PHL | Pr <u>opag</u> ation Delay, CP to Q ₀ | LS393 | | 12 13 | 20 20 | ns | |
| ^t PLH ^t PHL | $\overline{CP_0}$ to Q ₀ | LS390 | | 12 13 | 20 20 | ns | |
| ^t PLH ^t PHL | CP to Q ₃ | LS393 | | 40 40 | 60 60 | ns | C _L = 15 pF |
| ^t PLH ^t PHL | \overline{CP}_0 to Q_2 | LS390 | | 37 39 | 60 60 | ns | |
| ^t PLH ^t PHL | CP ₁ to Q ₁ | LS390 | | 13 14 | 21 21 | ns | |
| ^t PLH ^t PHL | $\overline{\text{CP}}_1$ to Q ₂ | LS390 | | 24 26 | 39 39 | ns | |
| ^t PLH ^t PHL | $\overline{CP_1}$ to Q ₃ | LS390 | | 13 14 | 21 21 | ns | |
| ^t PHL | MR to Any Output | LS390/393 | | 24 | 39 | ns | |

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

| | | | Limits | | | | |
|------------------|-------------------|-----------|--------|-----|-----|------|------------------|
| Symbol | Paramet | ter | Min | Тур | Max | Unit | Test Conditions |
| tw | Clock Pulse Width | LS393 | 20 | | | ns | |
| tw | CP0 Pulse Width | LS390 | 20 | | | ns | |
| tW | CP1 Pulse Width | LS390 | 40 | | | ns | $V_{CC} = 5.0 V$ |
| tw | MR Pulse Width | LS390/393 | 20 | | | ns | |
| t _{rec} | Recovery Time | LS390/393 | 25 | | | ns | |

AC WAVEFORMS





*The number of Clock Pulses required between tPHL and tPLH measurements can be determined from the appropriate Truth Table.

Case 751B-03 D Suffix **16-Pin Plastic** SO-16



Case 648-08 N Suffix **16-Pin Plastic**





- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER. DIMENSION A AND B DO NOT INCLUDE MOLD 2 3.
- PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 (0.006) 4.
- PER SIDE. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03. 5.

| | MILLIM | ETERS | INC | HES |
|-----|--------|------------|-------|-------|
| DIM | MIN | MAX | MIN | MAX |
| Α | 9.80 | 10.00 | 0.386 | 0.393 |
| В | 3.80 | 4.00 | 0.150 | 0.157 |
| С | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 | BSC | 0.050 | BSC |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| М | 0° | 7 ° | 0° | 7° |
| Р | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2.
- CONTROLLING DIMENSION: INCH. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL. 3.
- DIMENSION "B" DOES NOT INCLUDE MOLD 4. FLASH.
- 5.
- ROUNDED CORNERS OPTIONAL. 648-01 THRU -07 OBSOLETE, NEW STANDARD 6. 648-08.

| | MILLIM | ETERS | INC | HES | |
|-----|-----------|-------|-----------|-------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 18.80 | 19.55 | 0.740 | 0.770 | |
| В | 6.35 | 6.85 | 0.250 | 0.270 | |
| С | 3.69 | 4.44 | 0.145 | 0.175 | |
| D | 0.39 0.53 | | 0.015 | 0.021 | |
| F | 1.02 | 1.77 | 0.040 | 0.070 | |
| G | 2.54 | BSC | 0.100 BSC | | |
| н | 1.27 | BSC | 0.050 BSC | | |
| J | 0.21 | 0.38 | 0.008 | 0.015 | |
| ĸ | 2.80 | 3.30 | 0.110 | 0.130 | |
| L | 7.50 | 7.74 | 0.295 | 0.305 | |
| М | 0° | 10° | 0° | 10° | |
| S | 0.51 | 1.01 | 0.020 | 0.040 | |

- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY. 5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

- 620-09.

| | MILLIM | ETERS | INCHES | | |
|-----|--------|----------|-----------|-------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 19.05 | 19.55 | 0.750 | 0.770 | |
| В | 6.10 | 7.36 | 0.240 | 0.290 | |
| С | _ | 4.19 | - | 0.165 | |
| D | 0.39 | 0.53 | 0.015 | 0.021 | |
| E | 1.27 | BSC | 0.050 BSC | | |
| F | 1.40 | 1.77 | 0.055 | 0.070 | |
| G | 2.54 | BSC | 0.100 BSC | | |
| J | 0.23 | 0.27 | 0.009 | 0.011 | |
| K | _ | 5.08 | _ | 0.200 | |
| L | 7.62 | 7.62 BSC | | BSC | |
| M | 0° | 15° | 0° | 15° | |
| N | 0.39 | 0.88 | 0.015 | 0.035 | |

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