### **Power Products Division**

# Advance Information **HALF-BRIDGE DRIVER**

The MPIC2111 is a high voltage, high speed, power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for halfbridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- CMOS Schmitt-triggered Inputs with Pull-down
- Matched Propagation Delay for Both Channels
- Internally Set Deadtime
- High Side Output in Phase with Input

#### PRODUCT SUMMARY

| VOFFSET                       | 600 V MAX     |
|-------------------------------|---------------|
| I <sub>O+/-</sub>             | 200 mA/420 mA |
| VOUT                          | 10 – 20 V     |
| t <sub>on/off</sub> (typical) | 130 & 90 ns   |
| Deadtime (typical)            | 700 ns        |



#### **ORDERING INFORMATION**

| Device    | Package |
|-----------|---------|
| MPIC2111D | SOIC    |
| MPIC2111P | PDIP    |

10TOROLA



This document contains information on a new product. Specifications and information herein are subject to change without notice.





#### ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Rating   |                               | Symbol                               | Min   | Max   | Unit            |
|--|-------------------------------|--------------------------------------|---|---|-----------------|
| High Side Floating Supply Absolute Voltage<br>High Side Floating Supply Offset Voltage<br>High Side Floating Output Voltage<br>Low Side Fixed Supply Voltage<br>Low Side Output Voltage<br>Logic Input Voltage |                               | VB<br>VS<br>VHO<br>VCC<br>VLO<br>VIN | -0.3<br>V <sub>B</sub> -25<br>V <sub>S</sub> -0.3<br>-0.3<br>-0.3<br>-0.3 | 625<br>V <sub>B</sub> +0.3<br>V <sub>B</sub> +0.3<br>25<br>V <sub>CC</sub> +0.3<br>V <sub>CC</sub> +0.3 | V <sub>DC</sub> |
| Allowable Offset Supply Voltage Transient  |                               | dV <sub>S</sub> /dt                  | -   | 50  | V/ns            |
| *Package Power Dissipation @ $T_C \le +25^{\circ}C$  | (8 Lead DIP)<br>(8 Lead SOIC) | PD<br>-                              |   | 1.0<br>0.625  | Watt            |
| Thermal Resistance, Junction to Ambient  | (8 Lead DIP)<br>(8 Lead SOIC) | R <sub>θJA</sub>                     |   | 125<br>200  | °C/W            |
| Operating and Storage Temperature  |                               | T <sub>j</sub> , T <sub>stg</sub>    | -55   | 150   | °C              |
| Lead Temperature for Soldering Purposes, 10 sec  | conds                         | ΤL                                   | -   | 260   | °C              |

#### **RECOMMENDED OPERATING CONDITIONS**

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15 V differential.

| High Side Floating Supply Absolute Voltage | VB              | V <sub>S</sub> +10 | V <sub>S</sub> +20 | V  |
|--|-----------------|--------------------|--------------------|----|
| High Side Floating Supply Offset Voltage   | VS              | Note 1             | 600                |    |
| High Side Floating Output Voltage          | VHO             | ٧ <sub>S</sub>     | VB                 |    |
| Low Side Fixed Supply Voltage              | Vcc             | 10                 | 20                 |    |
| Low Side Output Voltage                    | VLO             | 0                  | V <sub>CC</sub>    | mA |
| Logic Input Voltage                        | V <sub>IN</sub> | 0                  | V <sub>CC</sub>    |    |
| Ambient Temperature                        | Т <sub>А</sub>  | -40                | 125                | °C |

Note 1: Logic operational for V<sub>S</sub> of -5 to +600 V. Logic state held for V<sub>S</sub> of -5 V to  $-V_{BS}$ .

Unit

Max

#### **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C unless otherwise specified)

## Characteristic STATIC ELECTRICAL CHARACTERISTICS

 $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol

Min

Тур

|   | -                   |      |     |     |                 |
|---|---------------------|------|-----|-----|-----------------|
| Logic "1" Input Voltage for HO & Logic "0" Input Voltage for LO @ V_CC = 10 V | VIH                 | 6.4  | -   | -   | V <sub>DC</sub> |
| Logic "1" Input Voltage for HO & Logic "0" Input Voltage for LO @ V_CC = 15 V | VIH                 | 9.5  | -   | -   |                 |
| Logic "1" Input Voltage for HO & Logic "0" Input Voltage for LO @ V_CC = 20 V | VIH                 | 12.6 | -   | -   |                 |
| Logic "0" Input Voltage for HO & Logic "1" Input Voltage for LO @ V_CC = 10 V | VIL                 | -    | -   | 3.8 |                 |
| Logic "0" Input Voltage for HO & Logic "1" Input Voltage for LO @ V_CC = 15 V | VIL                 | _    | -   | 6.0 |                 |
| Logic "0" Input Voltage for HO & Logic "1" Input Voltage for LO @ V_CC = 20 V | VIL                 | -    | -   | 8.3 |                 |
| High Level Output Voltage, $V_{BIAS} - V_O @ I_O = 0 A$                       | VOH                 | -    | -   | 100 | mV              |
| Low Level Output Voltage, VO @ IO = 0 A                                       | VOL                 | -    | -   | 100 |                 |
| Offset Supply Leakage Current @ $V_B = V_S = 600 V$                           | I <sub>LK</sub>     | -    | -   | 50  | μA              |
| Quiescent V <sub>BS</sub> Supply Current @ $V_{IN}$ = 0 V or V <sub>CC</sub>  | IQBS                | -    | 50  | -   |                 |
| Quiescent V <sub>CC</sub> Supply Current @ $V_{IN} = 0$ V or V <sub>CC</sub>  | IQCC                | -    | 70  | -   |                 |
| Logic "1" Input Bias Current @ V <sub>IN</sub> = 15 V                         | I <sub>IN+</sub>    | -    | 20  | 40  |                 |
| Logic "0" Input Bias Current @ VIN = 0 V                                      | I <sub>IN</sub>     | -    | -   | 1.0 |                 |
| VBS Supply Undervoltage Positive Going Threshold                              | V <sub>BSUV+</sub>  | -    | 8.5 | -   | V               |
| VBS Supply Undervoltage Negative Going Threshold                              | V <sub>BSUV</sub> - | -    | 8.2 | -   |                 |
| V <sub>CC</sub> Supply Undervoltage Positive Going Threshold                  | V <sub>CCUV+</sub>  | -    | 8.6 | -   |                 |
| V <sub>CC</sub> Supply Undervoltage Negative Going Threshold                  | VCCUV-              | _    | 8.2 | -   |                 |
| Output High Short Circuit Pulsed Current @ VOUT = 0 V, PW $\leq$ 10 $\mu s$   | IO+                 | 200  | 250 | -   | mA              |
| Output Low Short Circuit Pulsed Current @ V_OUT = 15 V, PW $\leq$ 10 $\mu s$  | I0-                 | 420  | 500 | -   |                 |
|   |                     |      |     |     |                 |

#### DYNAMIC ELECTRICAL CHARACTERISTICS

 $V_{BIAS}$  (V<sub>CC</sub>,  $V_{BS}$ ) = 15 V unless otherwise specified

| Turn–On Propagation Delay @ $V_S = 0 V$                         | ton              | - | 850 | - | ns |
|---|------------------|---|-----|---|----|
| Turn–Off Propagation Delay @ $V_S = 600 V$                      | <sup>t</sup> off | _ | 150 | - |    |
| Turn–On Rise Time @ CL = 1000 pF                                | tr               | - | 80  | - |    |
| Turn–Off Fall Time @ C <sub>L</sub> = 1000 pF                   | tf               | - | 40  | - |    |
| Deadtime, LS Turn–Off to HS Turn–On & HS Turn–Off to LS Turn–On | DT               | - | 700 | - |    |
| Delay Matching, HS & LS Turn–On/Off                             | MT               | - | 30  | - |    |

#### **TYPICAL CONNECTION**



#### MPIC2111

#### LEAD DEFINITIONS

| Symbol         | Lead Description   |
|----------------|--|
| IN             | Logic Input for High Side and Low Side Gate Driver Outputs (HO & LO), In Phase with HO |
| VB             | High Side Floating Supply  |
| НО             | High Side Gate Drive Output  |
| ٧ <sub>S</sub> | High Side Floating Supply Return   |
| Vcc            | Low Side Supply  |
| LO             | Low Side Gate Drive Output   |
| СОМ            | Logic and Low Side Return  |



Figure 1. Input / Output Timing Diagram



Figure 2. Switching Time Waveform Definitions



Figure 3. Deadtime Waveform Definitions

#### MPIC2111

#### PACKAGE DIMENSIONS



**MPIC2111** 

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