Product Preview

Low Voltage PLL Clock Driver

MPC990
MPC991

LOW VOLTAGE PLL CLOCK DRIVER

The MPC990/991 is a 3.3V compatible, PLL based ECL/PECL clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC990/991 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC990 and MPC991 devices are identical except in the interface to the reference clock for the PLL. The MPC990 offers an on–board crystal oscillator as the PLL reference while the MPC991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. Both designs offer a secondary single–ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency Up to 400MHz
- ECL/PECL Inputs and Outputs
- Operates from Either a 3.3V or 5.0V Supply
- Output Frequency Configurable
- TQFP Packaging
- ±25ps Cycle–to–Cycle Jitter

52 1

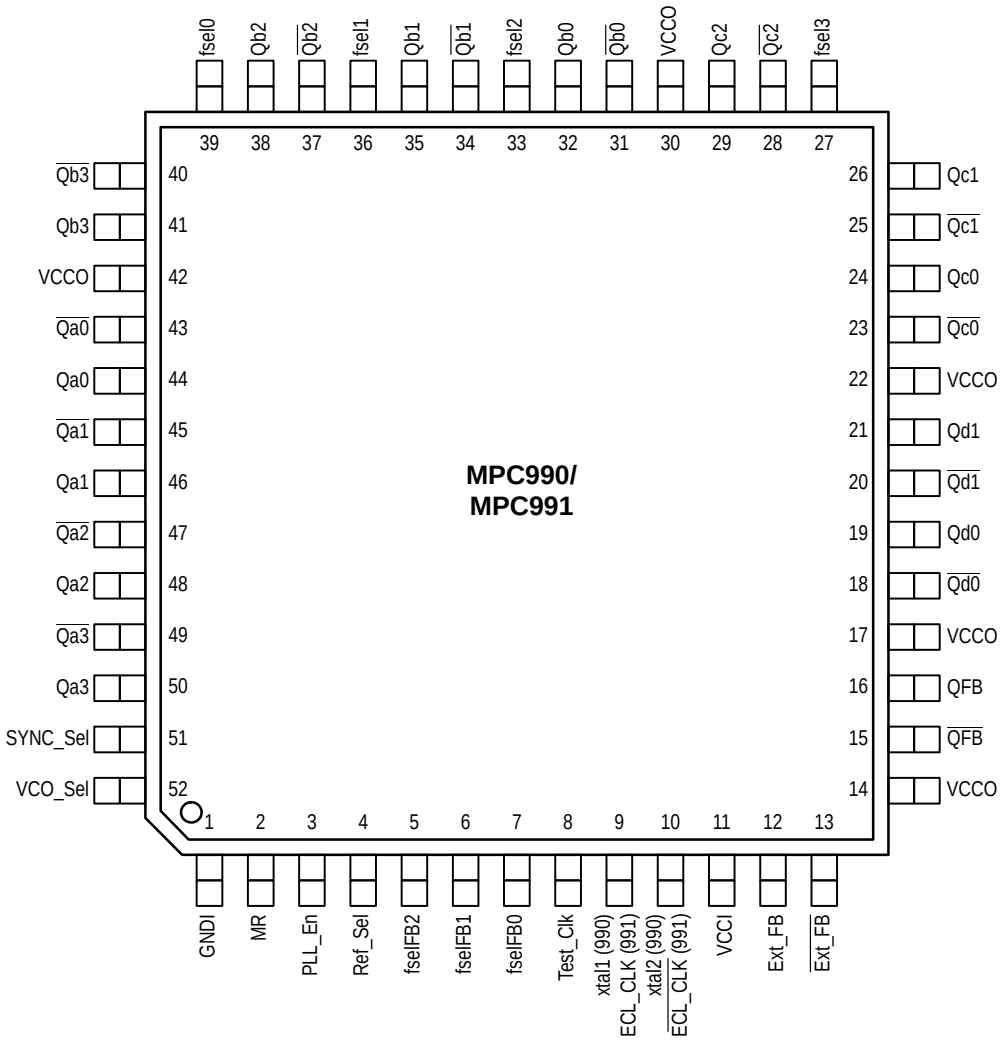
FA SUFFIX
TQFP PACKAGE
CASE 848D–02

The MPC990/991 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1 and 4:3, in addition the three banks can be configured to three different output frequencies. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet to signal the coincident edges of the two output banks. This features is useful full non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC990/991 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allwoing for unique input vs output frequency relationships. The FselFB inputs provide 6 different feedback frequencies from the QFB differential output pair.

The MPC990/991 features an external differential ECL/PECL feedback to the PLL. This external feedback features allows for the MPC991's use as a "zero" delay buffer. The propagation delay of between the input reference and the output is dependent on the feedback division ratio. proper selection of the feedback divisor will provide near zero delay through the device.

The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that depending on the programming several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.



FUNCTION TABLE 1

INPUTS				OUTPUTS		
fsel3	**fsel2**	**fsel1**	**fsel0**	**Qa**	**Qb**	**Qc**
0	0	0	0	÷2	÷2	÷2
0	0	0	1	÷2	÷2	÷4
0	0	1	0	÷2	÷4	÷4
0	0	1	1	÷2	÷2	÷6
0	1	0	0	÷2	÷6	÷6
0	1	0	1	÷2	÷4	÷6
0	1	1	0	÷2	÷4	÷8
0	1	1	1	÷2	÷6	÷8
1	0	0	0	÷2	÷2	÷8
1	0	0	1	÷2	÷8	÷8
1	0	1	0	÷4	÷4	÷6
1	0	1	1	÷4	÷6	÷6
1	1	0	0	÷4	÷6	÷8
1	1	0	1	÷6	÷6	÷8
1	1	1	0	÷6	÷8	÷8
1	1	1	1	÷8	÷8	÷8

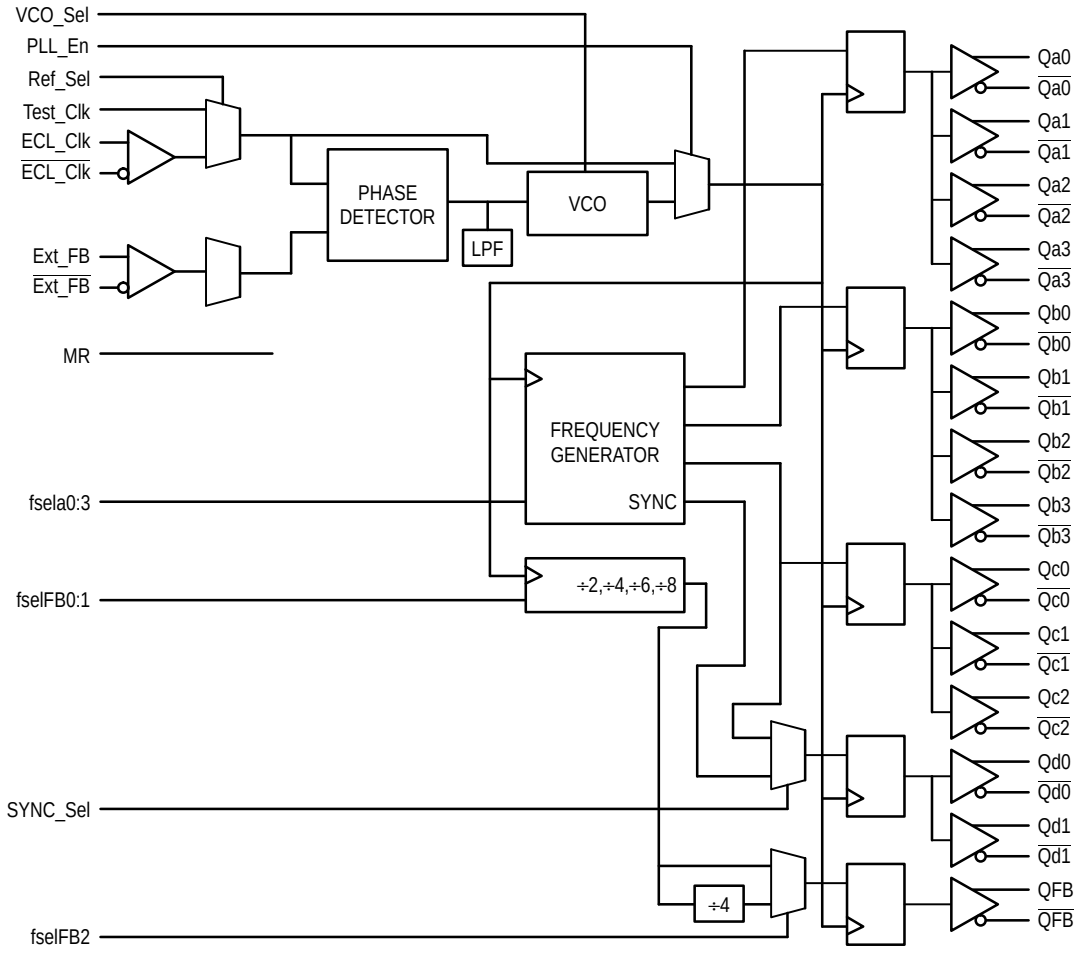
FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷2
0	0	1	÷4
0	1	0	÷6
0	1	1	÷8
1	0	0	÷8
1	0	1	÷16
1	1	0	÷24
1	1	1	÷32

FUNCTION TABLE 3

Control Pin	Logic ‘0’	Logic ‘1’
PLL_En	Enable PLL	Bypass PLL
VCO_Sel	fVCO	fVCO/2
Ref_Sel	xtal or ECL/PECL	Test_Clk
MR	—	Reset Outputs
SYNC_Sel	SYNC Outputs	Match Qc Outputs

MPC990/991 LOGIC DIAGRAM



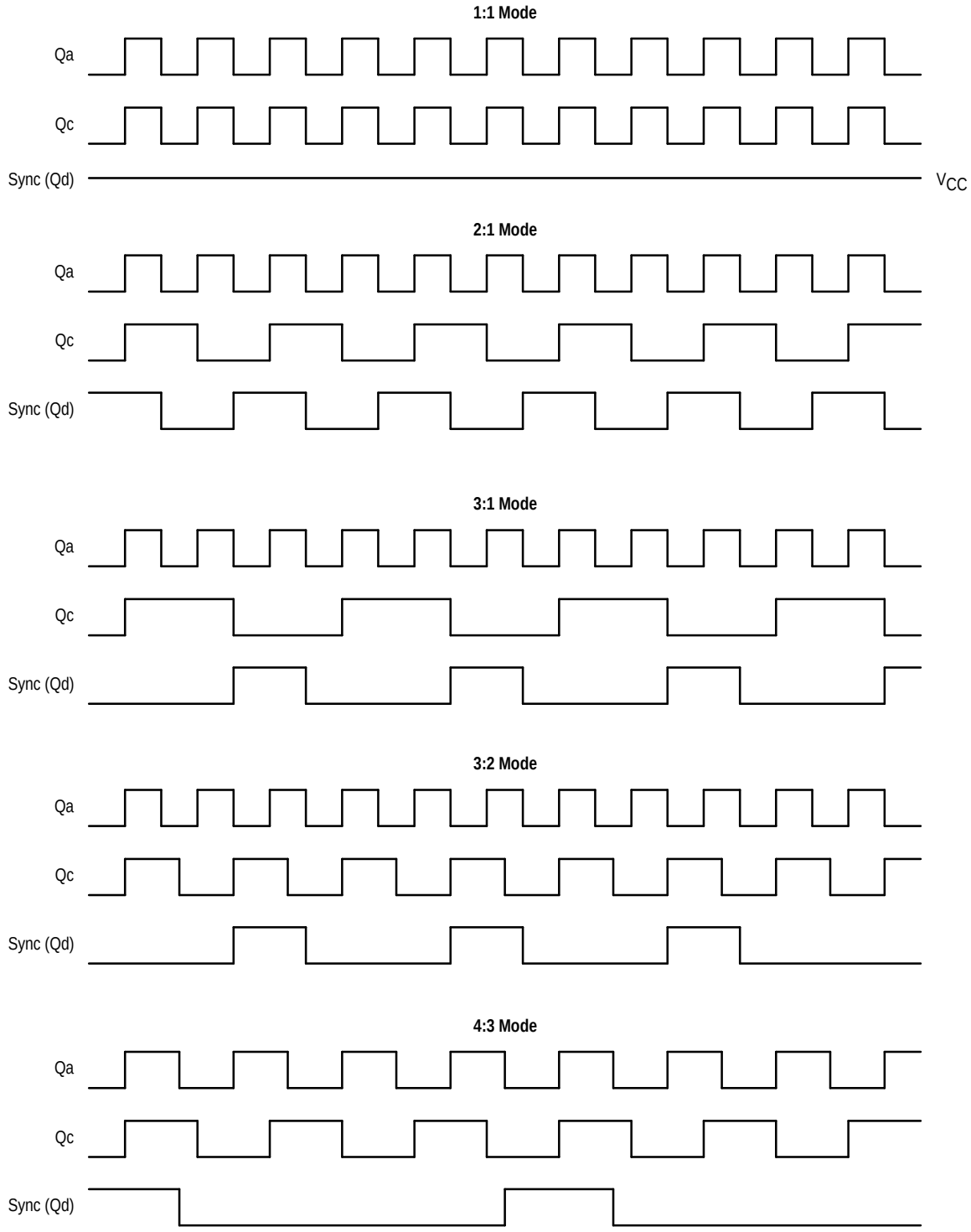


Figure 1. Timing Diagrams

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.2		0.8	ns	20% to 80%
t_{pw}	Output Duty Cycle		50 ±1%	%	ps	
t_{os}	Output-to-Output Skew Same Frequency Different Frequencies PCLK (–) to SYNC (+)			100 200 300	ps	
f_{VCO}	PLL VCO Lock Range Feedback = VCO/4 Feedback = VCO/6 Feedback = VCO/8 Feedback = VCO/12 Feedback = VCO/16 Feedback = VCO/24 Feedback = VCO/32	TBD TBD TBD TBD TBD TBD TBD	500–800 500–800 500–800 500–800 500–800 500–800 500–800	TBD TBD TBD TBD TBD TBD TBD	MHz	
f_{max}	Maximum Output Frequency Qa,Qb,Qc (÷2) Qa,Qb,Qc (÷4) Qa,Qb,Qc (÷6) Qa,Qb,Qc (÷8)			400 200 133 100	MHz	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±25	±50	ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MPC990/991 features an on–board crystal oscillator to allow for seed clock generaytion as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC990/991 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. In addition, with crystals with a higher shunt capacitance, it may be necessary to place a 1k resistor across the two crystal leads.

The oscillator circuit is a series resonant circuit as oppossed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC990/991 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 1. Crystal Specifications

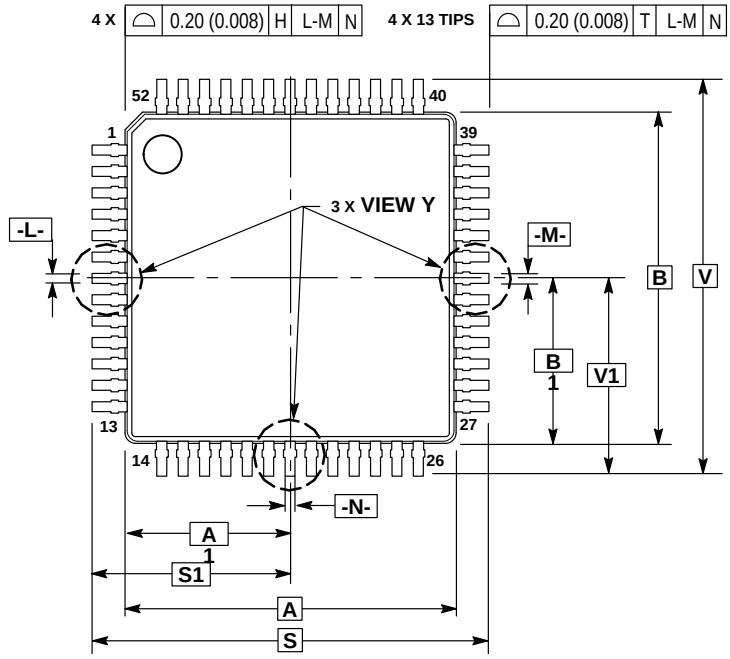
Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5pF Max
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100µW
Aging	5ppm/Yr (First 3 Years)

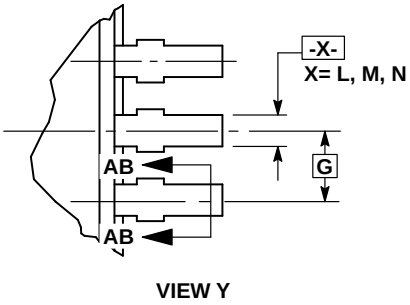
* See accompanying text for series versus parallel resonant discussion.

The MPC990/991 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal.

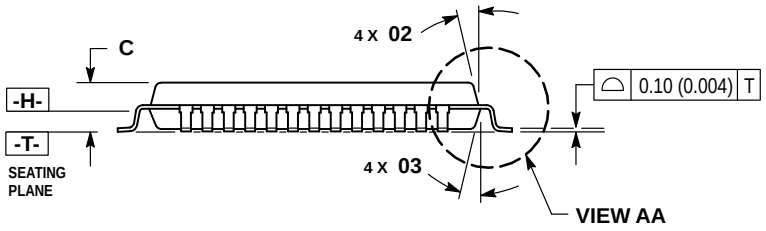
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D-02
ISSUE A





VIEW Y



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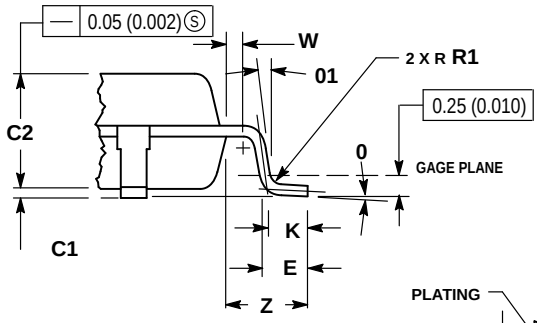

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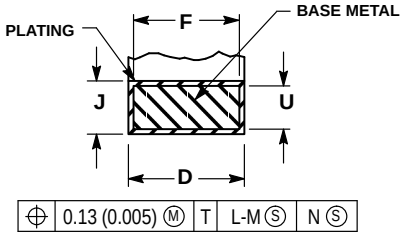

SECTION AB-AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.007 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.60	—	0.063
C1	0.05	0.15	0.002	0.006
C2	1.35	1.45	0.053	0.057
D	0.22	0.38	0.009	0.015
E	0.45	0.75	0.018	0.030
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
K	0.50 REF		0.020 REF	
R1	0.10	0.20	0.004	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
0	0°	7°	0°	7°
01	0°	—	0°	—
02	12° REF		12° REF	
03	5°	13°	5°	13°

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