Product Preview

Dual 3.3V PLL Clock Generator

MPC980

DUAL 3.3V PLL CLOCK GENERATOR

The MPC980 is a 3.3V dual PLL clock generator targeted for high end Pentium™ and PowerPC™ 603/604 personal computers. The MPC980 synthesizes processor as well as PCI clocks from a 14.31818MHz external crystal. In addition the device provides two buffered outputs of the 14.31818MHz crystal as well as a 40MHz SCSI clock, a 24MHz floppy clock and a12MHz keyboard clock. One of the buffered 14.31818MHz outputs can be configured to provide a 16MHz output rather than the second copy of the 14.31818MHz output.

- Provides Processor and System Clocks for Pentium™ Designs
- Provides Processor and System Clocks for PowerPC™ 603/604 Designs
- Two Fully Integrated Phase–Locked Loops
- Cycle–Cycle Jitter of ±150ps
- Operates from 3.3V Supply
- 52–Lead TQFP Packaging

52 1

FA SUFFIX
TQFP PACKAGE
CASE 848D–02

The processor clock outputs of the MPC980 can be programmed to provide 50, 60 or 66MHz. Under all processor output frequencies the PCI clock outputs will be equal to one half the processor clock outputs. The PCI outputs will run synchronously to the processor clock outputs. There are a total of ten output clocks which can be split into a group of four and a group of six. Either group can be configured as processor or PCI clocks. Each of the outputs can drive two series terminated transmission lines allowing for the driving of up to twelve independent processor loads and eight PCI clock loads. A pin selectable option is available to delay the PCI clock outputs relative to the processor clocks. The amount of delay is a function of the processor clock frequency and varies from 1.8ns to 2.6ns.

The output jitter of the the PLL is ±150ps peak to peak, cycle to cycle (the worst case deviation of the clock period is guaranteed to be less than ±150ps). The skews between one processor clock and any other processor clock (or one PCI clock to any other PCI clock) is 350ps (±175ps). The worst case skew between the processor clocks and the PCI clocks is 500ps (±250ps).

An output enable pin is provided to tristate all of the outputs for board level test. In addition a testing mode is provided to allow for the bypass of the PLL's for board level functional debug.

The product is packaged in a 52–lead TQFP to optimize board space and power supply distribution. The TQFP package occupies a 12mm x 12mm space on the PCB.

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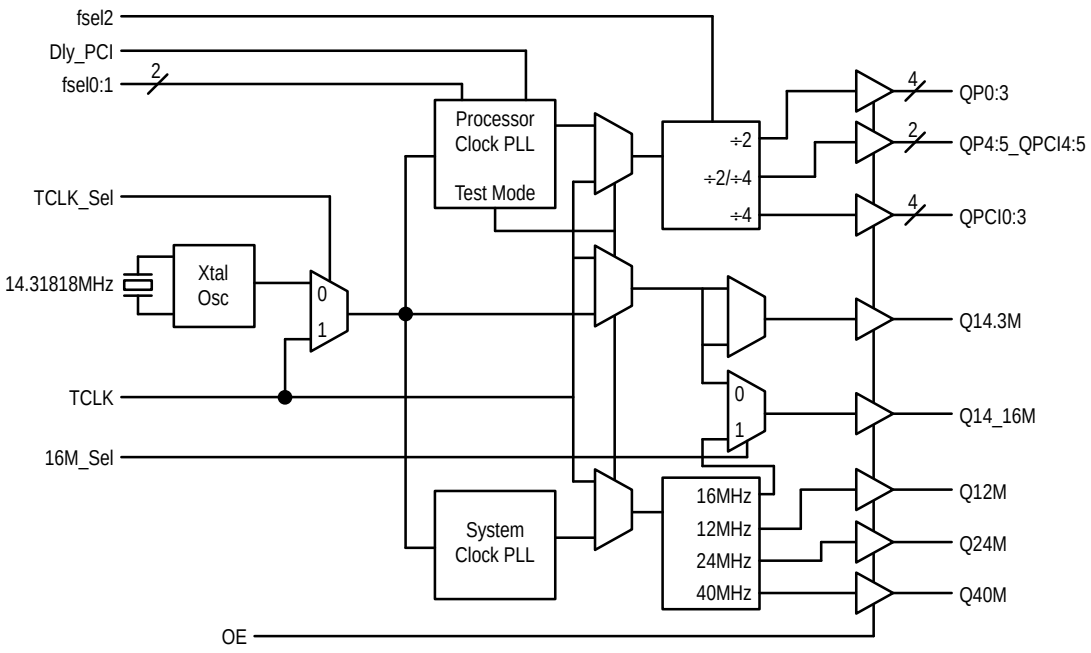
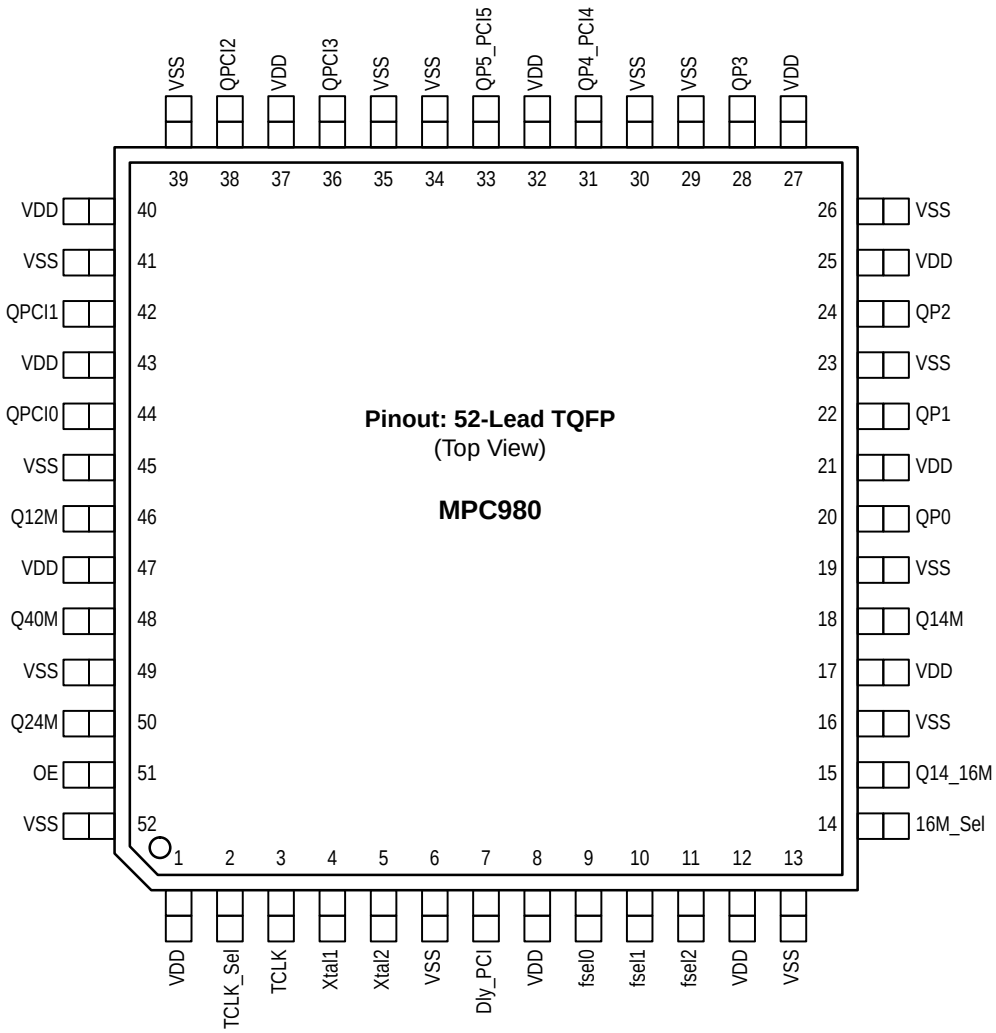
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM





Pinout: 52-Lead TQFP
(Top View)

MPC980

FUNCTION TABLE 1

OE	fsel0	fsel1	PCLK	PCICLK	Q14M	Q16M	Q24M	Q12M	Q40M
0	X	X	High Impedance	High Impedance	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z
1	0	0	50MHz	25MHz	14.31818	16	24	12	40
1	0	1	60MHz	30MHz	14.31818	16	24	12	40
1	1	0	66MHz	33MHz	14.31818	16	24	12	40
1	1	1	TCLK/2	TCLK/4	TCLK	TCLK/6	TCLK/4	TCLK/8	TCLK/2

FUNCTION TABLE 2

Dly_PCI	QP/QPCI Relationship
0	Synchronous Processor & PCI Clocks
1	PCI Clocks Lag Processor Clocks

FUNCTION TABLE 3

fsel2	QP/QPCI Output Configuration
0	6 Processor and 4 PCI Clocks
1	4 Processor and 6 PCI Clocks

FUNCTION TABLE 4

TCLK_Sel	PLL Input Reference
0	Crystal Oscillator
1	TCLK

DC CHARACTERISTICS (T_A = 0° to 70°C)

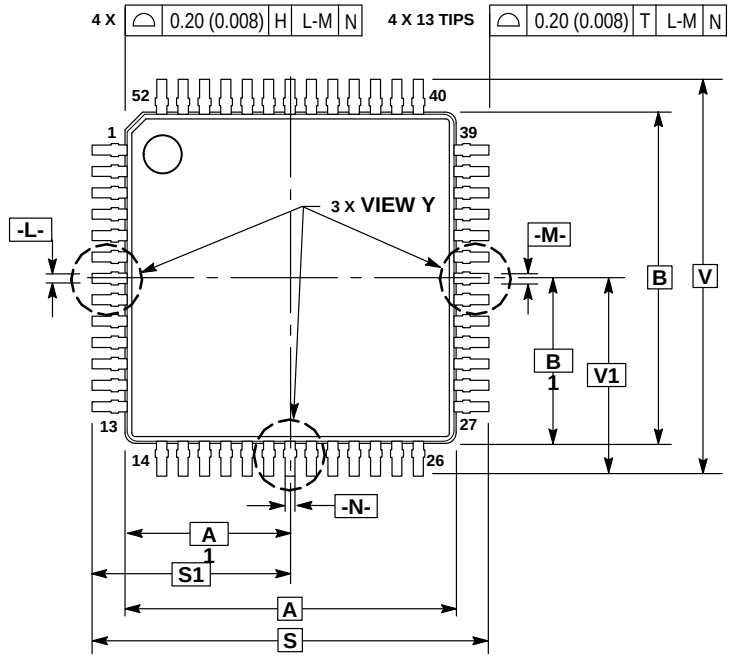
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{DD}	Power Supply Voltage	3.0		3.8	V	
V_{IL}	Input LOW Voltage			$0.3V_{DD}$	V	
V_{IH}	Input HIGH Voltage	$0.7V_{DD}$		V_{DD}	V	
V_{OH}	Output HIGH Voltage	V_{DD} –0.4			V	
V_{OL}	Output LOW Voltage			0.4	V	
C_{IN}	Input Capacitance			4.5	pF	

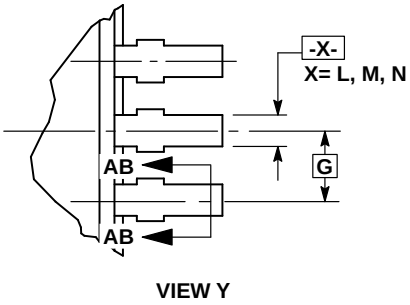
AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{Xtal}	Input Crystal Frequency		14.31818		MHz	
f_{max}	Maximum Output Frequency QP QPCI			66 33	MHz	
t_{dc}	Output Duty Cycle		$t_{CYCLE}/2$ ±500		ps	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±150	ps	
t_{skew}	Output–to–Output Skew QP to QP QPCI to QPCI QP to QPCI			350 350 500	ps	
t_{delay}	Time Delay QP to QPCI		$\frac{1}{8f_{QP}}$			
t_r, t_f	Output Rise/Fall Time			0.8	ns	1.0 to 1.8V
t_{LOCK}	PLL Lock Time			10	ms	
t_{PZL}, t_{PZH}	Output Enable Time		TBD			
t_{PLZ}, t_{PHZ}	Output Disable Time		TBD			

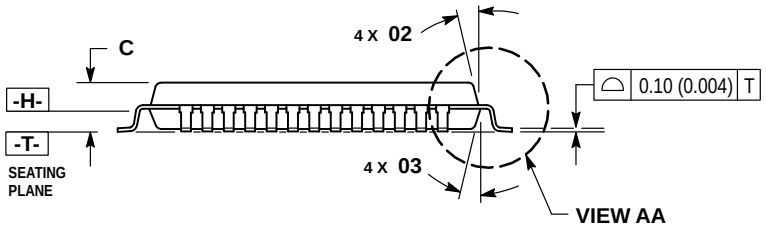
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D-02
ISSUE A





VIEW Y



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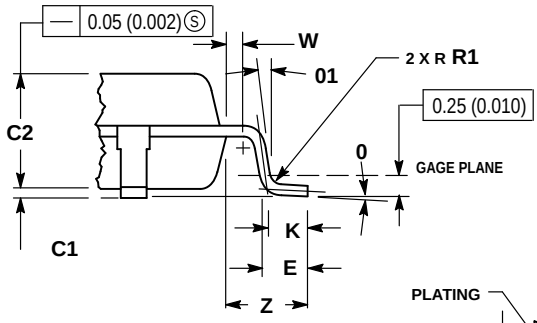

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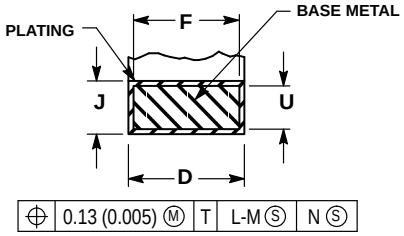

SECTION AB-AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.007 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.60	—	0.063
C1	0.05	0.15	0.002	0.006
C2	1.35	1.45	0.053	0.057
D	0.22	0.38	0.009	0.015
E	0.45	0.75	0.018	0.030
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
K	0.50 REF		0.020 REF	
R1	0.10	0.20	0.004	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
0	0°	7°	0°	7°
01	0°	—	0°	—
02	12° REF		12° REF	
03	5°	13°	5°	13°

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