Advance Information

3.3/5.0V PLL Clock Driver

MPC974

LOW VOLTAGE PLL CLOCK DRIVER

The MPC974 is a fully integrated PLL based clock generator and clock distribution chip which can operate from either a 3.3V or a 5.0V supply. The MPC974 is ideally suited for high speed, timing critical designs which need a high level of clock fanout. The device features 15 high drive CMOS (or LVCMOS) outputs, each output has the capability of driving a 50Ω parallel terminated transmission line or two 50Ω series terminated transmission lines on the incident edge.

- Fully Integrated PLL
- Two Reference Clock Inputs for Redundant Clock Applications
- Tristatable Outputs
- Logic Enable on the Outputs
- Specified for Both 3.3V and 5.0V V_{CC}
- Output Frequency Configurable
- TQFP Packaging
- ±100ps Typical Cycle–Cycle Jitter

52 1

FA SUFFIX
TQFP PACKAGE
CASE 848D-03

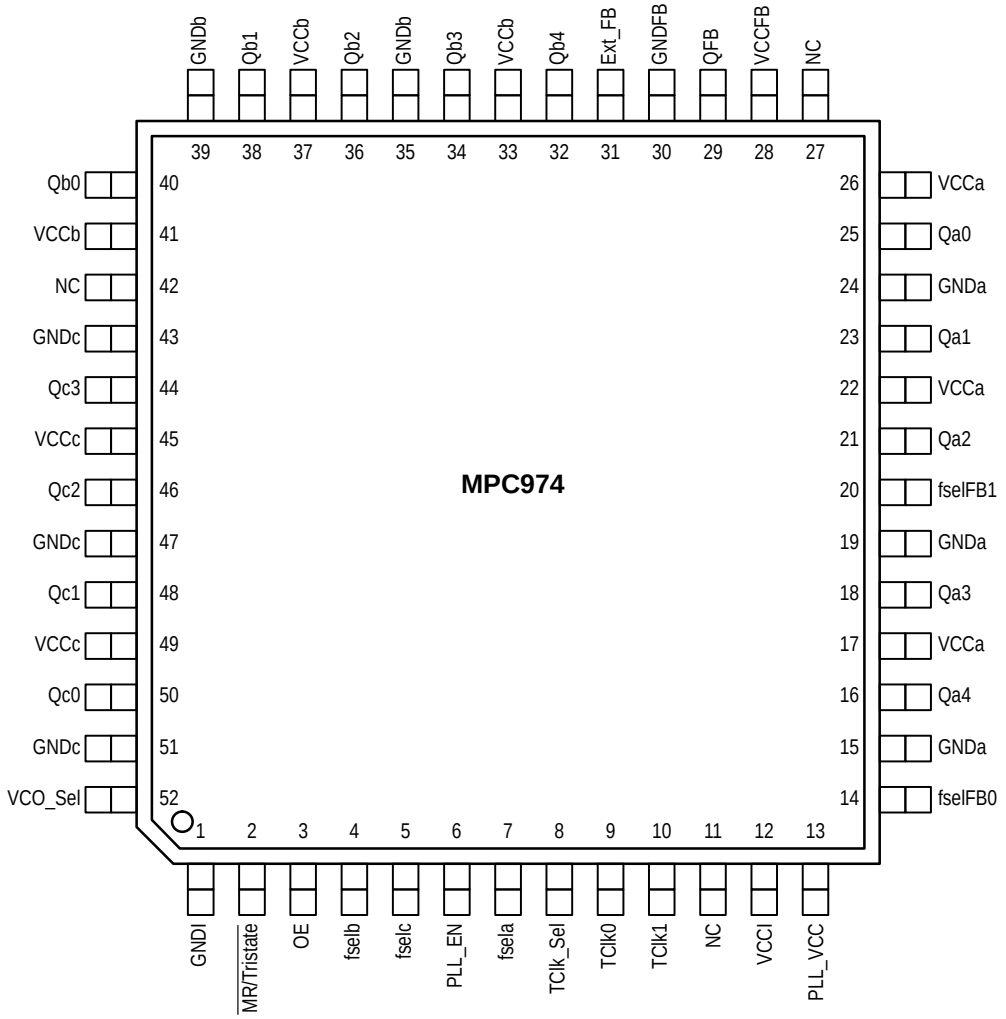
The MPC974 features 3 individually frequency programmable banks of outputs. The frequency programmability offers the capability of establishing output frequency relationships of 1:1, 2:1, 3:1, 3:2 and 3:2:1. In addition, the device features a separate feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_Sel pin provides an extended VCO lock range for added flexibility and general purpose usage.

The TCLK0 and TCLK1 inputs provide a method for dynamically switching the PLL between two different clock sources. The PLL has been optimized to provide small deviations in output pulse width and well controlled, slow transition back to lock when the inputs are switch between two references that are equal in frequency but out of phase with each other. This feature makes the MPC974 an ideal solution for fault tolerant applications which require redundant clock sources.

All of the control pins are TTL level (or LVCMOS/LVTTL if a 3.3V V_{CC} is used) inputs. The Fsel pins control the VCO divide ratios that are applied to the various output banks and the feedback output. The $\overline{\text{MR}}$/$\overline{\text{Tristate}}$ input will reset the internal flip flops and tristate the outputs when driven LOW. The OE pin will force all of the outputs except the feedback output LOW to allow for acquiring phase lock prior to providing clocks to the rest of the system. The PLL_En pin allows the PLL to be bypassed for board level functional test. When bypassed the signal on the selected TCLK will be routed around the PLL and will drive the internal dividers directly.

The MPC974 is packaged in the 52–lead TQFP package to provide optimum electrical performance as well as minimize board space requirements. The device is specified for both 3.3V and 5.0V V_{CC}'s. Note that there may be thermal issues to consider under some configurations and output frequencies when the device is operated from a V_{CC} of 5.0V.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



FUNCTION TABLE 1

fsela	Qa	fselb	Qb	fselc	Qc
0	÷2	0	÷2	0	÷4
1	÷4	1	÷4	1	÷6

FUNCTION TABLE 2

fselFB1	fselFB0	QFB
0	0	÷4
0	1	÷8
1	0	÷6
1	1	÷12

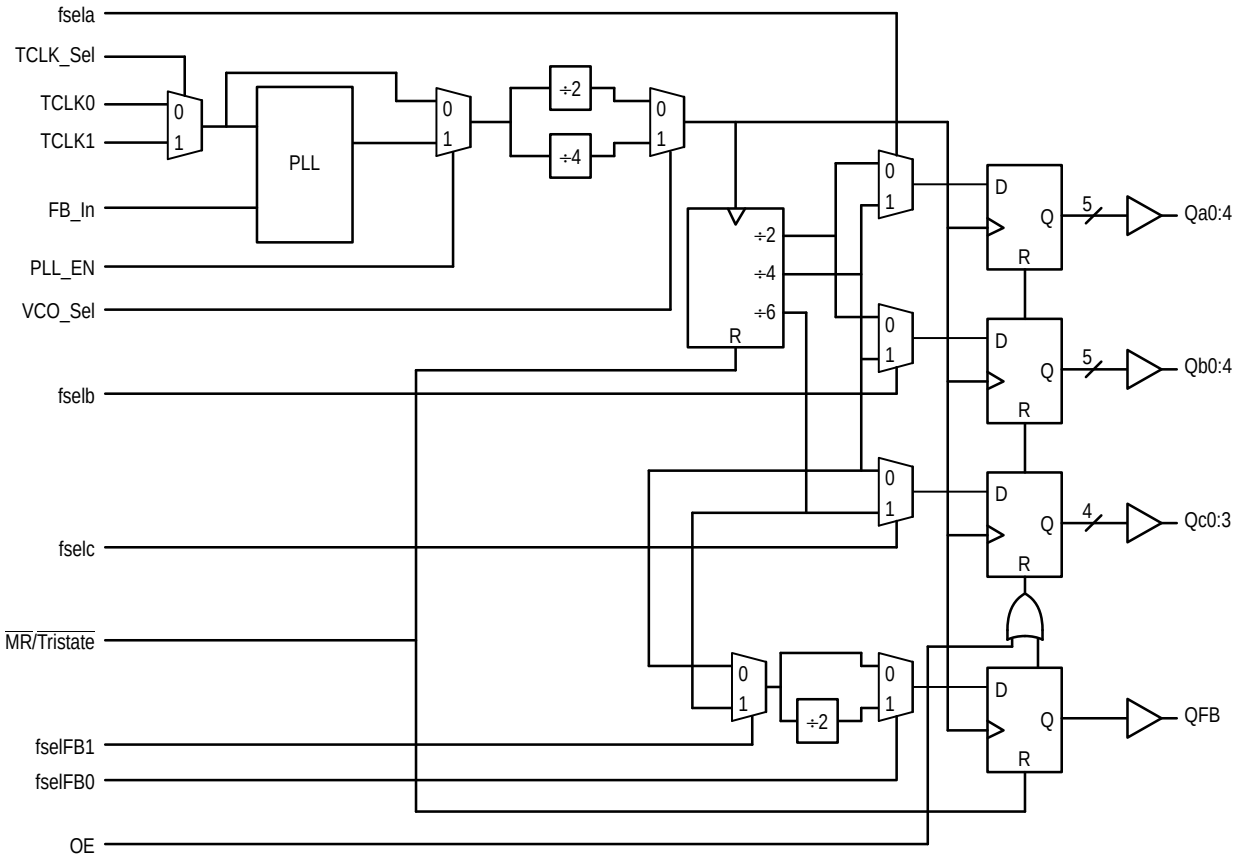
FUNCTION TABLE 3

VCO_Sel	fVCO
0	VCO/2
1	VCO/4

FUNCTION TABLE 4

Control Pin	Logic ‘0’	Logic ‘1’
$\overline{\text{MR}}$/Tristate	Master Reset/Output Tristate	Enable Outputs
PLL_EN	Bypass PLL	Enable PLL
TClk_Sel	TCLK0	TCLK1
OE	Qa, Qb, Qc Logic LOW	All Output Enabled

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	5.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		8	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V or 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA[1]
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA[1]
I_{IN}	Input Current			±100	µA	
I_{CC}	Maximum Quiescent Supply Current			120	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance			30	pF	Per Output

1. The MPC974 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have either pull–up or pull–down resistors which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	TBD	TBD	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V or 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.15		1.5	ns	0.8 to 2.0V
t_{pw}	Output Duty Cycle		$t_{CYCLE}/2$ ±500		ps	
f_{VCO}	PLL VCO Lock Range Feedback = VCO/8 Feedback = VCO/12 Feedback = VCO/16 Feedback = VCO/24 Feedback = VCO/32		200–500 200–500 200–500 200–500 200–500		MHz	
t_{pd}	SYNC to Feedback Propagation Delay Feedback = VCO/8 Feedback = VCO/12 Feedback = VCO/16 Feedback = VCO/24 Feedback = VCO/32	TBD	X_1±150 X_2±150 X_3±150 X_4±150 X_5±150	TBD	ps	Note 1
t_{os}	Output-to-Output Skew Same Frequency Different Frequency			350 500	ps	
f_{max}	Maximum Output Frequency Q (÷2) Q (÷4) Q (÷6)			100 67 45	MHz	VCO_Sel = 0
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

1. X_1, X_2, X_3, X_4, and X_5 all to be determined.

APPLICATIONS INFORMATION

Programming the MPC974

The MPC974 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input to output frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Function Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

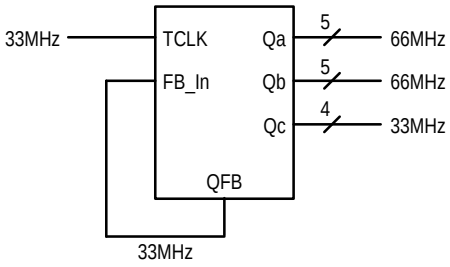
The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range is a function of the feedback divide ratios and can be found in the specification tables. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 10 and 100MHz the MPC974 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. The separate PLL feedback output allows for a wide range of output vs input frequency relationships. Function Table 1 can be used to identify the potential relationships available. Figure 1 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

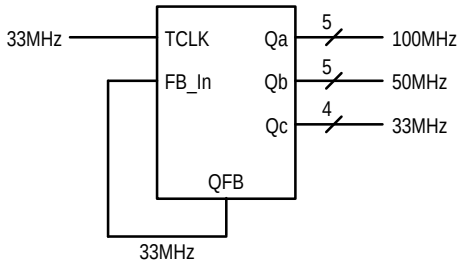
Using the MPC974 as a Zero Delay Buffer

The external feedback option of the MPC974 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is near zero. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The feedback divider affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a

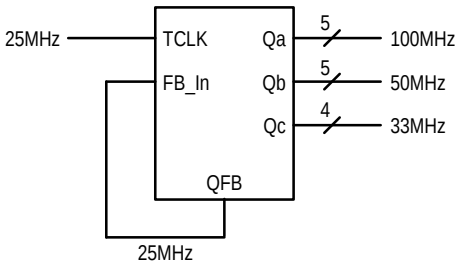
function of the feedback divisor the Tpd of the MPC974 is a function of the feedback configuration used. The Tpd of the device is specified in the specification tables.



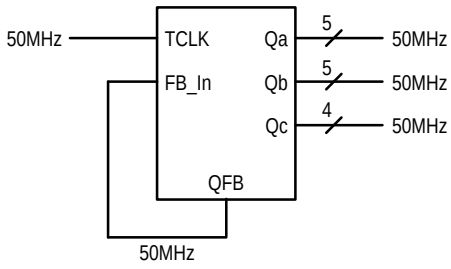
fsela	fselb	fselc	fselFB	VCO_Sel
0	0	0	00	0



fsela	fselb	fselc	fselFB	VCO_Sel
0	1	1	10	0



fsela	fselb	fselc	fselFB	VCO_Sel
0	1	1	01	0



fsela	fselb	fselc	fselFB	VCO_Sel
1	1	0	00	0

Figure 1. MPC974 Programming Schemes

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC974 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 850ps (300ps for Tpd variation plus 350ps output–to–output skew plus 200ps for jitter). For designs with multiple MPC974's that are configured differently one must account for the differences between the nominal delays of the multiple devices.

Driving Transmission Lines

The MPC974 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC974 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. NO TAG illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC974 clock driver is effectively doubled due to its capability to drive multiple lines.

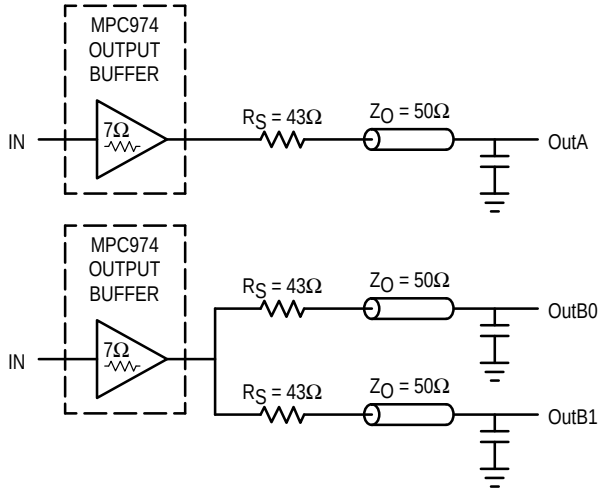


Figure 2. Single versus Dual Transmission Lines

The waveform plots of NO TAG show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC974 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC974. The output waveform in NO TAG shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

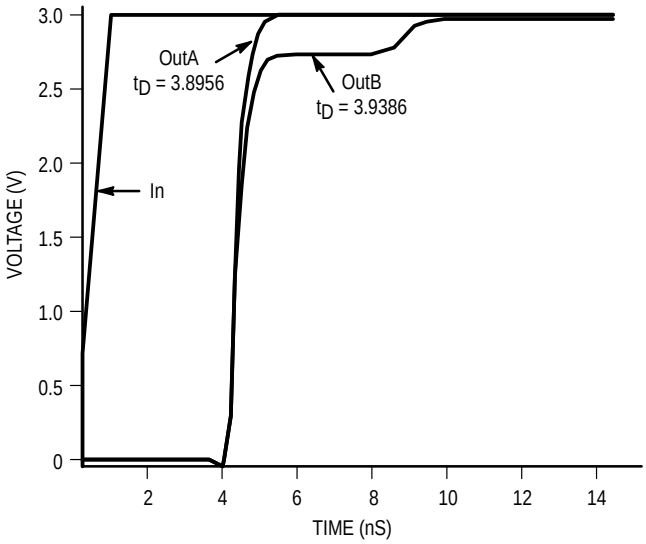
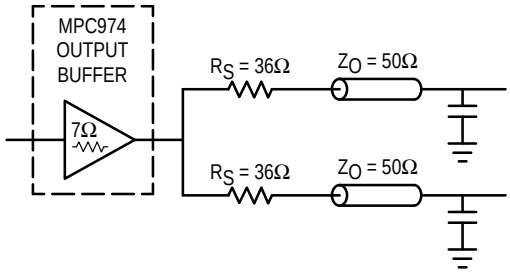


Figure 3. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in NO TAG should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



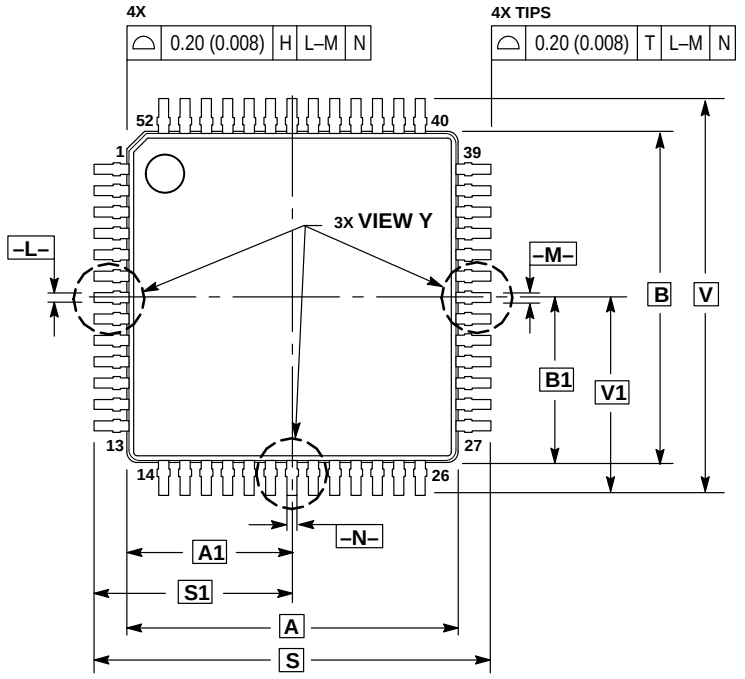
$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

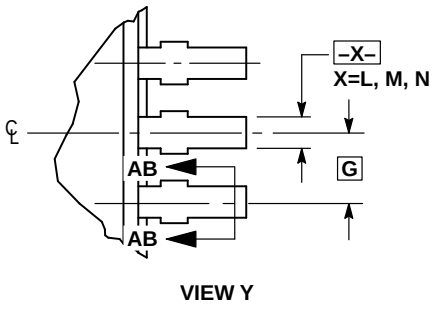
Figure 4. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

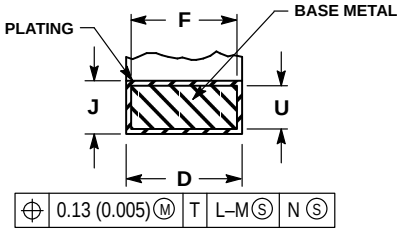
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D-03
ISSUE C

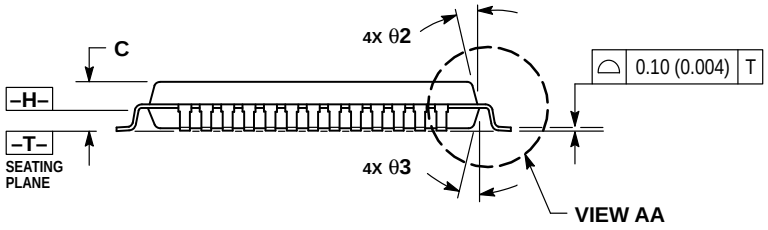


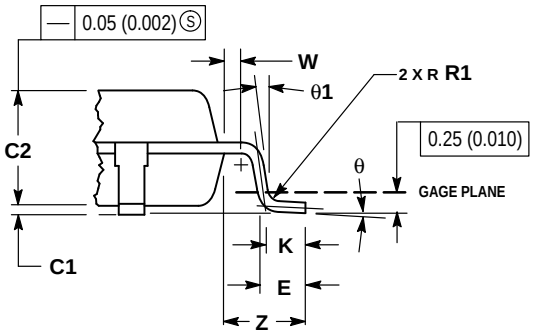


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

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