

## Low Voltage PLL Clock Driver

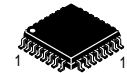
The MPC956 is a 3.3V PLL based clock driver designed explicitly to support the MPC601 and MPC601+ microprocessor. The device synthesizes all of the current and future MPC601 processor frequencies from a 33.33MHz crystal source. The three processor clocks lag the BCLK's by one VCO period to ease system integration. For system architectures which support an asynchronous PCI bus a buffered copy of the 33.33MHz is provided. This output can be fanout further via the MPC903 to provide the PCI bus clocks.

- Provide PowerPC™ 601 Clocks (66, 80 and 100 MHz)
- Support  $\div 2$ ,  $\div 3$  and  $\div 4$  Bus Modes
- Fully Integrated PLL
- Output Frequencies Synthesized from Single 33.33MHz Crystal
- Output Frequency Up to 200MHz
- Output–Output Skew 500ps
- Provides Asynchronous PCI Clock
- Power Management Features
- 3.3V VCC
- 32–Lead TQFP Packaging
- $\pm 150$ ps Cycle–to–Cycle PLL Jitter

The MPC956 provides a special power down mode for system power management. The scheme simplifies the design of a system which meets the Energy Star requirements. When asserted (driven to a logic HIGH) the Doze pin will seamlessly reduce all of the output frequencies of the chip. The reductions are implemented in a fashion to minimize power while keeping enough speed to not hamper the performance to the end user. Because the frequency reduction is timed internally there is no need to halt the system to implement the power down mode.

The 4 select pins choose among 14 possible output configurations. The configurations were chosen to represent the most common PowerPC 601 and PowerPC 601+ system applications. The outputs are synthesized from a 33.33MHz crystal, this crystal input is also buffered and provides an output for use with an asynchronous PCI bus.

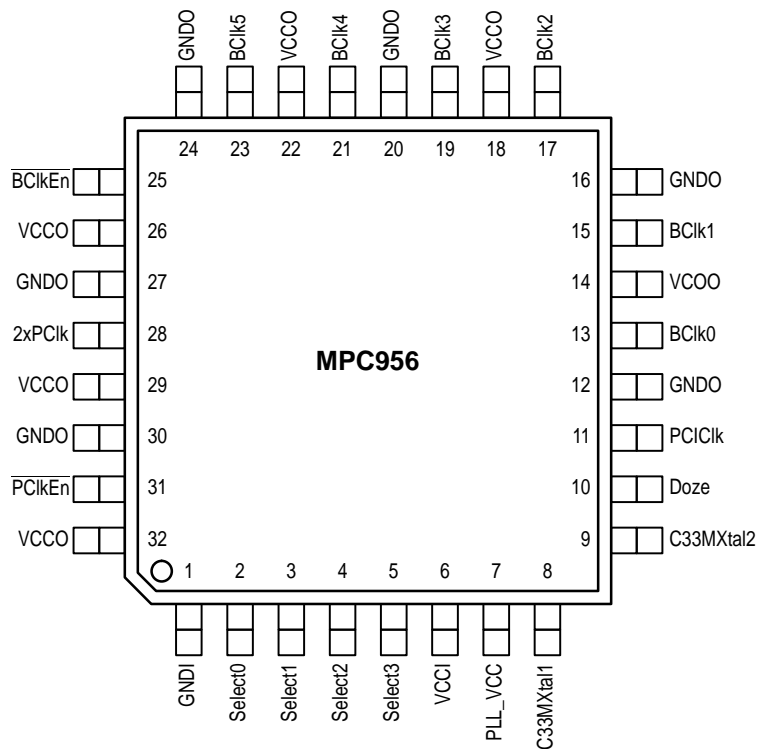
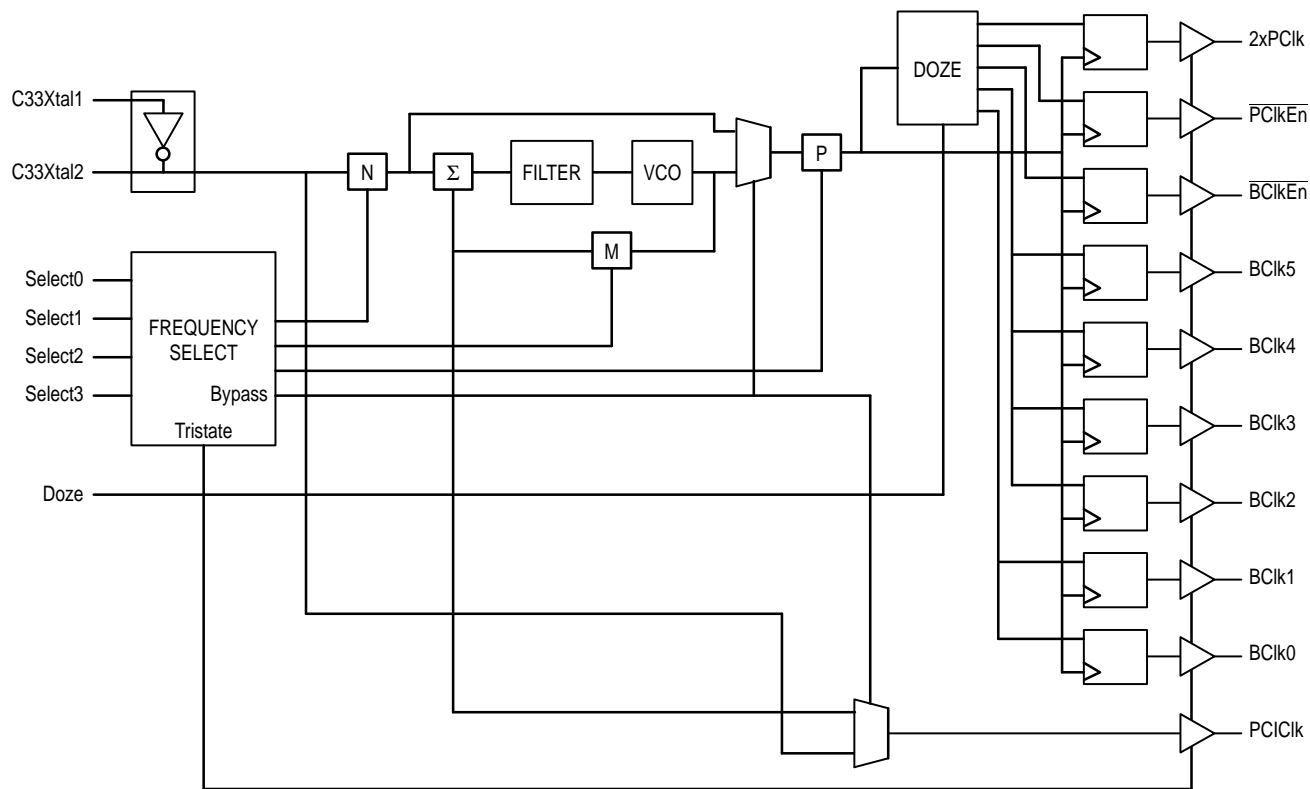
The MPC956 works from a 3.3V supply and is packaged in a 32 lead TQFP to optimize performance and board space requirements.

**MPC956****LOW VOLTAGE  
PLL CLOCK DRIVER****FA SUFFIX**  
TQFP PACKAGE  
CASE 873-01

PowerPC is a trademark of International Business Machines Corporation.



MPC956 LOGIC DIAGRAM



## MPC956 OUTPUT FREQUENCIES

Select	2xPClk	2xPClk, Doze	PClkEn	BCLKEn, BCLKn	PClkEn,BCLKEn, BCLKn, Doze
0	133.33	33.33	66.66	33.33	16.66
1	160	40	80	40	20
2	160	40	80	26.67	20
3	200	50	100	50	25
4	200	50	100	33.33	25
5	240	60	120	60	30
6	240	60	120	40	30
7	240	60	120	30	30
8	266.66	66.66	133.33	66.67	33.33
9	266.66	66.66	133.33	44.44	33.33
10	266.66	66.66	133.33	33.33	33.33
11	300	75	150	75	37.50
12	300	75	150	50	37.50
13	300	75	150	37.50	37.50

\*Current product only specified for 2xPClk of  $\leq 200$  MHz.

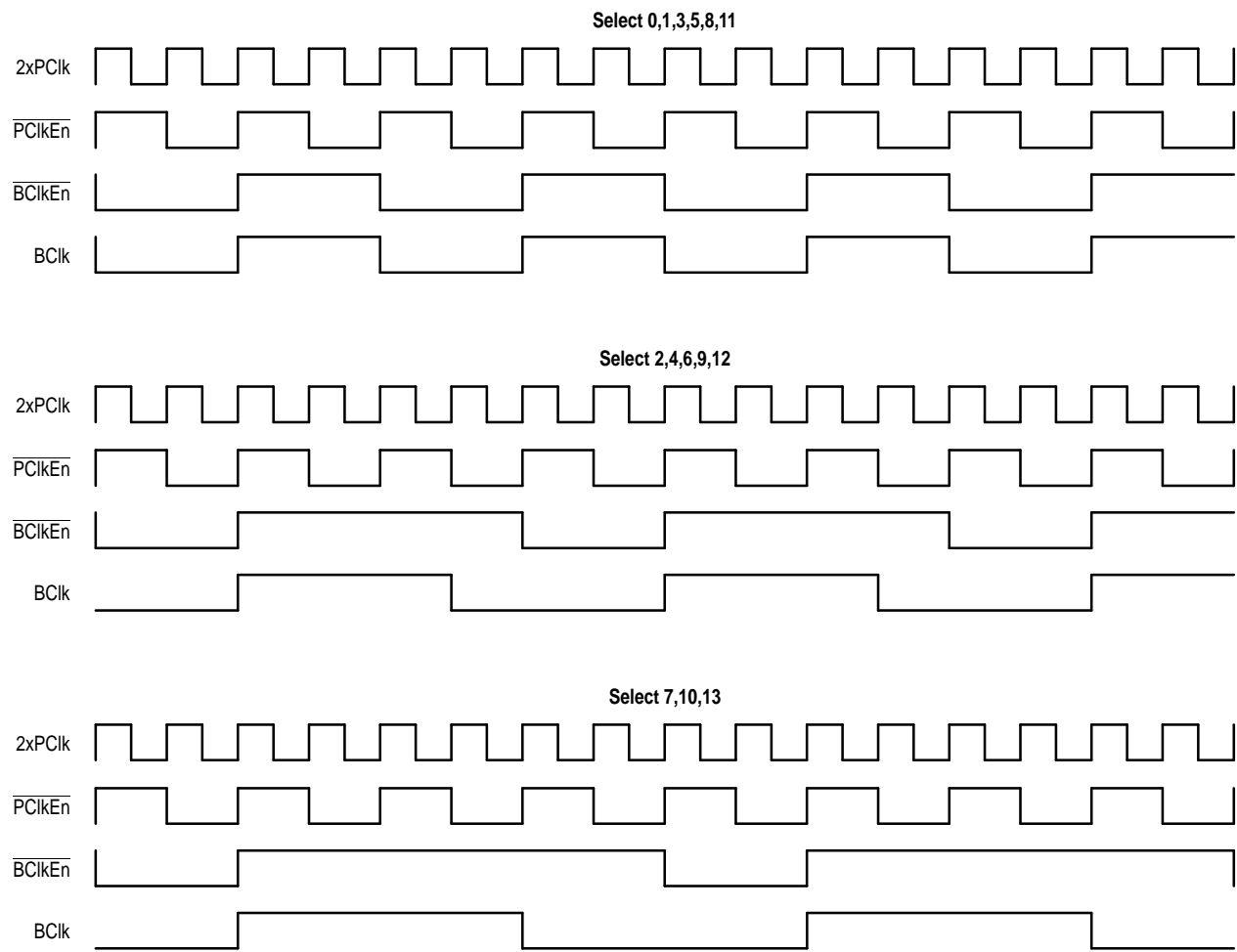
DC CHARACTERISTICS ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$V_{DD}$	Power Supply Voltage	3.0		3.8	V	
$V_{IL}$	Input LOW Voltage			$0.3V_{DD}$	V	
$V_{IH}$	Input HIGH Voltage	$0.7V_{DD}$		$V_{DD}$	V	
$V_{OH}$	Output HIGH Voltage	$V_{DD} - 0.4$			V	
$V_{OL}$	Output LOW Voltage			0.4	V	
$C_{IN}$	Input Capacitance			4.5	pF	

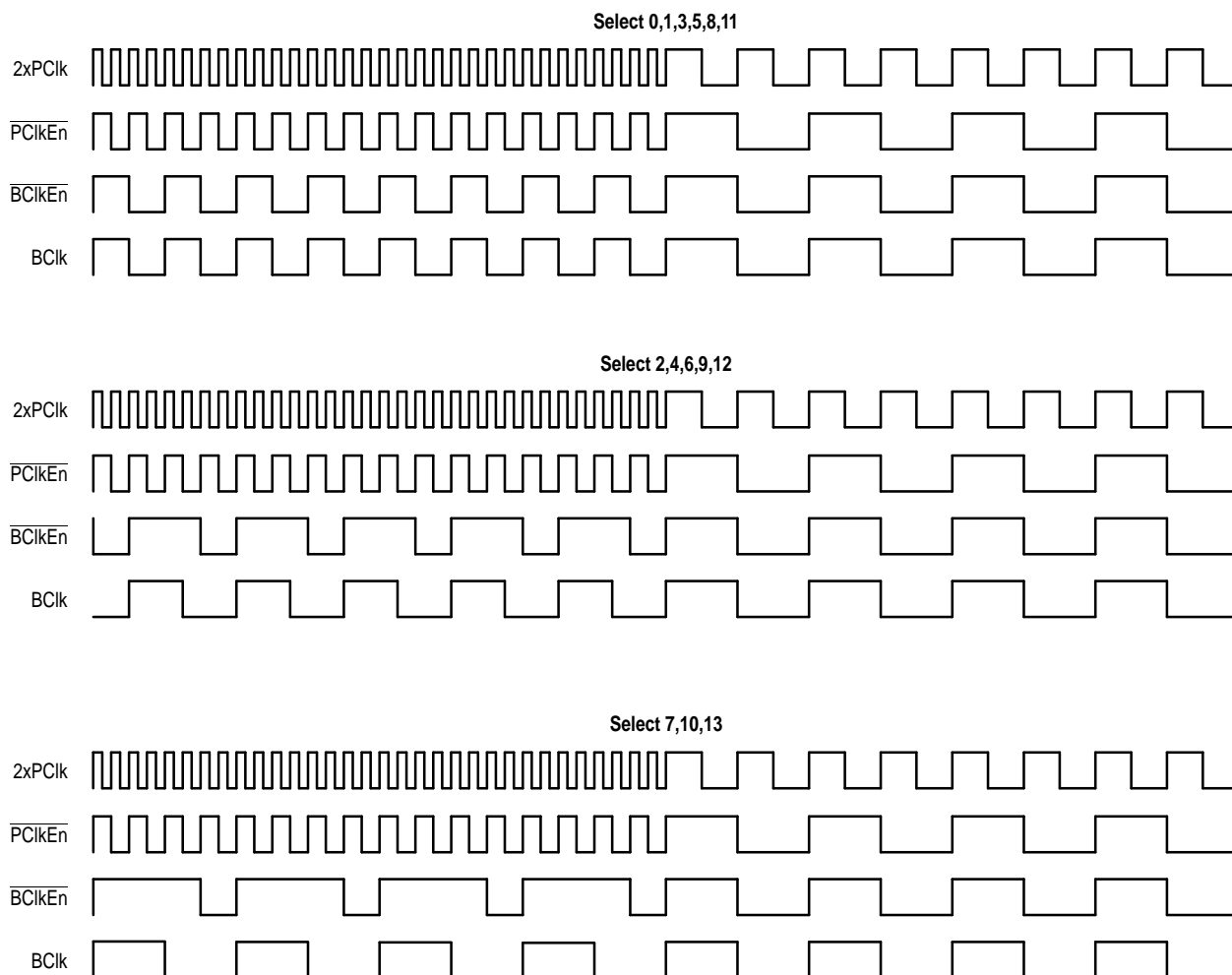
AC CHARACTERISTICS ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$f_{Xtal}$	Input Crystal Frequency	20		40	MHz	
$f_{max}$	Maximum Output Frequency 2xPCLK PCLKEN BCLK			200 100 50	MHz	1.4V, $Z_0 = 50\Omega$
$t_{dc}$	Output Duty Cycle 2xPCLK Other	35 45		65 55	%	1.4V, $Z_0 = 50\Omega$
$t_{jitter}$	PLL Cycle-to-Cycle Jitter (Peak-to-Peak)			$\pm 150$	ps	Note 2
$t_{skew}$	Output-to-Output Skew BLCK 2xPCLK, PCLKEN, BCLKEN		300 300	500 500	ps	1.4V, $Z_0 = 50\Omega$
$t_{per}$	Minimum Output Period 2xPCLK	4.85			ns	$F_{out2xP} = 200\text{MHz}$
$t_{pw}$	2xPCLK Pulse Width	1.75			ns	$F_{out2xP} = 200\text{MHz}$
$t_{pskew}$	BCLK to 2xPCLK Skew	$1/f_{VCO}$ -900		$1/f_{VCO}$	ps	$F_{out2xP} \leq 200\text{MHz}$
$t_{delay}$	Time Delay 2xPCLK to BCLKEN	50		550	ps	Note 1, 1.4V, $Z_0 = 50\Omega$
$t_r, t_f$	Output Rise/Fall Time			0.8	ns	1.0 to 1.8V, 1.4V, $Z_0 = 50\Omega$
$t_{LOCK}$	PLL Lock Time			10	ms	
$t_{PZL}, t_{PZH}$	Output Enable Time			20	ns	
$t_{PLZ}, t_{PHZ}$	Output Disable Time			20	ns	

1. Guaranteed to meet setup/hold times for the PowerPC™ 601 processor.
2. Guaranteed but not tested.



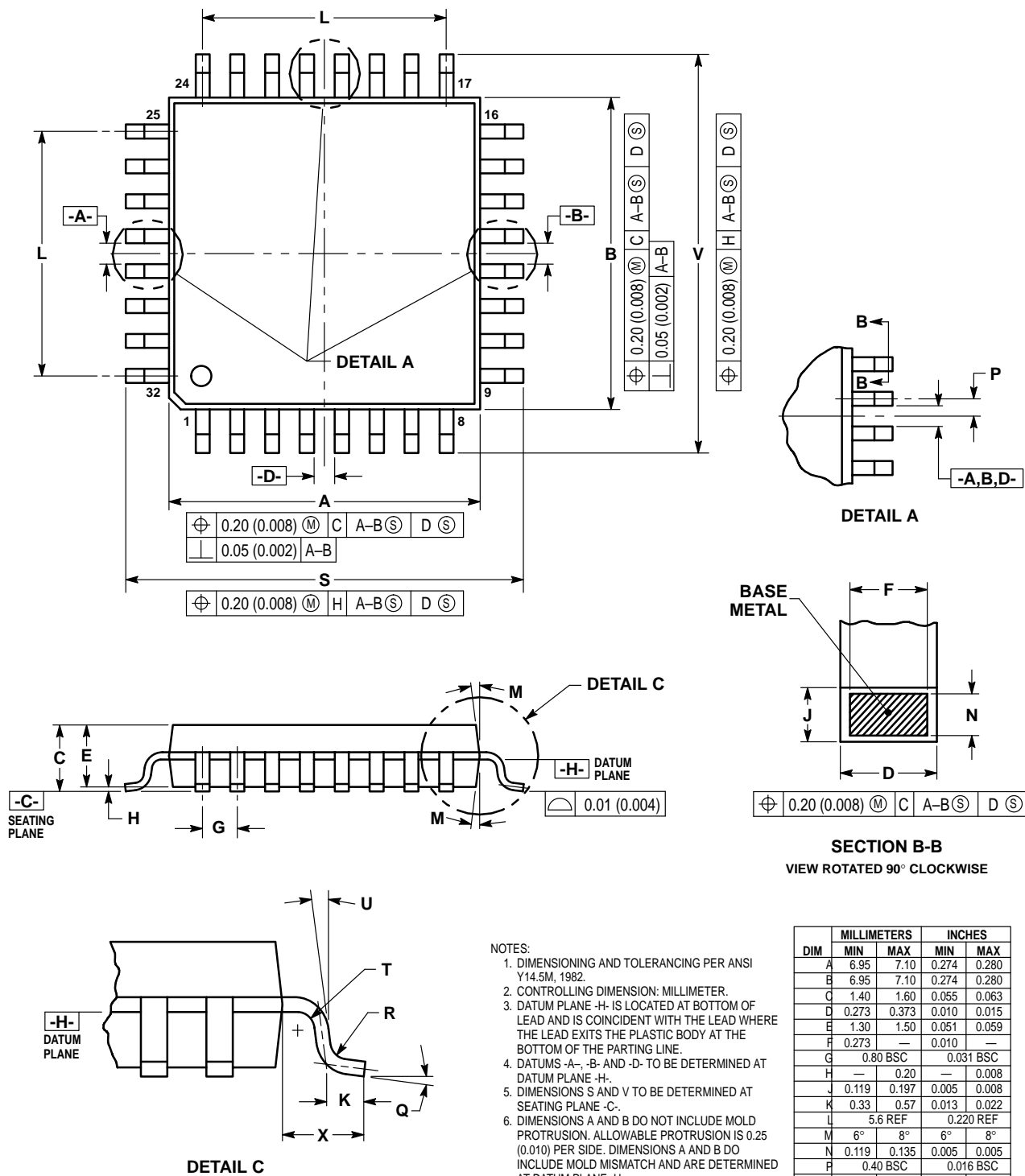
**Figure 1. Timing Diagrams for Select Options**  
(For clarity, processor clock lag not shown)



**Figure 2. Timing Diagrams for Doze Mode Transitions**  
 (For clarity, processor clock lag not shown)

## OUTLINE DIMENSIONS


FA SUFFIX  
TQFP PACKAGE  
CASE 873-01  
ISSUE A



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC	—	0.031 BSC	—
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF	—	0.220 REF	—
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC	—	0.016 BSC	—
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF	—	0.039 REF	—

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**How to reach us:**

**USA/EUROPE:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

**MFAX:** RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609  
**INTERNET:** <http://Design-NET.com>

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,  
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**HONG KONG:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



◇ CODELINE

MPC956/D

