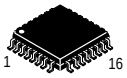
Product Preview

Low Voltage PLL Clock Driver

MPC955

LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
TQFP PACKAGE
CASE 873-01

The MPC955 is a 3.3V PLL based clock driver designed explicitly to support the MPC601 and MPC601+ microprocessor. The device synthesizes all of the current and future MPC601 processor frequencies from a 33.33MHz crystal source. For system architectures which support an asynchronous PCI bus a buffered copy of the 33.33MHz is provided. This output can be fanout further via the MPC903 to provide the PCI bus clocks.

- Provide PowerPC™ 601 Clocks (66, 80, 100, 120 133 and 150 MHz)
- Support ÷2, ÷3 and ÷4 Bus Modes
- Fully Integrated PLL
- Output Frequencies Synthesized from Single 33.33MHz Crystal
- Output Frequency Up to 300MHz
- Output–Output Skew 500ps
- Provides Asynchronous PCI Clock
- Power Management Features
- 3.3V V_{CC}
- 32–Lead TQFP Packaging
- ±150ps Cycle–to–Cycle Jitter

The MPC955 provides a special power down mode for system power management. The scheme simplifies the design of a system which meets the Energy Star requirements. When asserted the Doze pin will seemlessly reduce all of the output frequencies of the chip. The reductions are implemented in a fashion to minimize power while keeping enough speed to not hamper the performance to the end user. Because the frequency reduction is timed internally there is no need to halt the system to implement the power down mode.

The 4 select pins choose among 14 possible ouput configurations. The configurations were chosen to represent the most common PowerPC 601 and PowerPC 601+ system applications. The outputs are synthesized from a 33.33MHz crystal, this crystal input is also buffered and provided a an output for use with an aynchronous PCI bus. A Doze_PCI input is provided to seemlessly reduce the PCI bus frequency in half.

The MPC955 works from a 3.3V supply and is packaged in a 32 lead TQFP to optimize performance and board space requirements.

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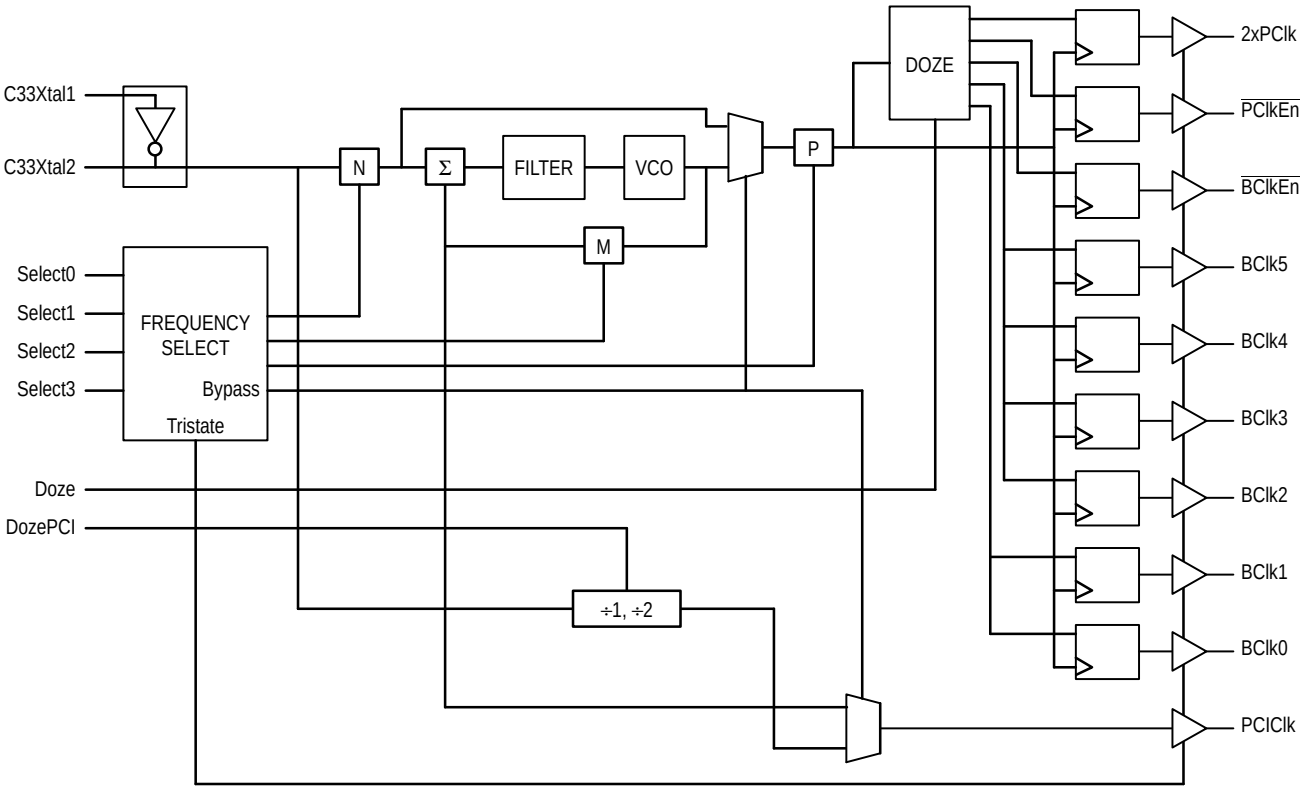
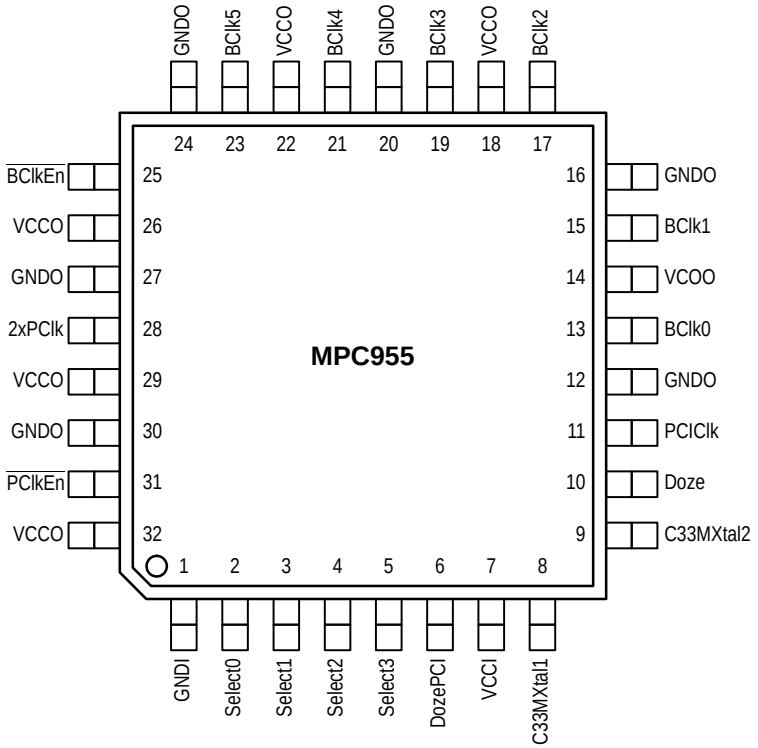
MPC955 LOGIC DIAGRAM





MPC955 OUTPUT FREQUENCIES

Select	2xPClk	2xPClk, Doze	$\overline{\text{PClkEn}}$	$\overline{\text{BClkEn}}$, BClkn	$\overline{\text{PClkEn}}$, $\overline{\text{BClkEn}}$, BClkn, Doze
0	133.33	33.33	66.66	33.33	16.66
1	160	40	80	40	20
2	160	40	80	26.67	20
3	200	50	100	50	25
4	200	50	100	33.33	25
5	240	60	120	60	30
6	240	60	120	40	30
7	240	60	120	30	30
8	266.66	66.66	133.33	66.67	33.33
9	266.66	66.66	133.33	44.44	33.33
10	266.66	66.66	133.33	33.33	33.33
11	300	75	150	75	37.50
12	300	75	150	50	37.50
13	300	75	150	37.50	37.50

DC CHARACTERISTICS (T_A = 0° to 70°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{DD}	Power Supply Voltage	3.0		3.8	V	
V_{IL}	Input LOW Voltage			$0.3V_{DD}$	V	
V_{IH}	Input HIGH Voltage	$0.7V_{DD}$		V_{DD}	V	
V_{OH}	Output HIGH Voltage	V_{DD} –0.4			V	
V_{OL}	Output LOW Voltage			0.4	V	
C_{IN}	Input Capacitance			4.5	pF	

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
f_{Xtal}	Input Crystal Frequency		33		34	MHz	
f_{max}	Maximum Output Frequency	2xPLCK $\overline{\text{PCLKEN}}$ BCLK			300 150 75	MHz	
t_{dc}	Output Duty Cycle	2xPCLK Other	35 45		65 55	%	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)				±150	ps	
t_{skew}	Output–to–Output Skew				350	ps	
t_{delay}	Time Delay	2xPCLK to $\overline{\text{BCLKEN}}$	300		600	ps	Note 1
t_r, t_f	Output Rise/Fall Time				0.8	ns	1.0 to 1.8V
t_{LOCK}	PLL Lock Time				10	ms	
t_{PZL}, t_{PZH}	Output Enable Time			TBD			
t_{PLZ}, t_{PHZ}	Output Disable Time			TBD			

1. Guaranteed to meet setup/hold times for the PowerPC™ 601 processor.

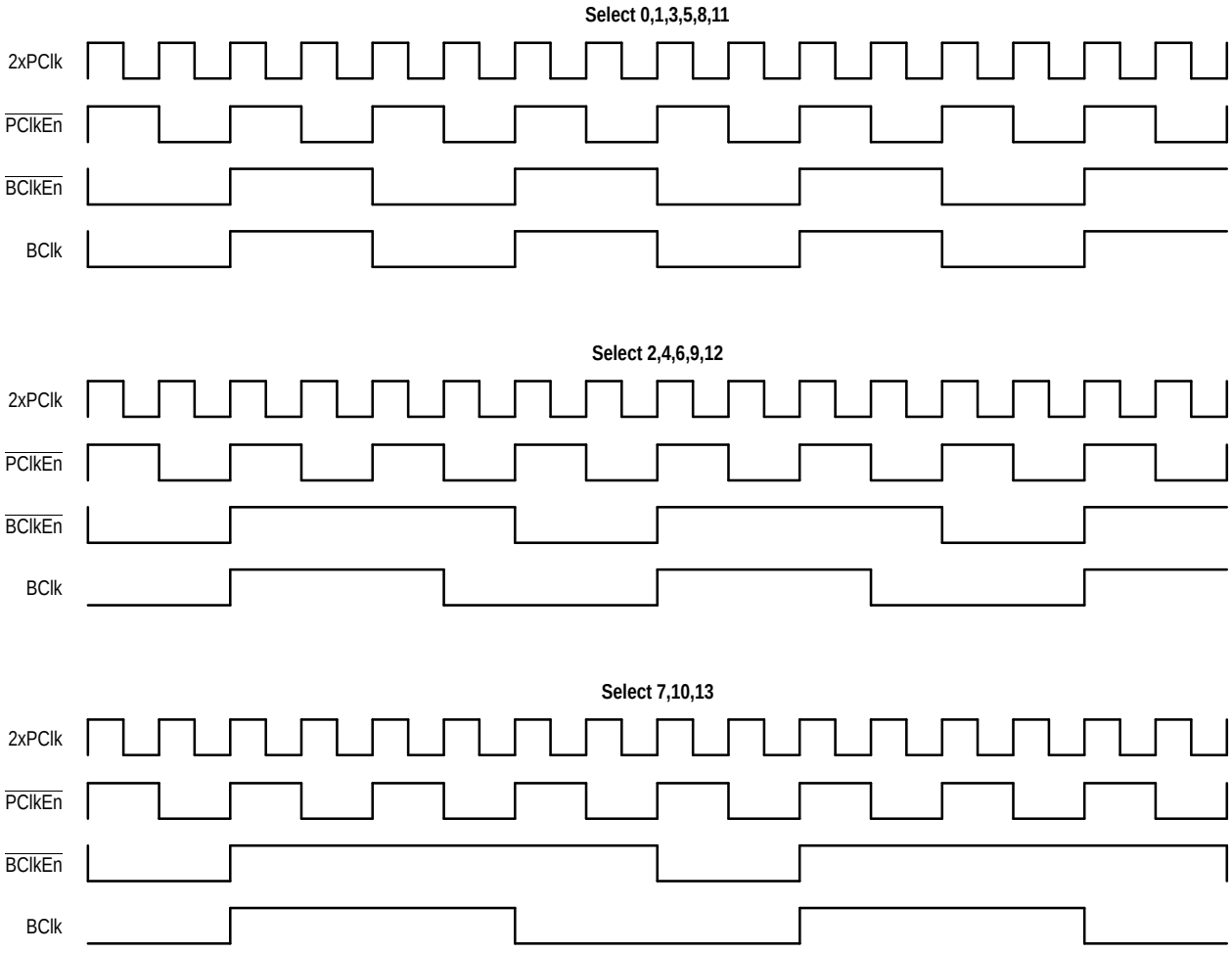


Figure 1. Timing Diagrams for Select Options

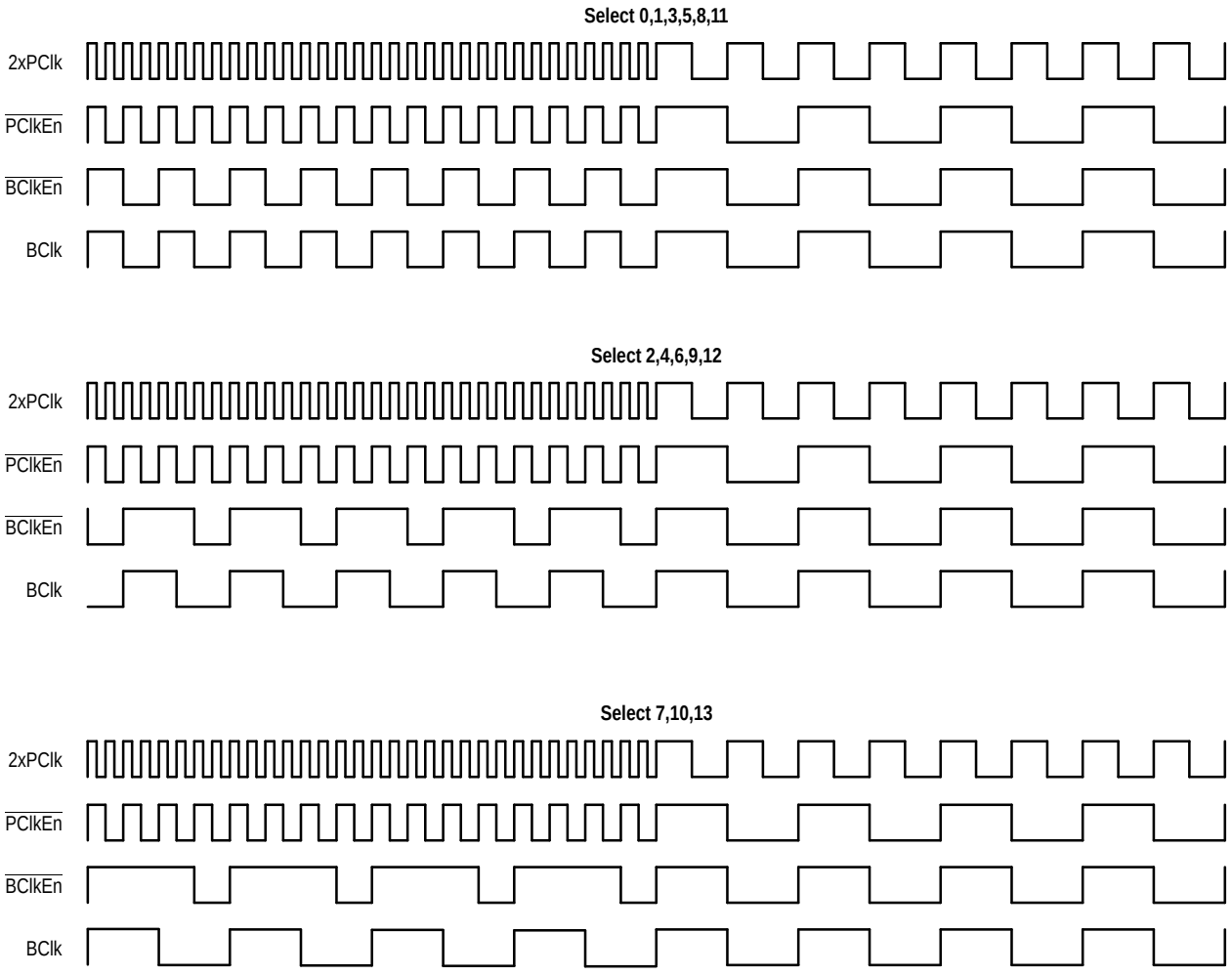
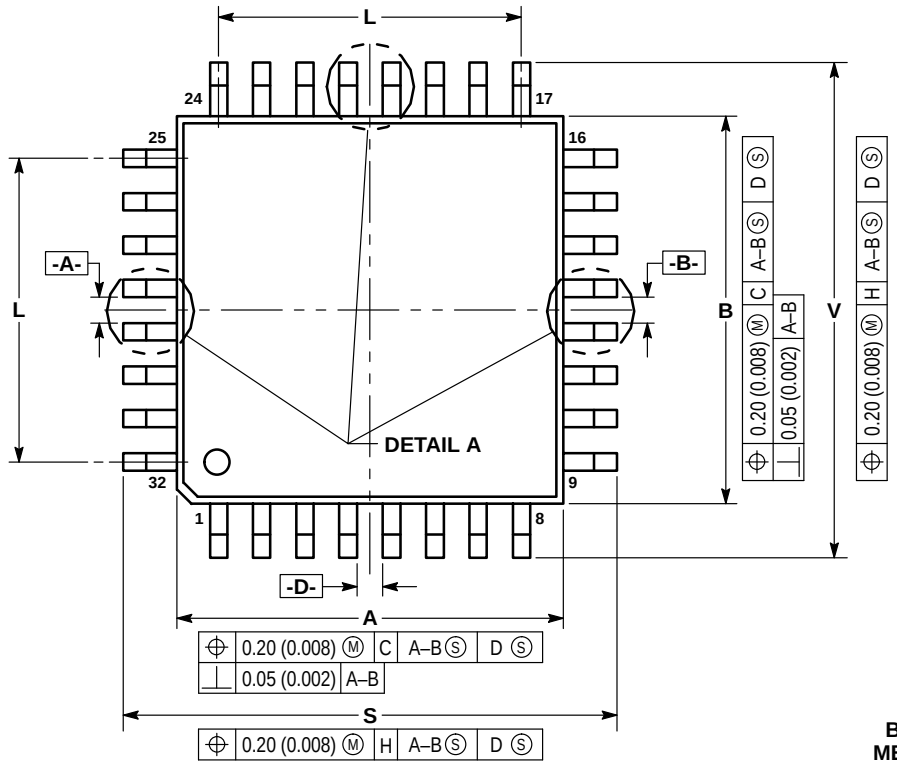
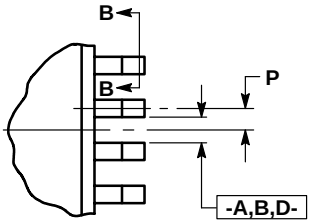


Figure 2. Timing Diagrams for Doze Mode Transitions

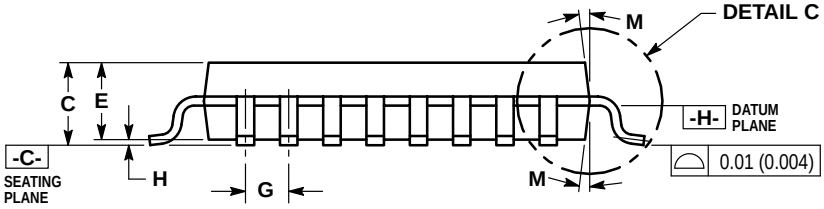
OUTLINE DIMENSIONS

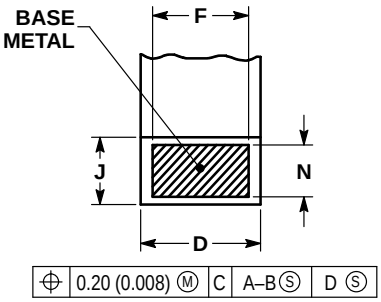
FA SUFFIX
TQFP PACKAGE
CASE 873-01
ISSUE A



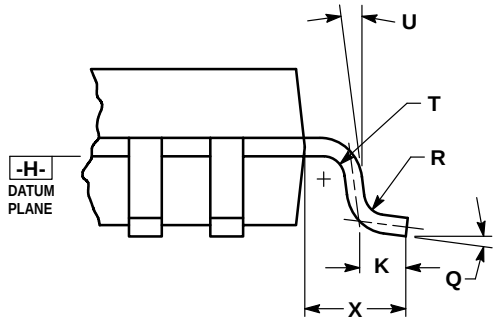


DETAIL A





SECTION B-B
VIEW ROTATED 90° CLOCKWISE



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A–, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

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