Product Preview

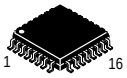
Low Voltage PLL Clock Driver

MPC952

LOW VOLTAGE PLL CLOCK DRIVER

The MPC952 is a 3.3V compatible, PLL based clock driver device targeted for desktop PC and Workstation applications. The device features a fully integrated PLL with no external components required. With output frequencies of up to 200MHz and eleven low skew outputs the MPC952 is well suited for many of today's maicroproceesor designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance. Jitter is an increasingly important parameter as more microprocessors and ASiC's are employing on chip PLL clock distribution.

- Fully Integrated PLL
- Output Frequency up to 200MHz
- Tri–statable Outputs
- Compatible with PowerPC™ and Intel Microprocessors
- Output Frequency Configurable
- TQFP Packaging
- ±50ps Cycle–to–Cycle Jitter



FA SUFFIX
TQFP PACKAGE
CASE 873-01

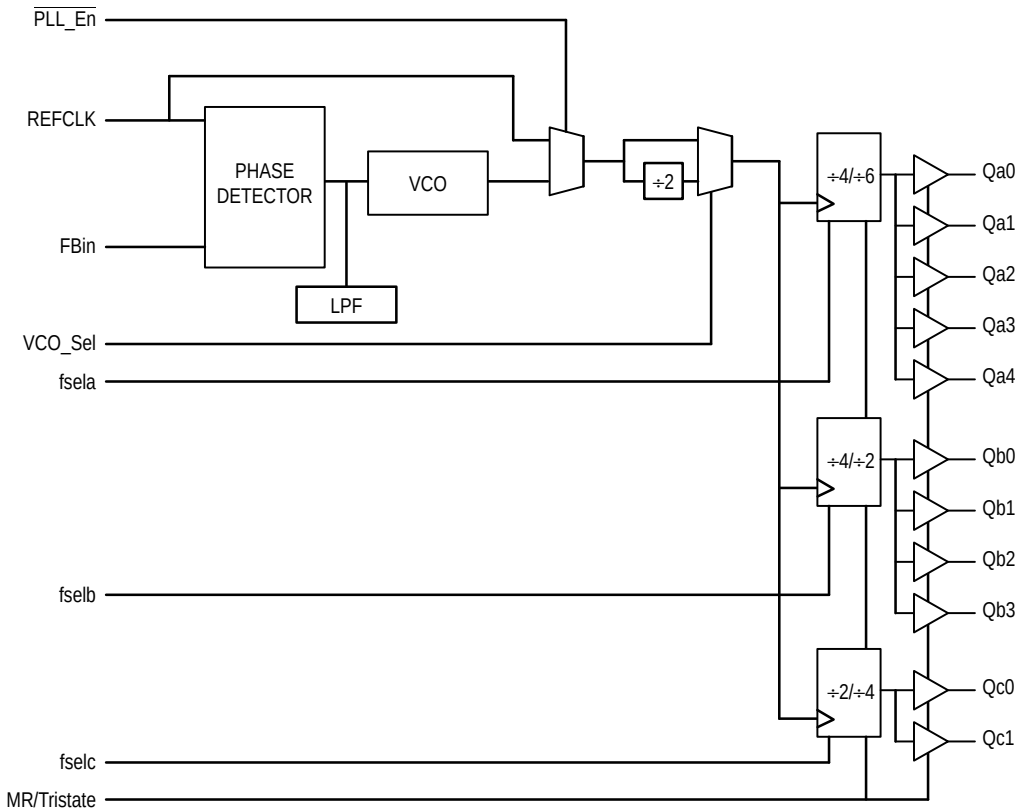
The MPC952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1 and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins as well as the other inputs are LVCMOS/LVTTL compatible inputs.

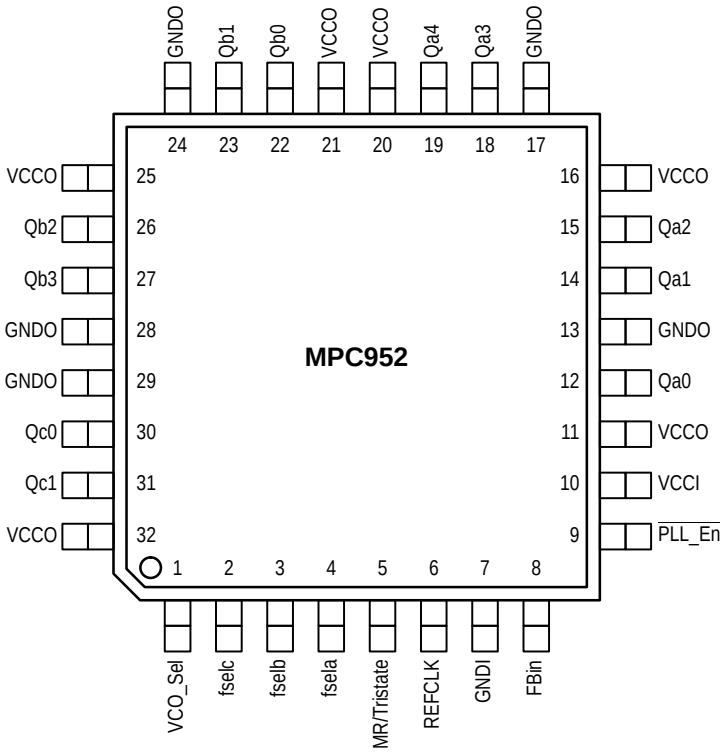
The MPC952 uses external feedback to the PLL. This features allows for the use of the device as a "zero" delay buffer. Any of the eleven outputs can be used as the feedback to the PLL. The VCO_Sel pin allows for the choice of two VCO ranges to optimize PLL stability and jitter performance. The MR/Tristate pins allows the user to force the outputs into high impedance for board level test.

For System debug the PLL of the MPC952 can be bypassed. The when force to a logic HIGH the PLLEN input will route the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The outputs of the MPC952 are LVCMOS outputs. The outputs are optimally designed to drive terminated transmission lines. For applications using series terminated transmission lines each MPC952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most desktop designs. For more information on driving transmission lines consult the applications section of this data sheet.

MPC952 LOGIC DIAGRAM





FUNCTION TABLES

fsela	Qna	fselb	Qnb	fselc	Qnc
0 1	÷4 ÷6	0 1	÷4 ÷2	0 1	÷2 ÷4

Control Pin	Logic ‘0’	Logic ‘1’
VCO_Sel	fVCO	fVCO/2
MR/Tristate	Output Enable	Tristate
$\overline{\text{PLL\_En}}$	Enable PLL	Disable PLL

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current	TBD	TBD	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA**1**
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA**1**
I_{IN}	Input Current			±100	µA	Note 2
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance				pF	
I_{CC}	Maximum Quiescent Supply Current			TBD	mA	

1 The MPC948 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).

2 Inputs have pull–up resistors which affect input current, $\overline{\text{PECL\_CLK}}$ has a pull–down resistor.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 1	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1 Maximum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time		0.20		1.0	ns	0.8 to 2.0V
t_{pw}	Output Pulse Width			$t_{CYCLE}/2$ ±500		ps	
t_{os}	Output-to-Output Skew	Same Frequency Different Frequencies			350 500	ps	
f_{VCO}	PLL VCO Lock Range	Feedback = VCO/4 Feedback = VCO/6 Feedback = VCO/8 Feedback = VCO/12	TBD TBD TBD TBD	200–500 200–500 200–500 200–500	TBD TBD TBD TBD	MHz	
f_{max}	Maximum Output Frequency	Qc,Qb (÷2) Qa,Qb,Qc (÷4) Qa (÷6)	200 125 80			MHz	
t_{pd}	SYNC to Feedback Delay	Feedback = VCO/4 Feedback = VCO/6 Feedback = VCO/8 Feedback = VCO/12		X_1±150 X_2±150 X_3±150 X_4±150		ps	Note 1
t_{PLZ}, t_{PHZ}	Output Disable Time				TBD		
t_{PZL}, t_{PLH}	Output Enable Time				TBD		
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±50	±100	ps	
t_{lock}	Maximum PLL Lock Time				10	ms	

1 X_1, X_2, X_3, and X_4 all to be determined.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC952 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC952 clock driver is effectively doubled due to its capability to drive multiple lines.

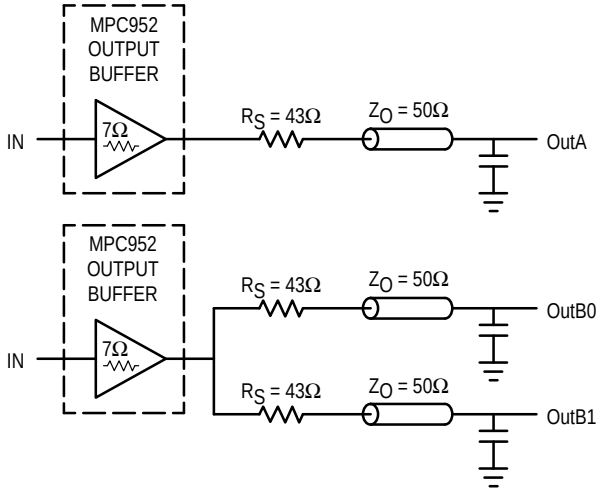


Figure 1. Single versus Dual Transmission Lines

The waveform plots of Figure 2 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC952 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC952. The output waveform in Figure 2 shows a step in the waveform, this step is caused

by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

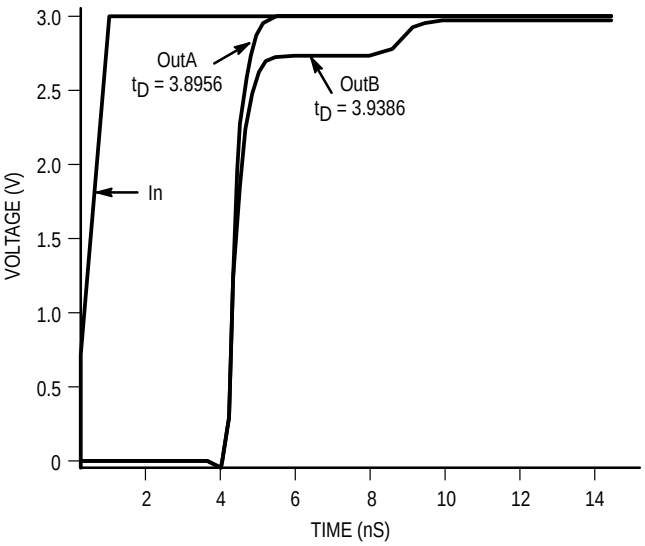
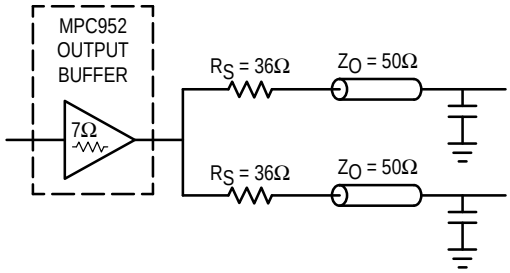


Figure 2. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



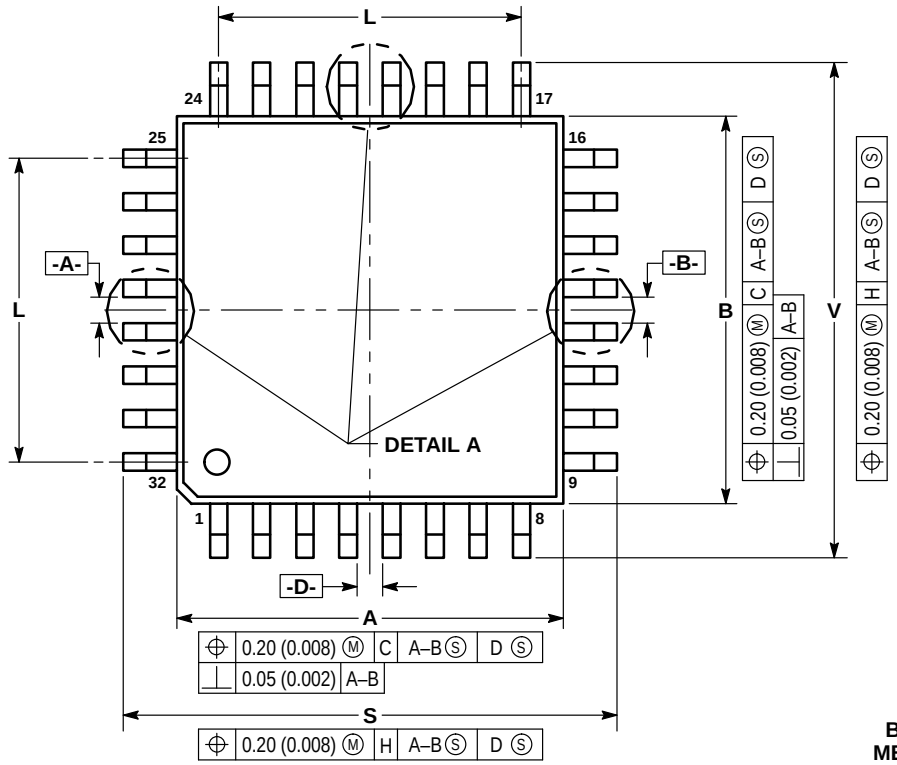
7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

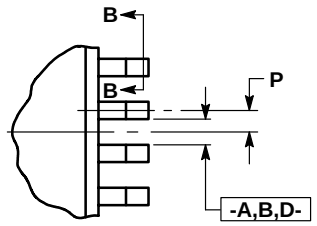
Figure 3. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

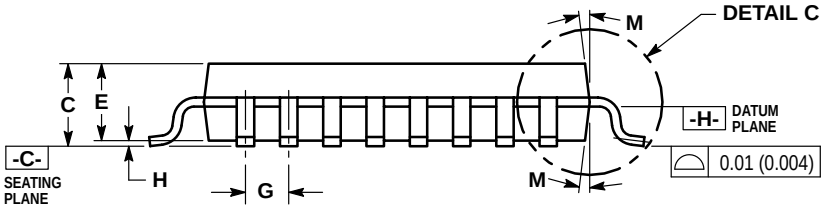
OUTLINE DIMENSIONS

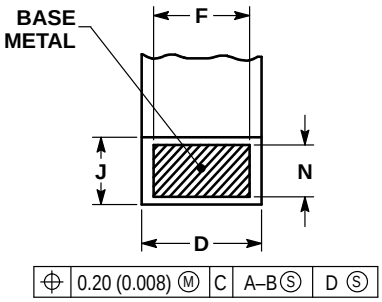
FA SUFFIX
TQFP PACKAGE
CASE 873-01
ISSUE A



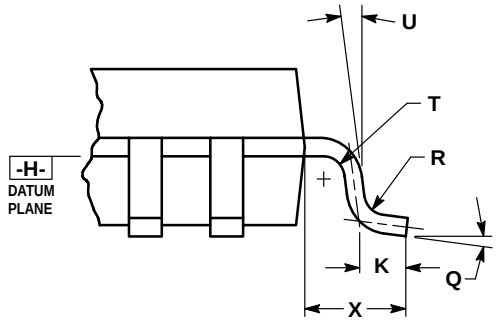


DETAIL A





SECTION B-B
VIEW ROTATED 90° CLOCKWISE



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A–, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.