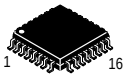
Low Voltage PLL Clock Driver

MPC950
MPC951

LOW VOLTAGE
PLL CLOCK DRIVER



FA SUFFIX
TQFP PACKAGE
CASE 873-01

The MPC950/951 are 3.3V compatible, PLL based clock driver devices targeted for high end desktop PC's. With output frequencies of up to 180MHz and output skews of 375ps the MPC950 is ideal for the most demanding desktop PC designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board today's microprocessors and ASiC's. The devices offer 9 low skew outputs, the outputs are configurable to support the clocking needs of the various high performance micro-processors.

- Fully Integrated PLL
- Oscillator or Crystal Reference Input
- Output Frequency up to 180MHz
- Tri-statable Outputs
- Compatible with PowerPC™ and Intel Microprocessors
- TQFP Packaging
- Output Frequency Configurable
- ±100ps Typical Cycle–to–Cycle Jitter

The PowerPC 601 microprocessor requires processor clock speeds of up to 160MHz with potentially higher speeds in the future. The MPC950 clock driver is well positioned for first and next generation MPC601 systems. In addition to the MPC601 the MPC950 can be configured to drive both the MPC603 and MPC604 microprocessors (for cost sensitive MPC603 designs refer to the MPC930 data sheet). The MPC950 can be configured with various number of outputs running at the processor clock rate while the rest run at half the processor clock to provide flexibility for addressing the various clock load requirements from one PowerPC based system to the next. The device can also be configured to drive the Pentium™ microprocessor. For applications where the entire system runs at 66MHz all 9 outputs can be programmed for the common clock rate. For future Pentium processor speed upgrades it is likely that the bus will run at half the processor speed, thus the MPC950 provides future upgradeability for Pentium based designs.

Two selectable feedback division ratios are available on the MPC950 to provide further flexibility. The FBSEL pin will choose between a divide by 8 or a divide by 16 of the VCO frequency to be compared with the input reference to the MPC950. The internal VCO is running at either 2x or 4x the high speed output, depending on configuration, so that the input reference will be either one half, one fourth or one eighth the high speed output.

The MPC951 replaces the crystal oscillator and internal feedback of the MPC950 with a differential PECL reference input and an external feedback input. These features allow for the MPC951 to be used as a zero delay, low skew fanout buffer. In addition, the external feedback allows for a wider variety of input-to-output frequency relationships. The MPC951 REF_SEL pin allows for the selection of an alternate LVCMOS input clock to be used as a test clock or to provide the reference for the PLL from an LVCMOS source.

The MPC950 provides an external test clock input for scan clock distribution or system diagnostics. In addition the REF_SEL pin allows the user to select between a crystal input to an on-board oscillator for the reference or to chose a TTL level oscillator input directly. The on-board crystal oscillator requires no external components beyond a series resonant crystal.

Both the MPC950 and MPC951 are fully 3.3V compatible and require no external loop filter components. All inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50Ω transmission lines. For series terminated 50Ω lines, each of the MPC950 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32-lead TQFP package to provide the optimum combination of board density and performance.

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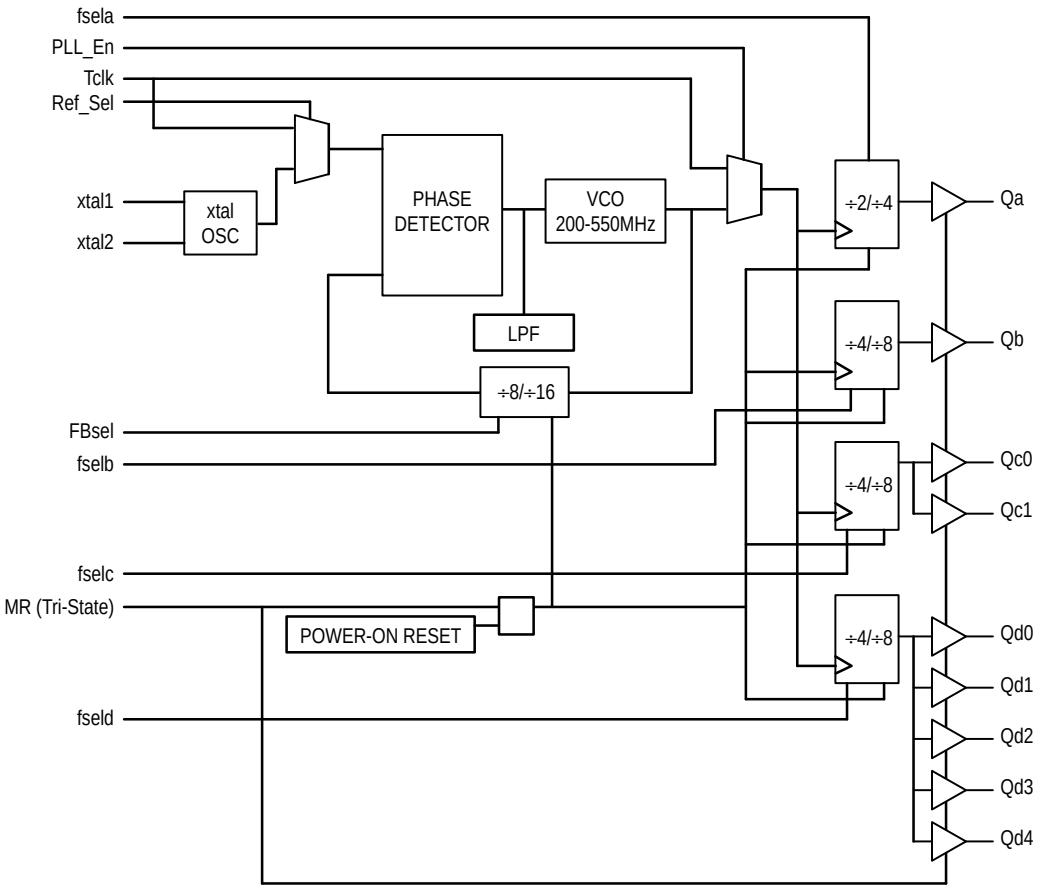
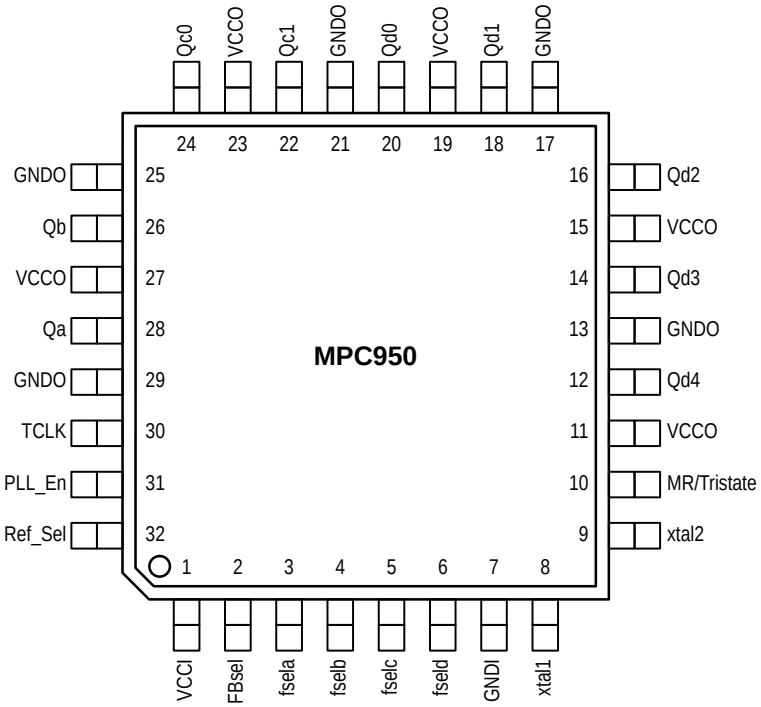
MPC950 LOGIC DIAGRAM

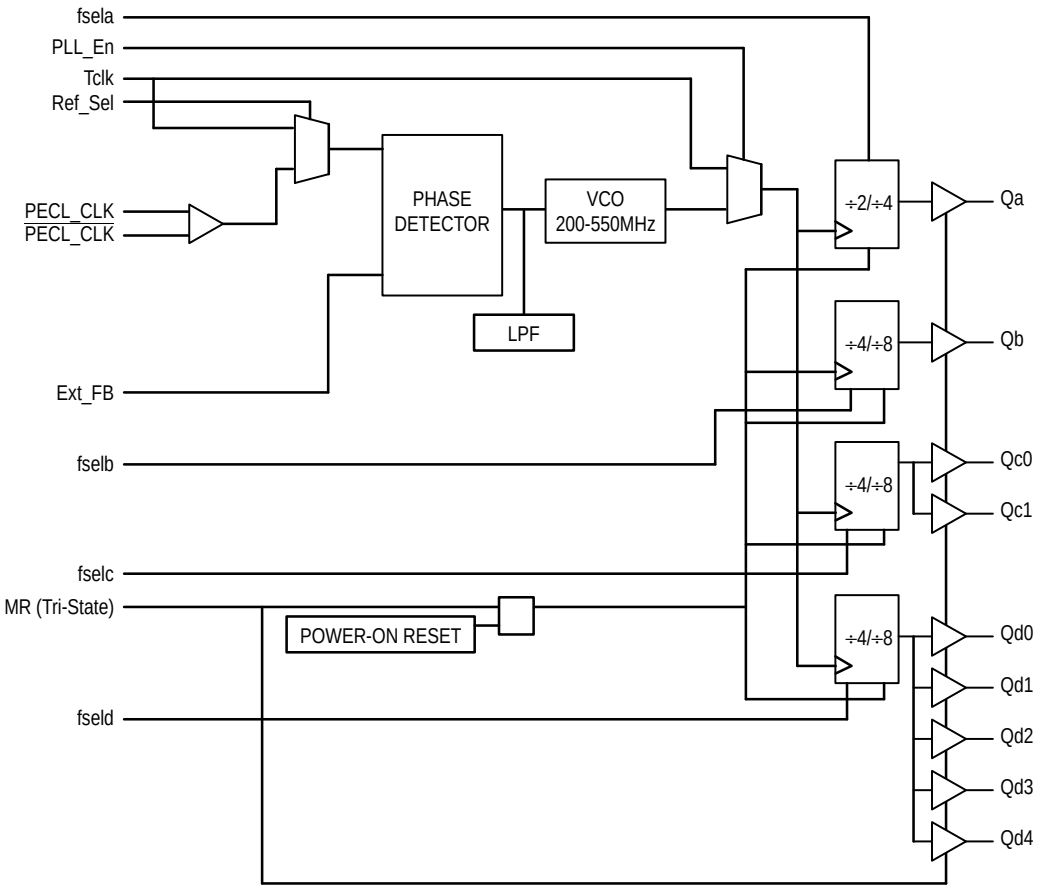


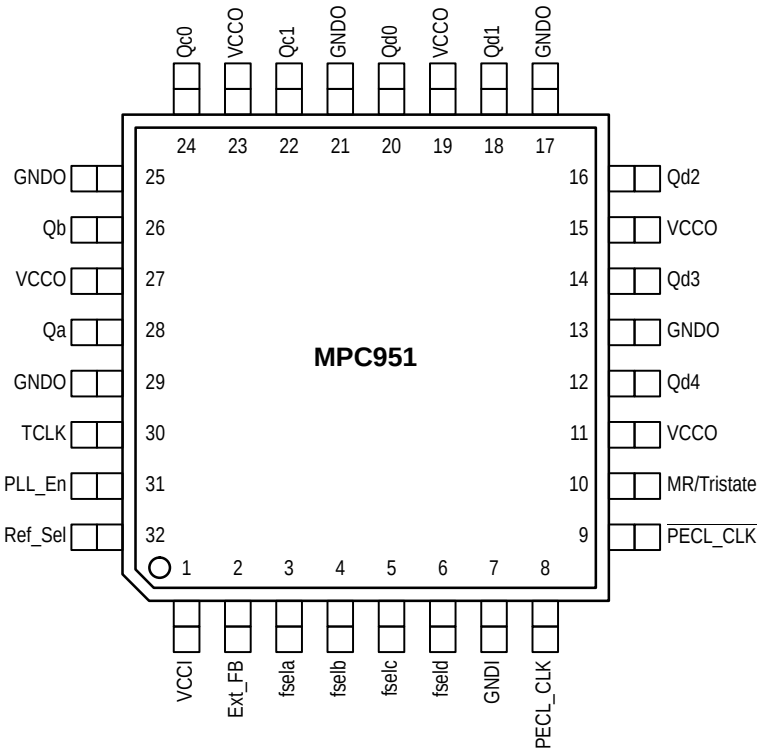


FUNCTION TABLES

Ref_Sel	Function
1	TCLK
0	XTAL_OSC
PLL_En	**Function**
1	PLL Enabled
0	PLL Bypass
FBsel	**Function**
1	÷8
0	÷16
MR/Tristate	**Function**
1	Outputs Disabled
0	Outputs Enabled

MPC951 LOGIC DIAGRAM





FUNCTION TABLES

Ref_Sel	Function
1	TCLK
0	PECL_CLK
PLL_En	**Function**
1	PLL Enabled
0	PLL Bypass
MR/Tristate	**Function**
1	Outputs Disabled
0	Outputs Enabled

FUNCTION TABLE – MPC950/951

INPUTS				OUTPUTS				TOTALS		
fsela	fselb	fselc	fseld	Qa(1)	Qb(1)	Qc(2)	Qd(5)	Total 2x	Total x	Total x/2
0	0	0	0	2x	x	x	x	1	8	0
0	0	0	1	2x	x	x	x/2	1	3	5
0	0	1	0	2x	x	x/2	x	1	6	2
0	0	1	1	2x	x	x/2	x/2	1	1	7
0	1	0	0	2x	x/2	x	x	1	7	1
0	1	0	1	2x	x/2	x	x/2	1	2	6
0	1	1	0	2x	x/2	x/2	x	1	3	5
0	1	1	1	2x	x/2	x/2	x/2	1	0	8
1	0	0	0	x	x	x	x	0	9	0
1	0	0	1	x	x	x	x/2	0	4	5
1	0	1	0	x	x	x/2	x	0	7	2
1	0	1	1	x	x	x/2	x/2	0	2	7
1	1	0	0	x	x/2	x	x	0	8	1
1	1	0	1	x	x/2	x	x/2	0	3	6
1	1	1	0	x	x/2	x/2	x	0	6	3
1	1	1	1	x	x/2	x/2	x/2	0	1	8

NOTE: x = $f_{VCO}/4$; 200MHz < f_{VCO} < 550MHz.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK Other	2.135 2.0		2.42 3.6	V	
V_{IL}	Input LOW Voltage	PECL_CLK Other	1.49		1.825 0.8	V	
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –40mA**1**
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 40mA**1**
I_{IN}	Input Current	Input High Current Input Low Current Input High Current (PECL) Input Low Current (PECL)			2 180 180 2	µA	
C_{IN}	Input Capacitance				4	pF	
C_{pd}	Power Dissipation Capacitance				20	pF	
I_{CCI}	Maximum Quiescent Supply Current			70	85	mA	

1 The MPC950/951 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 1	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1 Maximum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (V_{CC} = 3.3V ±5%)

		0°C		25°C to 70°C				
Symbol	Characteristic	Min	Max	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.15	1.0	0.15		1.0	ns	0.8 to 2.0V
t_{pw}	Output Duty Cycle	$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ +750	$t_{CYCLE}/2$ –750		$t_{CYCLE}/2$ +750	ps	
$t_{sk(O)}$	Output-to-Output Skews for Same Frequencies		450		200	375	ps	
	for Different Frequencies Qa_{fmax} < 150MHz		550		325	500		
	for Different Frequencies Qa_{fmax} > 150MHz		800			750		
f_{Xtal}	Crystal Oscillator Frequency	10	25	10		25	MHz	Note 2
f_{VCO}	PLL VCO Lock Range Feedback = VCO/4	200	550	200		550	MHz	MPC951
	Feedback = VCO/8	150	550	150		550		MPC950 or 951
	Feedback = VCO/16	150	550	150		550		MPC950
f_{max}	Maximum Output Frequency Qa (÷2)		180			180	MHz	
	Qa/Qb (÷4)		137.5			137.5		
	Qb (÷8)		69			69		
t_{pd}	SYNC to Feedback Delay						ps	
	Feedback = VCO/4				X_1±150			MPC951 Only[1]
	Feedback = VCO/8				X_2±150			MPC951 Only[1]
$t_{PLZ,HZ}$	Output Disable Time		7			7	ns	
t_{PZL}	Output Enable Time		6			6	ns	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)				±100		ps	Note 3
t_{lock}	Maximum PLL Lock Time		10			10	ms	

1 X_1 and X_2 all to be determined. The specification is guaranteed for the MPC951 only.
2 See Applications Info section for more crystal information.
3 See Applications Info section for more jitter information.

APPLICATIONS INFORMATION

Programming the MPC950/951

The MPC950/951 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option of the MPC951 allows for a great deal of flexibility in establishing unique input to output frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 4:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/8. These settings will provide output frequencies with a 4:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range is a function of the feedback divide ratios and can be found in the specification tables. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC950/951 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs for the MPC950. For external feedback (MPC951) Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external

feedback condition. Figure 1 through Figure 6 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Using the MPC951 as a Zero Delay Buffer

The external feedback option of the MPC951 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The feedback divider affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the feedback divisor the Tpd of the MPC951 is a function of the feedback configuration used. The Tpd of the device is specified in the specification tables.

When used as a zero delay buffer the MPC951 will likely be in a nested clock tree application. For these applications the MPC951 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC951 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC951 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 650ps (300ps for Tpd variation plus 350ps output–to–output skew). For devices that are configured differently one must account for the differences between the nominal delays of the multiple devices.

Table 1. Programmable Output Frequency Relationships

INPUTS				OUTPUTS			
fsela	**fselb**	**fselc**	**fseld**	**Qa**	**Qb**	**Qc**	**Qd**
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

Table 2. Input Reference versus Output Frequency Relationships (MPC950 Only)

					FB_Sel = ‘1’				FB_Sel = ‘0’			
Config	**fsela**	**fselb**	**fselc**	**fseld**	**Qa**	**Qb**	**Qc**	**Qd**	**Qa**	**Qb**	**Qc**	**Qd**
1	0	0	0	0	4x	2x	2x	2x	8x	4x	4x	4x
2	0	0	0	1	4x	2x	2x	x	8x	4x	4x	2x
3	0	0	1	0	4x	2x	x	2x	8x	4x	2x	4x
4	0	0	1	1	4x	2x	x	x	8x	4x	2x	2x
5	0	1	0	0	4x	x	2x	2x	8x	2x	4x	4x
6	0	1	0	1	4x	x	2x	x	8x	2x	4x	2x
7	0	1	1	0	4x	x	x	2x	8x	2x	2x	4x
8	0	1	1	1	4x	x	x	x	8x	2x	2x	2x
9	1	0	0	0	2x	2x	2x	2x	4x	4x	4x	4x
10	1	0	0	1	2x	2x	2x	x	4x	4x	4x	2x
11	1	0	1	0	2x	2x	x	2x	4x	4x	2x	4x
12	1	0	1	1	2x	2x	x	x	4x	4x	2x	2x
13	1	1	0	0	2x	x	2x	2x	4x	2x	4x	4x
14	1	1	0	1	2x	x	2x	x	4x	2x	4x	2x
15	1	1	1	0	2x	x	x	2x	4x	2x	2x	4x
16	1	1	1	1	2x	x	x	x	4x	2x	2x	2x

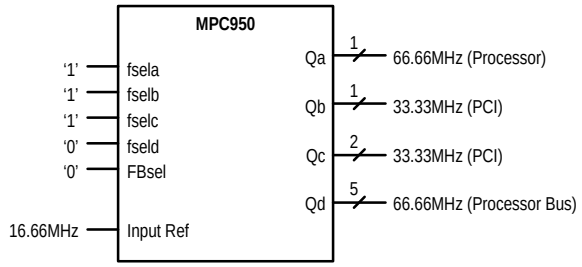


Figure 1. Pentium/PowerPC 604 Configuration

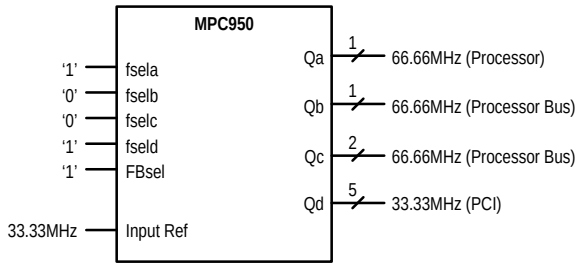


Figure 2. Pentium/PowerPC 604 Configuration

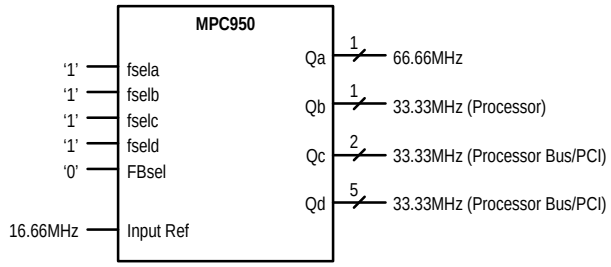


Figure 3. PowerPC 603 Configuration

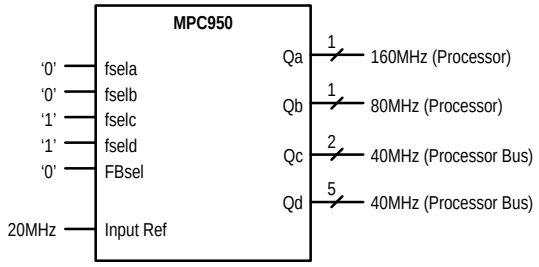


Figure 4. PowerPC 601 Configuration

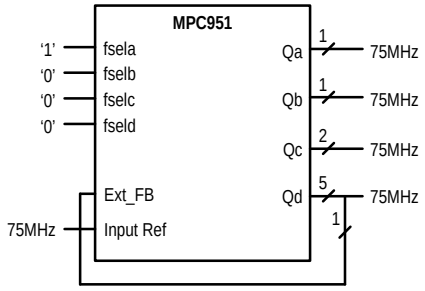


Figure 5. "Zero" Delay Buffer

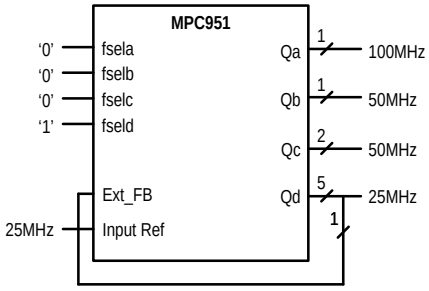


Figure 6. "Zero" Delay Frequency Multiplier

Jitter Performance of the MPC950/951

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC950/951 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC950/951, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC950/951. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle–to–cycle jitter. Most likely, this is a conservative estimate of the cycle–to–cycle jitter.

There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are

switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC950/951, where a number of the outputs can be switching synchronously but at different frequencies a “multi–modal” jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 7, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a “multi–modal” distribution as pictured in Figure 7. Depending on the size of the PLL jitter and the relative displacement of the edges the “multi–modal” distribution will appear truly “multi–modal” or simply like a “fat” Gaussian distribution. Again note that in the case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

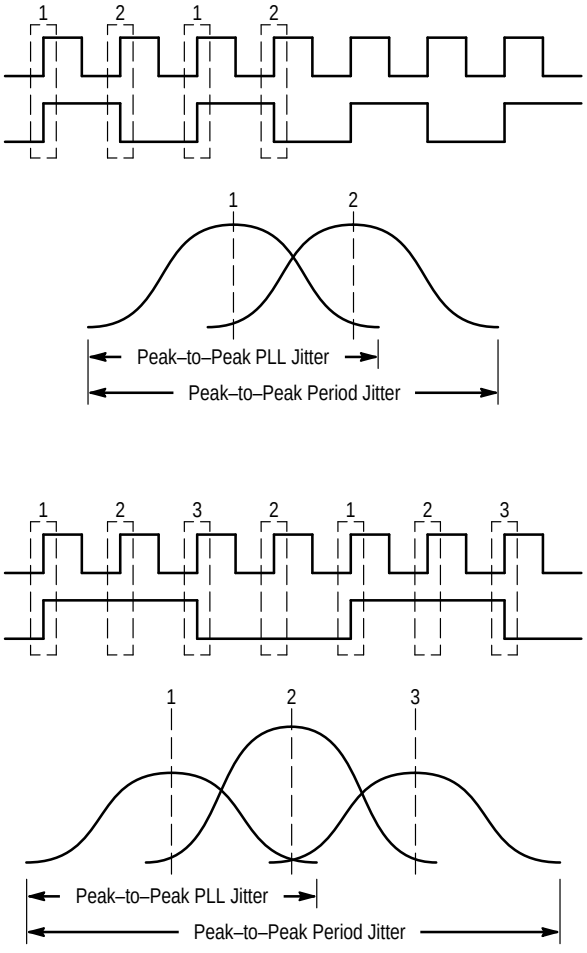
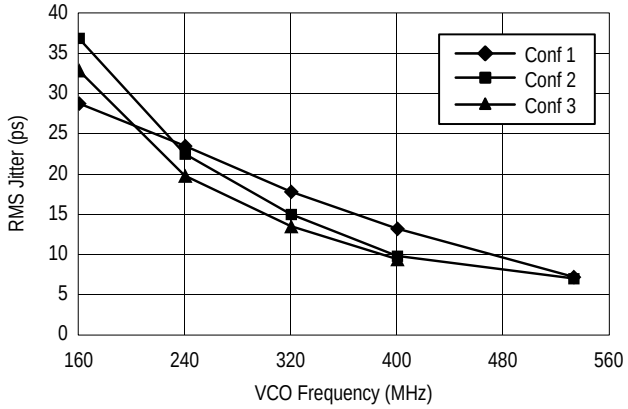


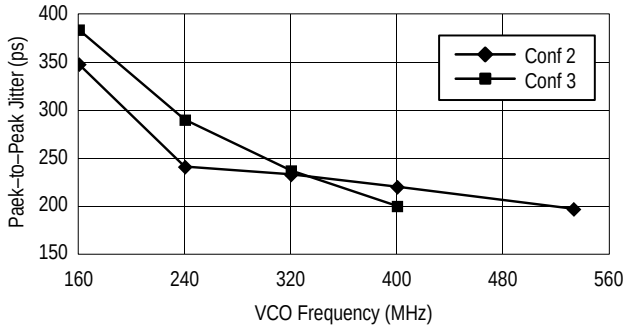
Figure 7. PLL Jitter and Edge Displacement

Figure 8 graphically represents the PLL jitter of the MPC950/951. The data was taken for several different output configurations. By triggering on the lowest frequency output the PLL jitter can be measured for configurations in which outputs are switching at different frequencies. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency.



Conf 1 = All Outputs at the Same Frequency
Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

Figure 8. RMS PLL Jitter versus VCO Frequency



Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

Figure 9. Peak–to–Peak Period Jitter versus VCO Frequency

Two different configurations were chosen to look at the period displacement caused by the switching outputs. Configuration 3 is considered worst case as the “trimodal” distribution (as pictured in Figure 7) represents the largest spread between distribution peaks. Configuration 2 is considered a typical configuration with half the outputs at a high frequency and the remaining outputs at one half the high frequency. For these cases the peak–to–peak numbers are reported in Figure 9 as the sigma numbers are useless because the distributions are not Gaussian. For situations where the outputs are synchronous and switching at different frequencies the measurement technique described here is insufficient to use for establishing guaranteed limits. Other techniques are currently being investigated to identify a more accurate and repeatable measurement so that guaranteed

limits can be provided. The data generated does give a good indication of the general performance, a performance that in most cases is well within the requirements of today's microprocessors.

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline may be the most difficult, and in some cases impossible, to follow. Try to minimize the number of different frequencies sourced from a single chip. The fixed edge displacement associated with the switching noise in most cases nearly doubles the "effective" jitter of a high speed output.

Power Supply Filtering

The MPC950/951 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC950/951 provides separate power supplies for the output buffers (V_{CCO}) and the internal logic (V_{CCI}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCI} pin for the MPC950/951.

Figure 10 illustrates two typical power supply filter schemes. The MPC950/951 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCI} pin of the MPC950/951. From the data sheet the I_{CCI} current (the current sourced through the V_{CCI} pin) is typically 70mA (85mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCI} pin very little DC voltage drop can be tolerated. The ferrite bead shown in Figure 10a must have a DC resistance of 1–2 ohm to meet the voltage drop criteria. The ferrite bead could be eliminated altogether and the filter could consist of only the two capacitors, this will provide a level of filtering although it would not be optimum due the lack of any significant AC impedance in the power line.

Figure 10b takes advantage of the fact that most 3.3V systems still have a 5.0V supply available. Here the DC resistance of the filter is used to drop the supply down towards 3.3V while providing the AC impedance one needs for filtering. A 1000µH choke with a DC resistance of around 22Ω is shown (a series combination of choke and resistor could be used to optimize the DC resistance) to optimize AC attenuation, however a simple resistor could also be used. It is important that the V_{CCI} pin never be more positive than V_{CCO}+0.5V to ensure that no internal parasitic diodes are turned on.

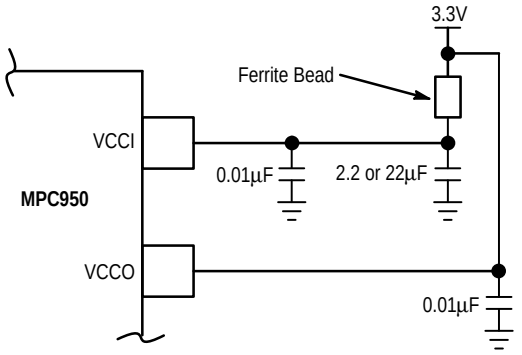


Figure 10a. Power Supply Filter from a 3.3V Supply

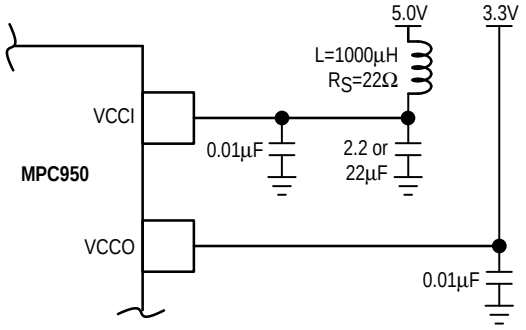


Figure 10b. Power Supply Filter from a 5.0V Supply

Although the MPC950/951 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the On–Board Crystal Oscillator

The MPC950/951 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC950/951 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. In addition, with crystals with a higher shunt capacitance, it may be necessary to place a 1k resistor across the two crystal leads.

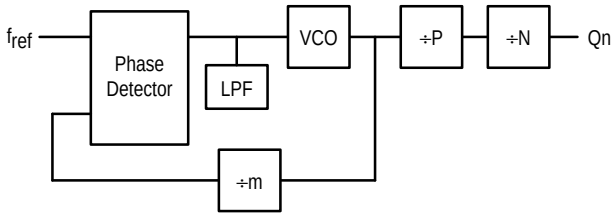
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC950/951 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 3. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5pF Max
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC950/951 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 11 should be used. The P and the M values for the MPC950/951 are also included in Figure 11. The M values can be found in the configuration tables included in this applications section.



$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 8 (FBsel = ‘1’), 16(FBsel = ‘0’)
P = 1

Figure 11. PLL Block Diagram

For the MPC950/951 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

Qa = 160MHz
Qb = 80MHz
Qc = 40MHz
Qd = 40MHz
FBSel = ‘0’

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 3

fQd = VCO/8 then N = 8 OR fQa = VCO/2 then N = 2

From Figure 11

m = 16 and P = 1

$$f_{ref} = \frac{40 \cdot 8 \cdot 1}{16} = 20MHz \text{ OR } \frac{160 \cdot 2 \cdot 1}{16} = 20MHz$$

Driving Transmission Lines

The MPC950/951 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can

be driven by each output of the MPC950/951 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC950/951 clock driver is effectively doubled due to its capability to drive multiple lines.

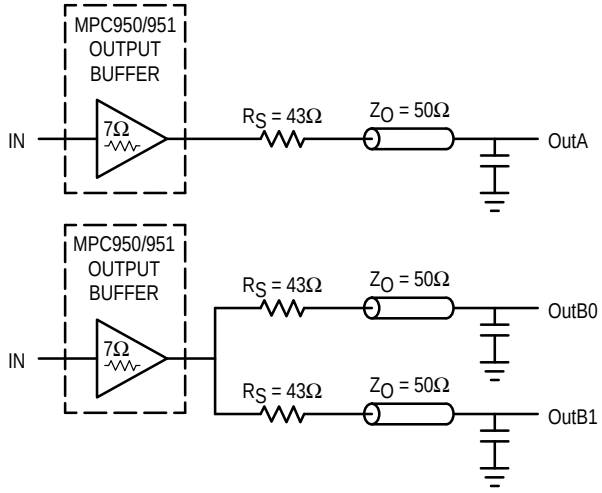


Figure 12. Single versus Dual Transmission Lines

The waveform plots of Figure 13 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC950/951 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC950/951. The output waveform in Figure 13 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / (Rs + Ro + Zo))$$

$Zo = 50\Omega \,||\, 50\Omega$
$Rs = 43\Omega \,||\, 43\Omega$
$Ro = 7\Omega$

$$VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)$$
$$= 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

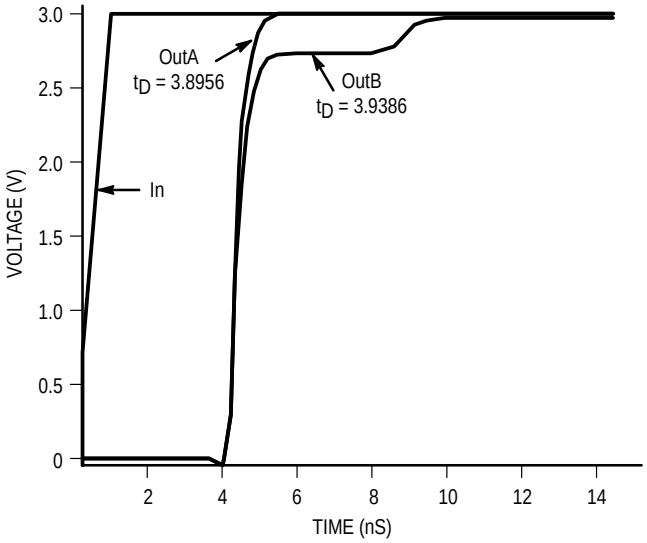
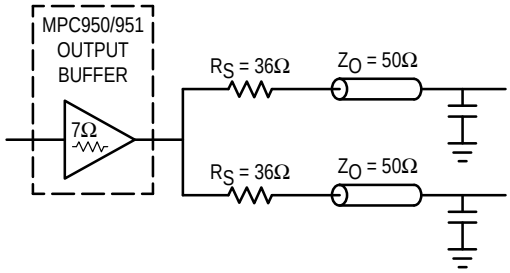


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



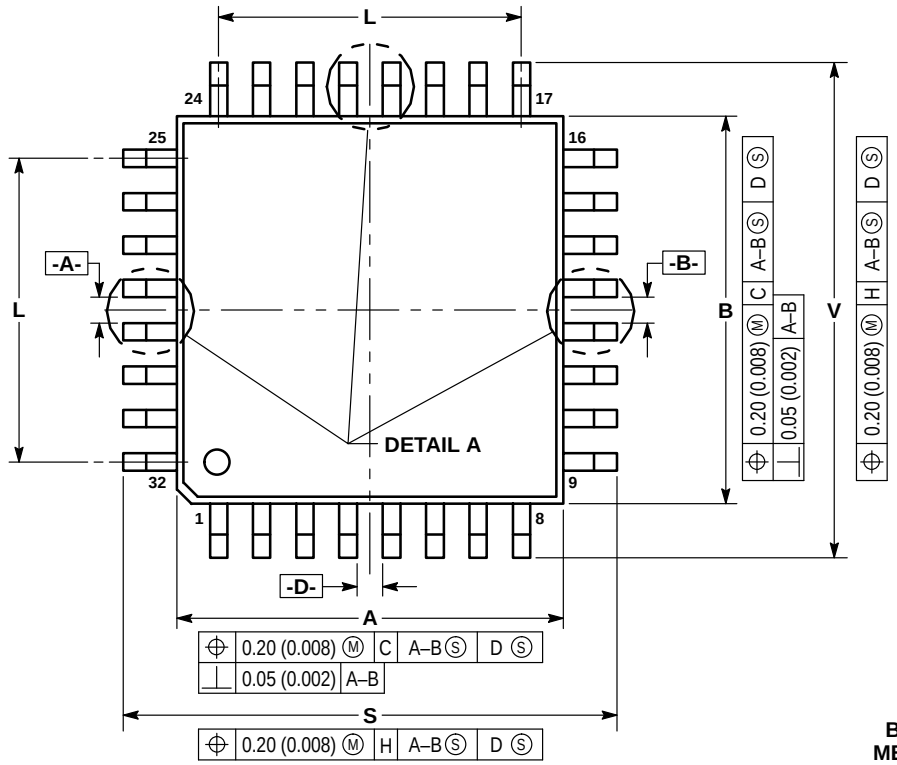
$$7\Omega + 36\Omega \,||\, 36\Omega = 50\Omega \,||\, 50\Omega$$
$$25\Omega = 25\Omega$$

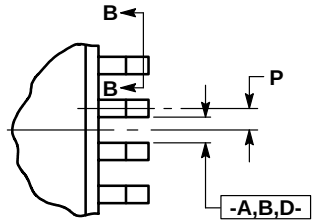
Figure 14. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

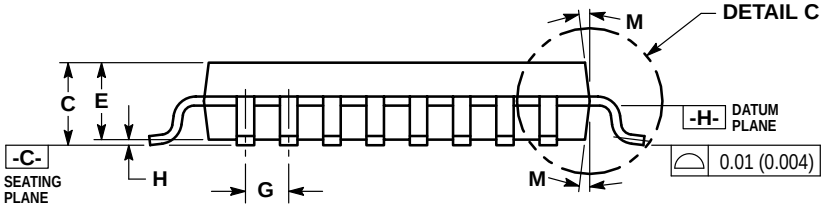
OUTLINE DIMENSIONS

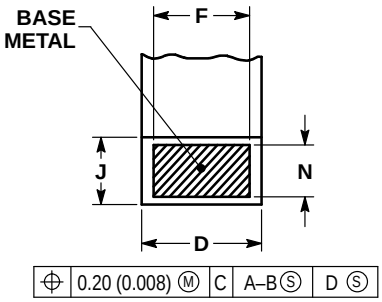
FA SUFFIX
TQFP PACKAGE
CASE 873-01
ISSUE A



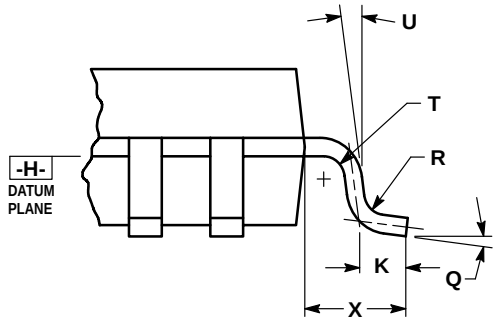


DETAIL A





SECTION B-B
VIEW ROTATED 90° CLOCKWISE



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A–, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

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JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
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