*Advance Information*

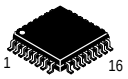
# Low Voltage 1:10 CMOS Clock Driver

**MPC946**

**LOW VOLTAGE 1:10 CMOS CLOCK DRIVER**

The MPC946 is a low voltage CMOS, 10 output clock buffer. The 10 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The ten outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 300ps the MPC946 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with an even higher level of performance consult the MPC949 data sheet.

- Clock Distribution for Pentium™ Systems with PCI
- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 300ps Output to Output Skew
- Drives up to 20 Independent Clock Lines
- Maximum Input/Output Frequency of 100MHz
- Tristatable Outputs
- 32–Lead TQFP Packaging
- 3.3V VCC Supply




**FA SUFFIX**
TQFP PACKAGE
CASE 873-01

With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC946 are ideal for driving series terminated transmission lines. More specifically each of the 10 MPC946 outputs can drive two series terminated transmission lines. With this capability, the MPC946 has an effective fanout of 1:20 in applications using point–to–point distribution schemes.

The MPC946 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected.

All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/Tristate input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

The MPC946 is fully 3.3V compatible. The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

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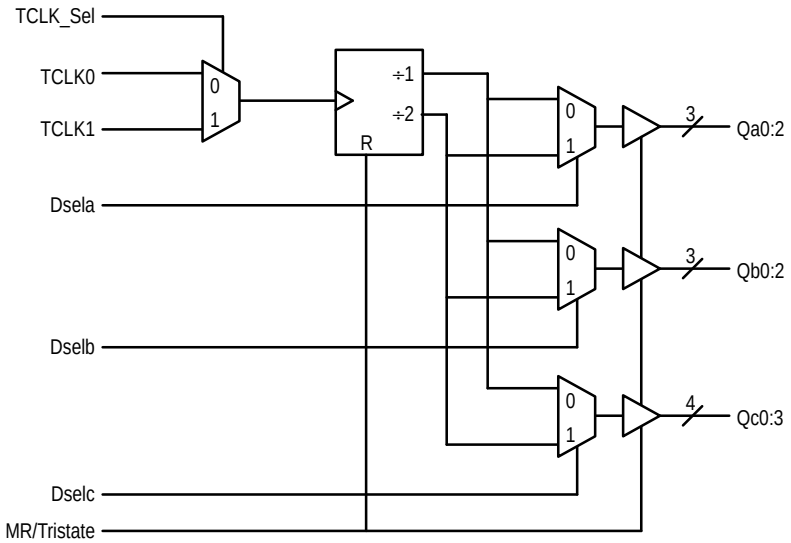
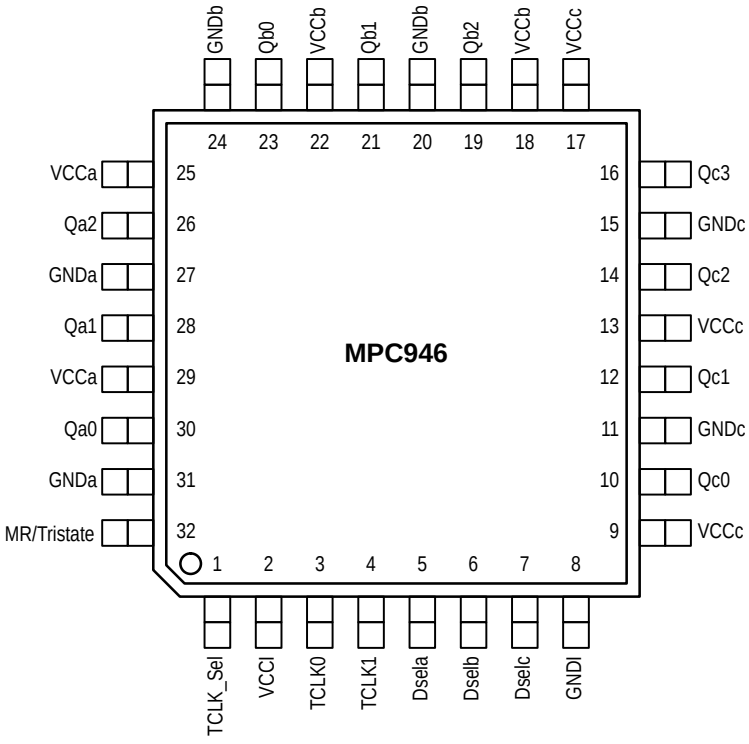
This document contains information on a new product. Specifications and information herein are subject to change without notice.

## LOGIC DIAGRAM




**Pinout: 32-Lead TQFP** (Top View)




### FUNCTION TABLES

| TCLK_Sel | Input |
|---|---|
| 0<br>1 | TCLK0<br>TCLK1 |
| **Dselx** | **Outputs** |
| 0<br>1 | 1x<br>1/2x |
| **MR/Tristate** | **Outputs** |
| 0<br>1 | Tristate<br>Enabled |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current (CMOS Inputs) | TBD | TBD | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.5 | | | V | $I_{OH}$ = –20mA**1** |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | V | $I_{OL}$ = 20mA**1** |
| $I_{IN}$ | Input Current | | | –100 | µA | Note 2 |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 21 | | mA | |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | TBD | pF | |

**1** The MPC946 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).

**2** $I_{IN}$ current is a result of internal pull–up resistors.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | 100 | | | MHz | Note 1 |
| $t_{pd}$ | Propagation Delay TCLK to Q | | 10 | | ns | Note 1 |
| $t_{sk(o)}$ | Output-to-Output Skew | | 300 | | ps | Note 1 |
| $t_{sk(pr)}$ | Part-to-Part Skew | | 2.0 | | ns | Note 2 |
| $t_{pwo}$ | Output Pulse Width | | $t_{CYCLE}$/2 ±500 | | ps | Note 1, Measured at $V_{CC}$/2 |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | | | 11 | ns | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | | | 11 | ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | 0.8V to 2.0V |

**1.** Driving 50Ω transmission lines.

**2.** Part-to-part skew at a given temperature and voltage.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC946 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC946 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC946 clock driver is effectively doubled due to its capability to drive multiple lines.

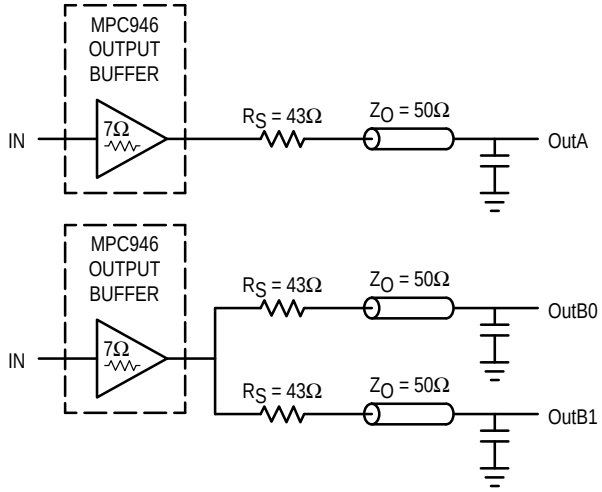



**Figure 1. Single versus Dual Transmission Lines**

The waveform plots of Figure 2 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC946 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC946. The output waveform in Figure 2 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS ( Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

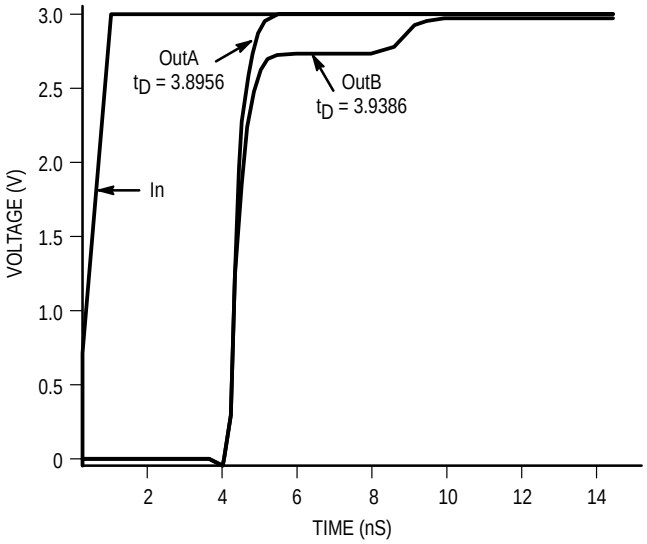
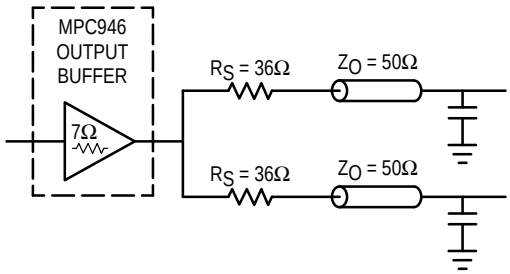



**Figure 2. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

**Figure 3. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

## OUTLINE DIMENSIONS

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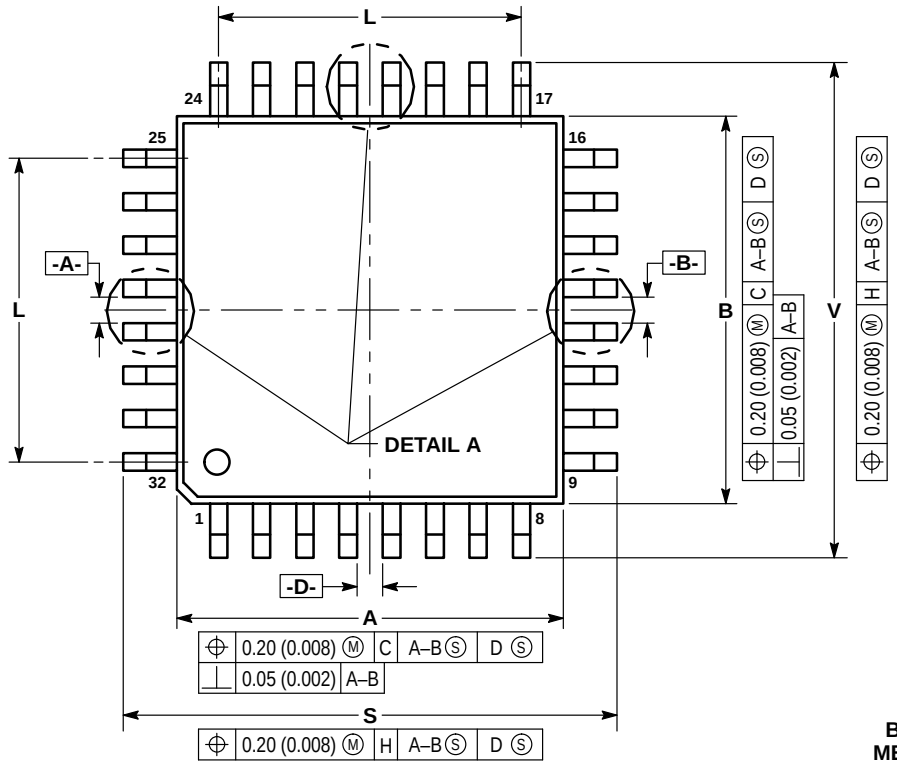
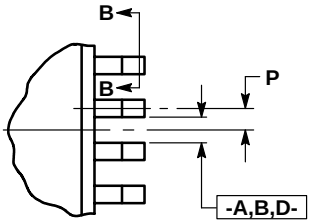
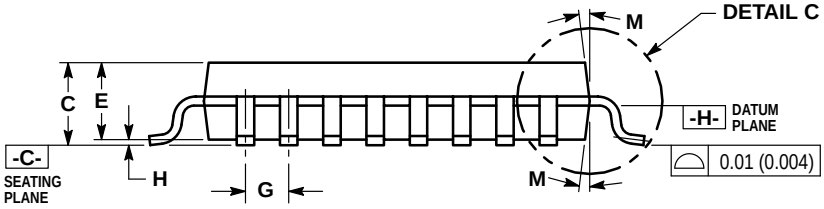
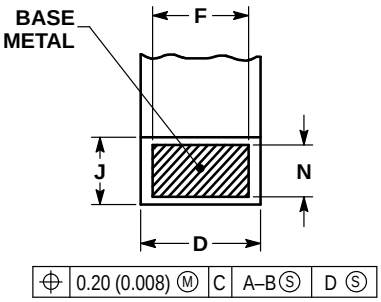
CASE 873-01
ISSUE A



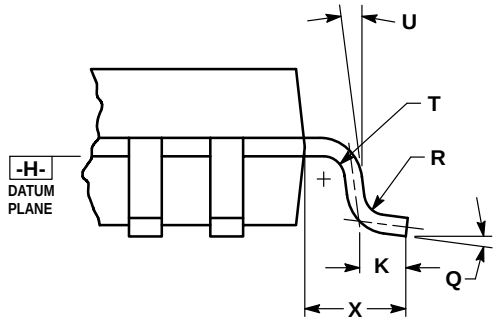




**DETAIL A**




**SECTION B-B**
**VIEW ROTATED 90° CLOCKWISE**




**DETAIL C**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A–, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.95 | 7.10 | 0.274 | 0.280 |
| B | 6.95 | 7.10 | 0.274 | 0.280 |
| C | 1.40 | 1.60 | 0.055 | 0.063 |
| D | 0.273 | 0.373 | 0.010 | 0.015 |
| E | 1.30 | 1.50 | 0.051 | 0.059 |
| F | 0.273 | — | 0.010 | — |
| G | 0.80 BSC | | 0.031 BSC | |
| H | — | 0.20 | — | 0.008 |
| J | 0.119 | 0.197 | 0.005 | 0.008 |
| K | 0.33 | 0.57 | 0.013 | 0.022 |
| L | 5.6 REF | | 0.220 REF | |
| M | 6° | 8° | 6° | 8° |
| N | 0.119 | 0.135 | 0.005 | 0.005 |
| P | 0.40 BSC | | 0.016 BSC | |
| Q | 5° | 10° | 5° | 10° |
| R | 0.15 | 0.25 | 0.006 | 0.010 |
| S | 8.85 | 9.15 | 0.348 | 0.360 |
| T | 0.15 | 0.25 | 0.006 | 0.010 |
| U | 5° | 11° | 5° | 11° |
| V | 8.85 | 9.15 | 0.348 | 0.360 |
| X | 1.0 REF | | 0.039 REF | |

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