Advance Information

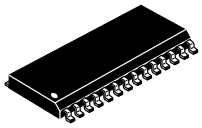
Multiple Output Clock Synthesizer

MPC9159-422

MULTIPLE OUTPUT CLOCK SYNTHESIZER

The MPC9159–422 is a multiple output clock synthesizer ideally suited for Pentium processor based motherboards that require both 3.3V and 5V clock operation. The device provides additional CPU clocks over other 9159 options. Both synchronous and asynchronous PCI bus clocks are supported.

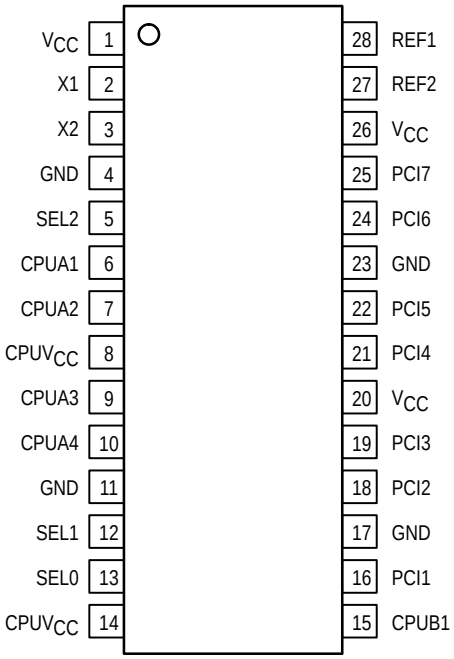
- Supports dual 3.3V/5V operation
- Five Skew Controlled CPU Clock Outputs
- Seven Skew Controlled PCI Clock Outputs
- Synchronous and Asynchronous PCI Clock Modes
- Two 14.318 Reference Clock Outputs
- 40Ω Output Drivers
- Built In Crystal Oscillator
- Available in 28–lead SOIC and SSOP



DW SUFFIX
PLASTIC SOIC
CASE 751H–03

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Pinout: 28-Lead SOIC Package (Top View)



FUNCTIONAL BLOCK DIAGRAM

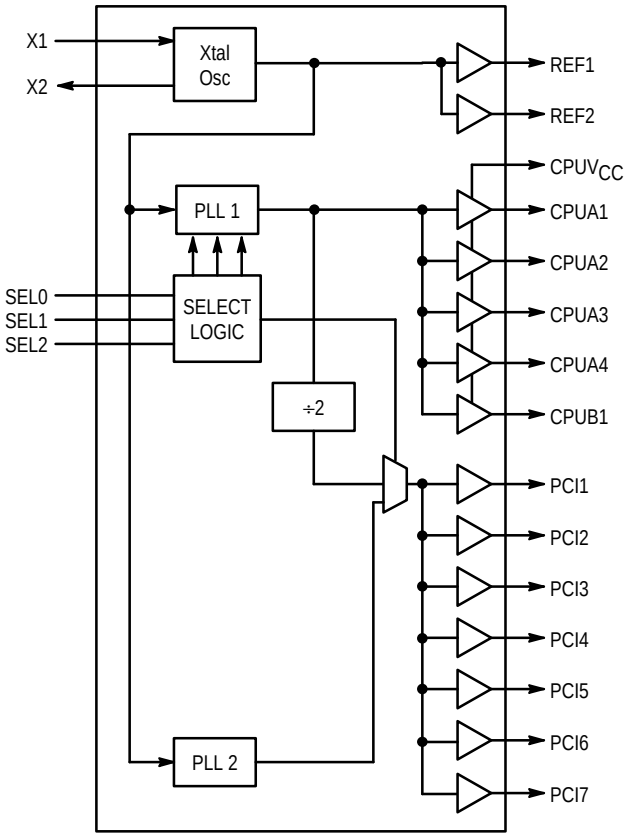


Table 1. Output Frequency Selection

SEL0	SEL1	SEL2	CPUA1:4 CPUB1	PCI1:7	PCI MODE
0	0	0	50	25	Sync
0	0	1	50	33.3	Async
0	1	0	60	30	Sync
0	1	1	60	33.3	Async
1	0	0	66.6	33.3	Sync
1	0	1	75	33.3	Async
1	1	0	66.6	33.3	Sync
1	1	1	Hi–Z	Hi–Z	N/A

Table 2. Pin Descriptions

Pin Name	I/O	Function
PCI1–7	O	PCI Bus Clock Outputs
GND	–	Ground Connection
CPUA1–4	O	CPU Clock Outputs
CPUB1	O	Delayed CPU Clock Output
REF1–2	O	Fixed 14.318MHz Outputs for Various Motherboard Functions
SEL0	I	Frequency Selection Input, LSB (Note 1)
SEL1	I	Frequency Selection Input (Note 1)
SEL2	I	Frequency Selection Input, MSB (Note 1)
V_{CC}	–	Power Supply Connection, 3.3V
$CPUV_{CC}$	–	CPU Output Power Supply
X1	I	Crystal Connection or External Reference Frequency Input
X2	–	Crystal Connection, Leave Unconnected When Using External Reference

1. All inputs, except for X1, have an internal pull–up resistor. Unconnected inputs will assume a logic HIGH condition.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	Input Voltage	–0.5 to +7.0	V
T_A	Operating Temperature Range (In Free-Air)	0 to +70	°C
T_A	Ambient Temperature Range (Under Bias)	–55 to +125	°C
T_{STG}	Storage Temperature Range	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

DC CHARACTERISTICS ($0°C < T_A < 70°C$; $V_{CC} = 3.3V \pm 10\%$)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current		150	–	mA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 3.3V
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 3.3V
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 24mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24mA; V_{CC} = 3.3V
I_{IH}	Input Low Current			–30	µA	V_{IN} = 0V (Includes Pull–Up)
I_{IL}	Input High Current			10	µA	$V_{IN} = V_{CC}$
R_P	Input Resistor Pull–Up		130		kΩ	V_{IN} = 0V
C_I	Input Capacitance			6	pF	Except X1, X2
L_I	Input Inductance			7	nH	Except X1, X2
C_L	Xtal Load Capacitance	10	12	14	pF	Total load from X1, X2

1. Valid power supply connections: 1) $V_{CC} = CPUV_{CC} = 3.3V \pm 5\%$; 2) $V_{CC} = 5V \pm 10\%$, $CPUV_{CC} = 3.3V \pm 5\%$; 3) $V_{CC} = CPUV_{CC} = 5.0V \pm 5\%$

DC CHARACTERISTICS ($0°C < T_A < 70°C$; $V_{CC} = 5.0V \pm 10\%$)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current		230	275	mA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 24mA
V_{OH}	Output High Voltage	V_{CC}–0.4V			V	I_{OH} = –24mA; V_{CC} = 5.0V
I_{IH}	Input Low Current			–30	µA	V_{IN} = 0V (Includes Pull–Up)
I_{IL}	Input High Current			10	µA	$V_{IN} = V_{CC}$
R_P	Input Resistor Pull–Up		150		kΩ	V_{IN} = 0V
C_I	Input Capacitance			6	pF	Except X1, X2
L_I	Input Inductance			7	nH	Except X1, X2
C_L	Xtal Load Capacitance	10	12	14	pF	Total load from X1, X2

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AC CHARACTERISTICS[1] (0°C < T_A < 70°C; V_{CC} = 3.3V ±10%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
Processor Clock Outputs (CPUA1–4, CPUB1)						
t_{jcc}	Output Clock Jitter, Cycle–to–Cycle			±250	ps	
t_{sk}	Output Clock Skew (CPUA1–4)			200	ps	Between Any Two Outputs
t_{delay}	CPUA to CPUB Delay		100		ps	
t_{slew}	Output Slew Rate	1.6			V/ns	10pF Load
Bus Clock Outputs (BCLK0–6)						
t_{jcc}	Output Clock Jitter, Cycle–to–Cycle			±250	ps	
t_{sk}	Output Clock Skew			200	ps	Between Any Two Outputs
t_{sk}	Output Clock Skew			500	ps	
t_{slew}	Output Slew Rate	1.0			V/ns	30pF Load
All Clock Outputs						
d_t	Output Duty Cycle	40	50	60	%	@ 1.5V
t_r	Rise Time	0.5		2.0	ns	From 0.4V to 2.4V
t_f	Fall Time	0.5		2.0	ns	From 2.4V to 0.4V
T_{PU}	Stabilization Time from Power–Up			3.0	ms	Within 0.1% Final Freq.
f_D	Long Term Output Frequency Stability (Note 2)			0.01	%	Over V_{CC} and T_A Range
Z_{out}	Output Buffer Impedance V_{CC} = 3.3V V_{CC} = 5.0V		40 30		Ω	

1. All AC tests are performed with the following load conditions: Series terminated lines @ 1.5V thresholds.
2. Long term frequency stability solely affected by crystal oscillator frequency shifts.

APPLICATIONS INFORMATION

MPC9159 Crystal Oscillator

The MPC9159 requires an input clock to generate all output frequencies. The input reference clock can be either an externally generated clock signal or the output from an internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open. The input threshold voltage of pin X1 is $V_{CC}/2$.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The MPC9159 incorporates the feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is 12pF. For optimum frequency accuracy without the addition of external capacitors, a parallel–resonant mode crystal specifying a load of 12pF should be used. This will typically yield reference frequency accuracies within ±100ppm. To achieve similar accuracies with a crystal calling for a greater load, external capacitors must be added such that the total load (internal, external, and parasitic capacitors) equals that called for by the crystal. For example, the use of a crystal calling for a 20pF load capacitance would require the addition of a 16pF capacitor at both pin X1 and X2, each terminated to ground (viewed by the crystal, these external load capacitors are connected in series through the common ground). Failure to match capacitance or the use of a series resonant crystal could result in an oscillator frequency error as high as 500ppm.

The MPC9159 crystal oscillator circuit provides performance characteristics superior to those used in most other clock generator devices. The 14.318MHz output clock from REF0 and REF1 and REF2 exhibits excellent stability, duty cycle and frequency accuracy over a variety of operating and crystal parameters. Duty cycle is also maintained when using an external clock source (connected to pin X1, pin X2 is left open), as long as the external clock has good duty cycle.

MPC9159 PLL Circuits

The MPC9159 PLL (Phase Lock Loop) circuits exhibit fast loop response, satisfying a requirement for the Intel PCI chip sets. Output frequencies are stable within 3msec after power up. Upon changing the condition of SEL1 and SEL0, a new CPU/PCI clock frequency will stabilize within 1msec.

The MPC9159 PLL circuits are optimized for low jitter, stable operation suitable for P6, Pentium and other processor applications. On–chip PLL loop components further assure system noise rejection. With recent MPC9159 enhancements, the MPC9159 has less long–term jitter when compared to other earlier MPC9159 devices.

MPC9159 Clock Outputs

The MPC9159 output buffers are designed to provide good transmission line matching capability and low circuit noise. Output buffer rise and fall times are regulated to limit EMI, control circuit noise and reduce signal and supply bounce. Output slew rate is controlled to within 0.5 to 2V/nS. The MPC9159 has approximately 40Ω clock output buffer impedance (all clock outputs). DC output V/I curves are shown later in this specification. The V/I curves show typical characteristics; parameters shown can change up to ±20% over variations in process, temperature and power supply voltage.

Power Supply Recommendation

All MPC9159 V_{CC} pins should use a common supply connection which is a filtered version of the main system supply. The supply filter is made up of components FB (Ferrite Bead) and C1. These components should be placed somewhere near the clock device, prior to distribution to the decoupling capacitors and V_{CC} pins. C1 should be a tantalum type device.

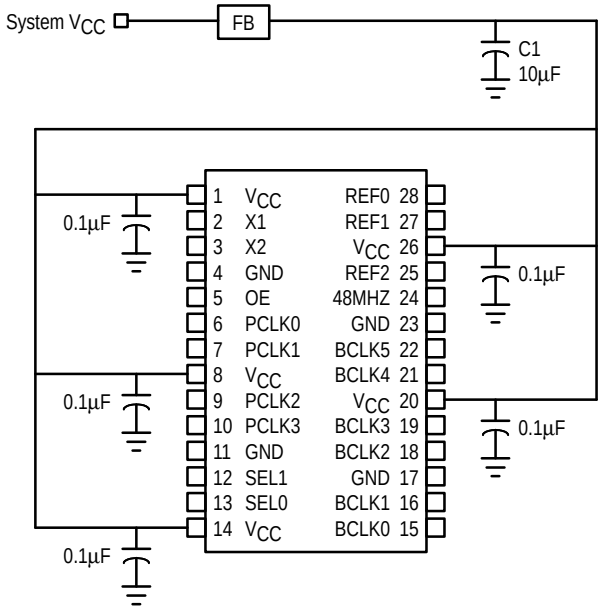


Figure 1. Recommended Power Supply Schematic
(MPC9159–404 Option Shown)

The use of a series resistor in the power supply line is not recommended. Although this does assist C1 in low frequency filtering, the MPC9159 consumes relatively high supply current (as compared to simpler clock chips), resulting in significant voltage drop across the series supply resistor.

It is important to decouple each V_{CC} pin separately. The decoupling capacitor should have a value between 0.02µf and 0.1µf. Surface mount is the preferred package since its physical properties contribute a lower impedance at high frequency. In general, smaller surface mount devices work best (use SMT 603 format if possible). The decoupling cap should be placed as close to the V_{CC} pin as possible since its effect will otherwise be negated by the inductance of the power supply trace. To further maximize the benefit of the decoupling capacitor, the power supply trace should be routed to the decoupling capacitor first, then to the V_{CC} pin.

For MPC9159 ground connections, the best approach is to connect all ground (GND) pins directly to the system ground

plane. This also applies to decoupling capacitors and select pins when programmed to logic 0.

Output Series Termination

With typical MPC9159 edge rates of 1.5V/ns, a PCB trace becomes a transmission line when it is over 1–inch in length. This transmission line needs some sort of termination scheme to ensure good signal integrity at the load (device receiving clock signal). Most motherboards use the practice of *series termination*. In series termination, a series termination resistor (external resistor) is added in series with the driver device output, as shown in Figure 2, series termination resistor value is chosen so that its value, added to the output impedance of the driver, is equal to the PCB trace impedance, or in other words, $R_{TH} = R_S + Z_L$. The series termination resistor must be located close to the device output.

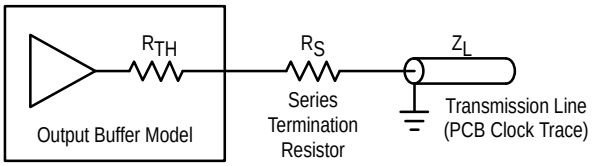


Figure 2. Clock Output Series Termination

Typical system PCB trace impedance is 50–70Ω, which is low enough to produce sufficient signal rise and fall time at the load capacitance presented by a standard CMOS input. Figure 3 illustrates proper series termination of the 40Ω and 20Ω MPC9159 output driving a 60Ω transmission line.

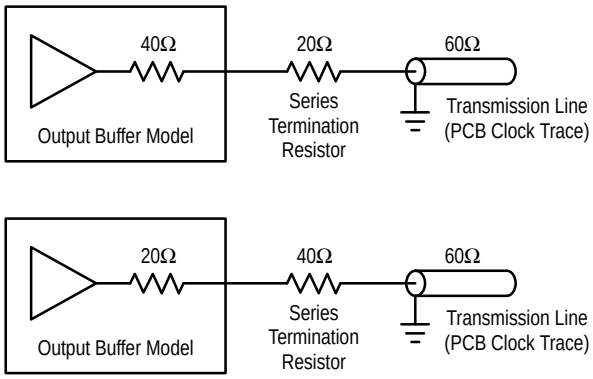


Figure 3. Clock Output Series Termination

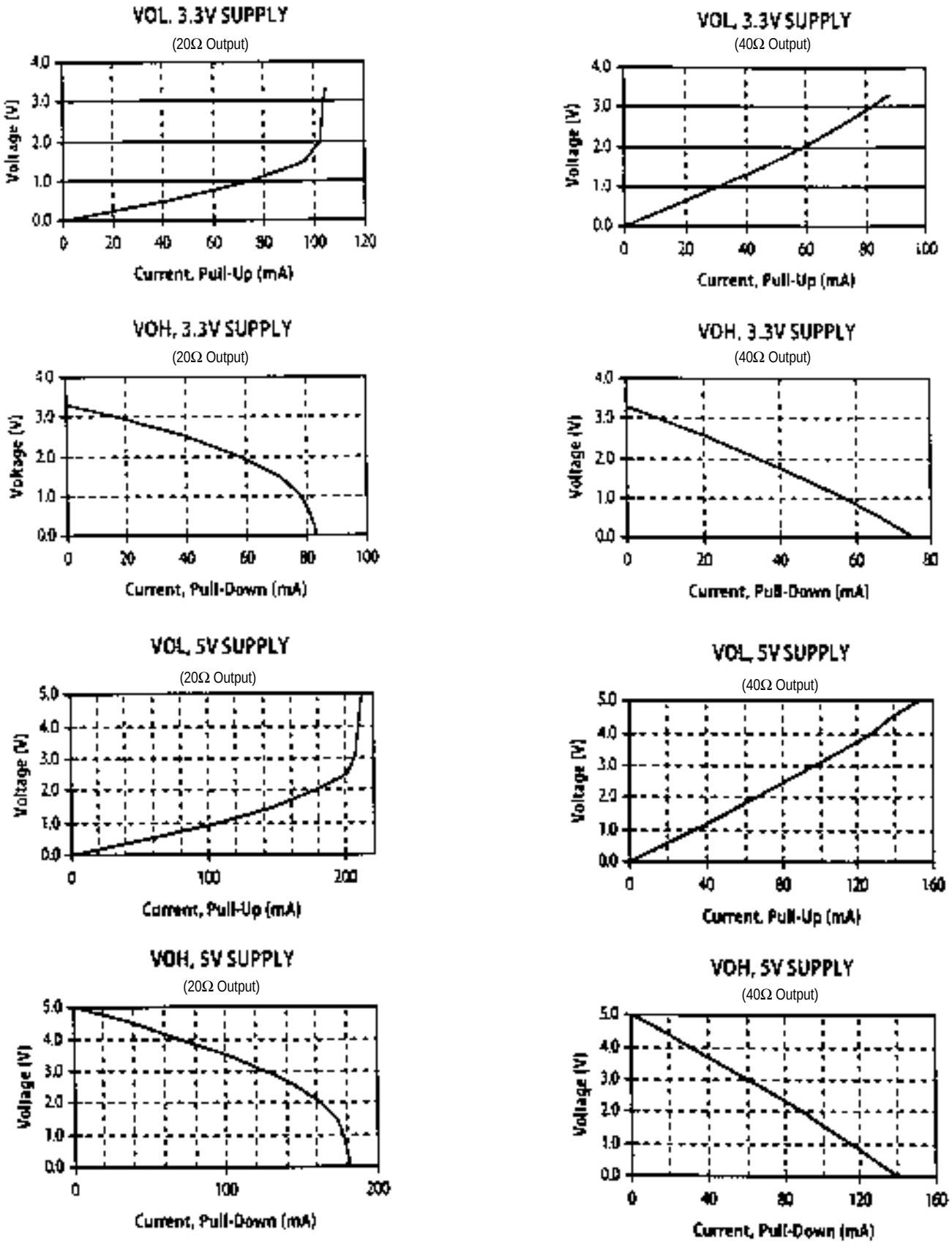
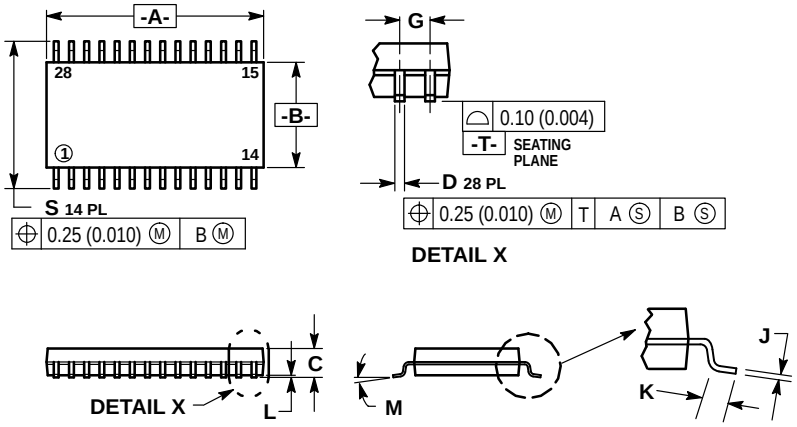


Figure 4. Typical Output V/I Characteristics for MPC9159

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751H–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.70	18.50	0.697	0.728
B	8.23	8.90	0.324	0.350
C	2.04	2.50	0.080	0.098
D	0.35	0.50	0.014	0.020
G	1.27 BSC		0.050 BSC	
J	0.14	0.25	0.0060	0.0098
K	0.40	1.27	0.016	0.050
L	0.05	0.20	0.002	0.008
M	0°	8°	0°	8°
S	11.50	12.10	0.453	0.476

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