Product Preview

Low-Voltage 1:9 Differential ECL/HSTL to HSTL Clock Driver

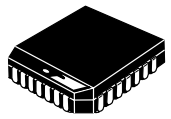
MPC911

LOW-VOLTAGE 1:9 DIFFERENTIAL ECL/HSTL TO HSTL CLOCK DRIVER

The MPC9111 is a low skew 1–to–9 differential HSTL compatible output fanout buffer. The device is functionally equivalent to the MC100LVE111 device. The device accepts either LVPECL or HSTL compatible input levels and provides 9 low skew differential HSTL compatible outputs. The device operates from a single 3.3V V_{CC} supply.

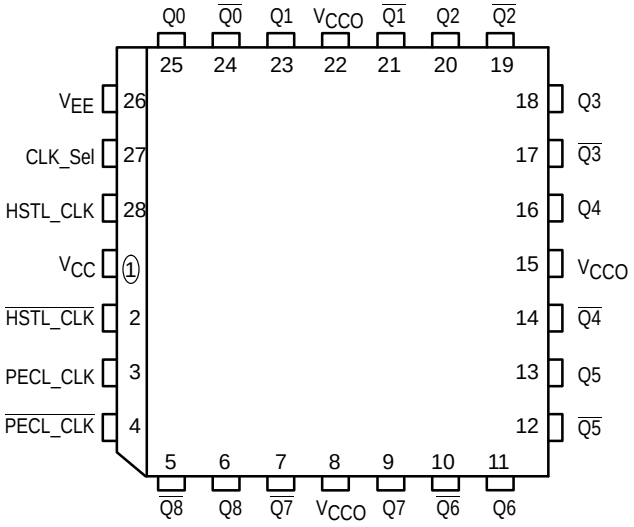
- 200ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Open Emitter HSTL Compatible Outputs
- Differential Design
- 28–Lead PLCC
- 3.3V V_{CC}

The MPC911 HSTL outputs are not realized in the conventional manner. To minimize part–to–part and output–to–output skew the HSTL compatible output levels are generated with an open emitter architecture. The outputs are pulled down with 50Ω to ground rather than the typical 50Ω to V_{DDQ} pullup of a “standard” HSTL output. The open emitter architecture allows for the realization of device skews which are competitive with Today’s ECL fanout buffers, skews which are an order of magnitude less than a CMOS transistors based buffer. Because the HSTL outputs are pulled to ground the MPC911 does not utilize the V_{DDQ} supply of the HSTL standard. The output levels are derived from V_{CC}, an internal regulator minimizes the output level variation with V_{CC} variations.



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



PIN NAMES

Pins	Function
HSTL_CLK, $\overline{\text{HSTL\_CLK}}$	Differential HSTL Input
PECL_CLK, $\overline{\text{PECL\_CLK}}$	Differential PECL Input
Q0–Q8, $\overline{\text{Q0}}$–$\overline{\text{Q8}}$	Differential Outputs

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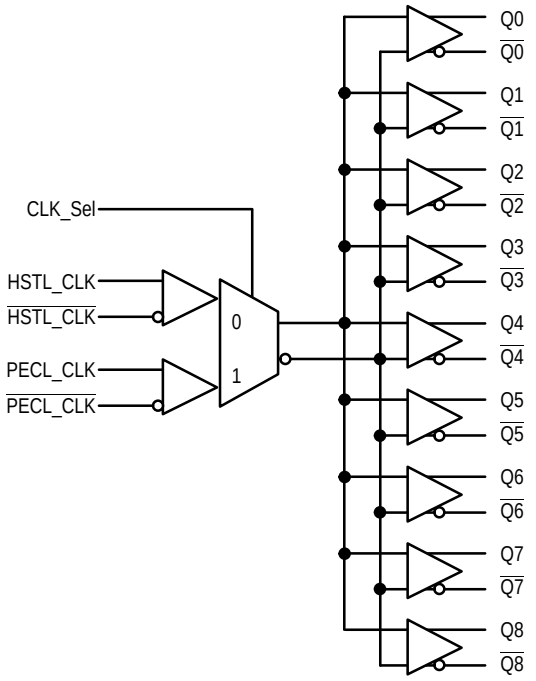
LOGIC SYMBOL



HSTL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	1.0			1.0			1.0			1.0			V
V_{OL}	Output LOW Voltage			0.4			0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{ref} + 0.10		1.9	V_{ref} + 0.10		1.9	V_{ref} + 0.10		1.9	V_{ref} + 0.10		1.9	V
V_{IL}	Input LOW Voltage	–0.3		V_{ref} – 0.10	–0.3		V_{ref} – 0.10	–0.3		V_{ref} – 0.10	–0.3		V_{ref} – 0.10	V
V_X	Input Crossover Volt	0.68		0.9	0.68		0.9	0.68		0.9	0.68		0.9	V
V_{ref}	Input Reference Volt	0.68		0.9	0.68		0.9	0.68	0.75	0.9	0.68		0.9	
I_{CC}	Power Supply Current													mA

LV PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{CC}	Power Supply Voltage	3.0		3.8	3.0		3.8	3.0		3.8	3.0		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{CC}	Power Supply Current													mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

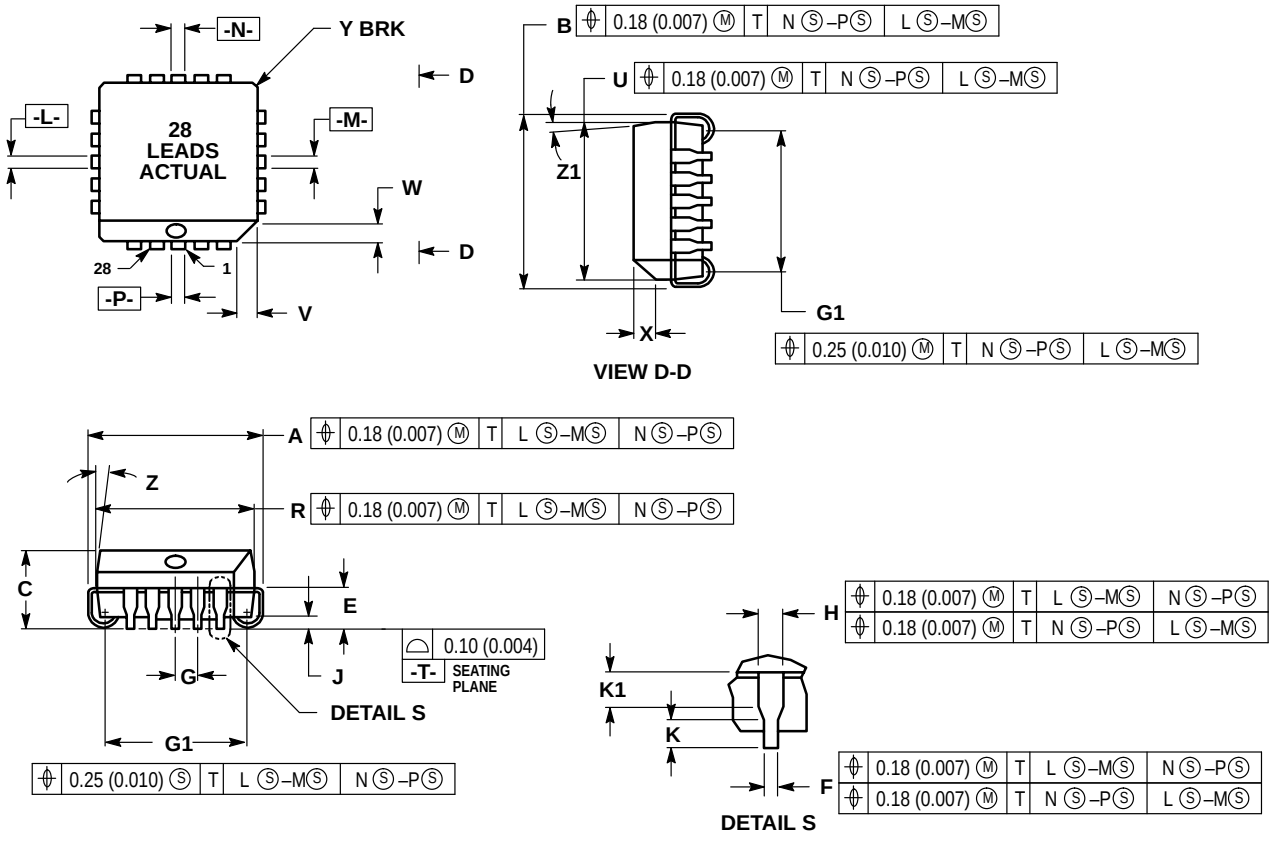
AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

		–40°C			0°C			25°C			85°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single-ended)		 1.2 1.2			 1.2 1.2			 1.2 1.2			 1.2 1.2		ns	 Note 1 Note 2
t_{skew}	Within-Device Skew Part-to-Part Skew (Diff)		50 200			50 200			50 200			50 200		ps	Note 3
V_{PP}	Minimum Input Swing PECL_CLK	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range PECL_CLK	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time		800			800			800			800		ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the MPC911 as a differential input as low as 50 mV will still produce full HSTL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02
ISSUE D



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 776-01 IS OBSOLETE, NEW STANDARD 776-02.

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