

## 1:6 PCI Clock Generator/ Fanout Buffer

The MPC903 and MPC904 are a six output clock generation devices targeted to provide the clocks required in a 3.3V or 5.0V PCI environment. The device operates from a 3.3V supply and can interface to either a TTL input or an external crystal. The inputs to the device can be driven with 5.0V when the  $V_{CC}$  is at 3.3V. The outputs of the MPC903/904 meet all of the specifications of the PCI standard. The two devices are identical except in the function of the Output Enables.

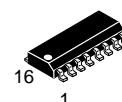
- Six Low Skew Outputs
- Synchronous Output Enables for Power Management
- Low Voltage Operation
- XTAL Oscillator Interface
- 16-Lead SOIC Package
- 5.0V Tolerant Enable Inputs

The MPC903/904 device is targeted for PCI bus or processor bus environments with up to 12 clock loads. Each of the six outputs on the MPC903/904 can drive two series terminated  $50\Omega$  transmission lines. This capability effectively makes the MPC903/904 a 1:12 fanout buffer.

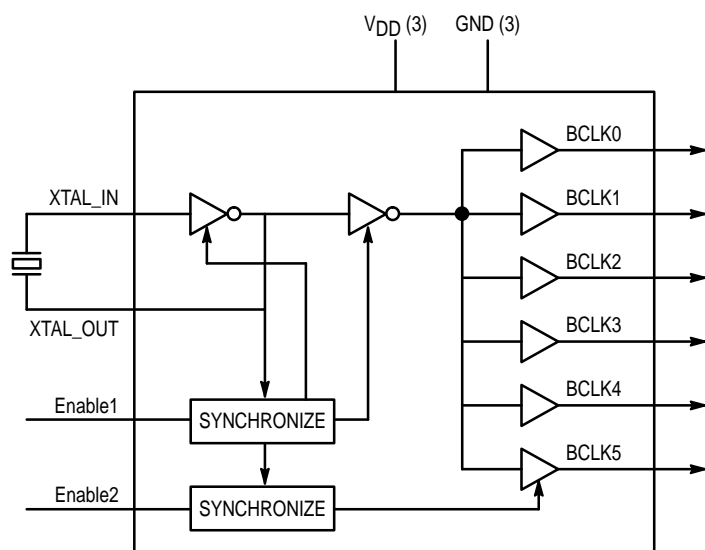
The MPC903 offers two synchronous enable inputs to allow users flexibility in developing power management features for their designs. Both enable signals are active HIGH inputs. A logic '0' on the Enable1 input will pull all of the outputs into the logic '0' state and shut down the internal oscillator for a zero power sleep state. A logic '0' on the Enable2 input will disable only the BCLK5 output. The Enable2 input can be used to disable any high power device for system power savings during periods of inactivity. Both enable inputs are synchronized internal to the chip so that the output disabling will happen only when the outputs are already LOW. This feature guarantees no runt pulses will be generated during enabling and disabling. Note that when the MPC903/904 is re-enabled via the Enable1 pin, the user must allow for the oscillator to regain stability. Thus, the re-enabling of the chip cannot occur instantaneously. The MPC904 Enable functions are slightly different than the 903 and are outlined in the function tables on the following page.

## MPC903 MPC904

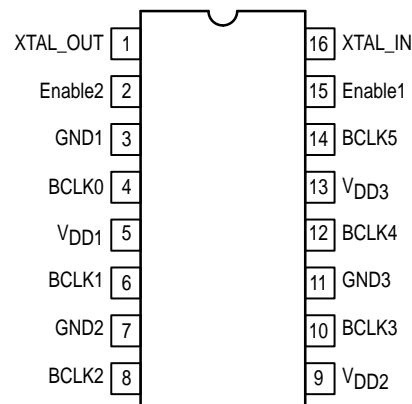
### 1:6 PCI CLOCK GENERATOR/ FANOUT BUFFER



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B-05



**Pinout: 16-Lead Plastic Package (Top View)**



## FUNCTION TABLE

ENABLE1	ENABLE2	Outputs 0 to 4		Output 5		OSC (On/Off)	
		MPC903	MPC904	MPC903	MPC904	MPC903	MPC904
0	0	LOW	LOW	LOW	LOW	OFF	OFF
0	1	LOW	LOW	LOW	TOGGLING	OFF	ON
1	0	TOGGLING	TOGGLING	LOW	LOW	ON	ON
1	1	TOGGLING	TOGGLING	TOGGLING	TOGGLING	ON	ON

## ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	4.6	V
V <sub>IN</sub>	Input Voltage	-0.5	V <sub>CC</sub> + 0.5	V
T <sub>oper</sub>	Operating Temperature Range	0	+70	°C
T <sub>stg</sub>	Storage Temperature Range	-65	+150	°C
T <sub>sol</sub>	Soldering Temperature Range (10 Sec)		+260	°C
T <sub>j</sub>	Junction Temperature Range		+125	°C
P(E1=1)	Power Dissipation		TBD	mW
P(E1=0)	Power Dissipation		40	μW
ESD	Static Discharge Voltage	2000		V
I <sub>Latch</sub>	Latch Up Current	50		mA

\* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T <sub>A</sub>	Ambient Temperature Range	0	70	°C
V <sub>DD</sub>	Positive Supply Voltage (Functional Range)	3.0	3.6	V
t <sub>DCin</sub>	T <sub>high</sub> (at XTAL_IN Input) T <sub>low</sub> (at XTAL_IN Input)	0.44T <sup>1</sup> 0.44T <sup>1</sup>	0.56T <sup>1</sup> 0.56T <sup>1</sup>	T = Period

<sup>1</sup> When using External Source for reference, requirement to meet PCI clock duty cycle requirement on the output.

DC CHARACTERISTICS (T<sub>A</sub> = 0–70°C; V<sub>DD</sub> = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V <sub>IH</sub>	High Level Input Voltage	2.0		5.5 <sup>2</sup>	V	
V <sub>IL</sub>	Low Level Input Voltage			0.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.4			V	I <sub>OH</sub> = -36mA <sup>1</sup>
V <sub>OL</sub>	Low Level Output Voltage			0.4	V	I <sub>OL</sub> = 36mA <sup>1</sup>
I <sub>IH</sub>	Input High Current			2.5 <sup>2</sup>	μA	
I <sub>IL</sub>	Input Low Current			2.5	μA	
I <sub>CC</sub>	Power Supply Current		20 37 78	45 95	μA mA mA	DC 33MHz 66MHz
C <sub>IN</sub>	Input Capacitance			9.0 4.5	pF	XTAL_IN Others

<sup>1</sup> The MPC903/904 outputs can drive series terminated or parallel terminated 50Ω (or 50Ω to V<sub>CC</sub>/2) transmission lines on the incident edge (see Applications Info).

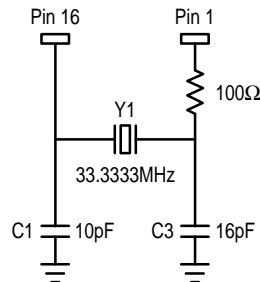
<sup>2</sup> XTAL\_IN input will sink up to 10mA when driven to 5.5V. There are no reliability concerns associated with the condition. Note that the Enable1 input must be a logic HIGH. Do not take the Enable1 input to a logic LOW with >V<sub>CC</sub> volts on the XTAL\_IN input.

**AC CHARACTERISTICS** ( $T_A = 0-70^{\circ}\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

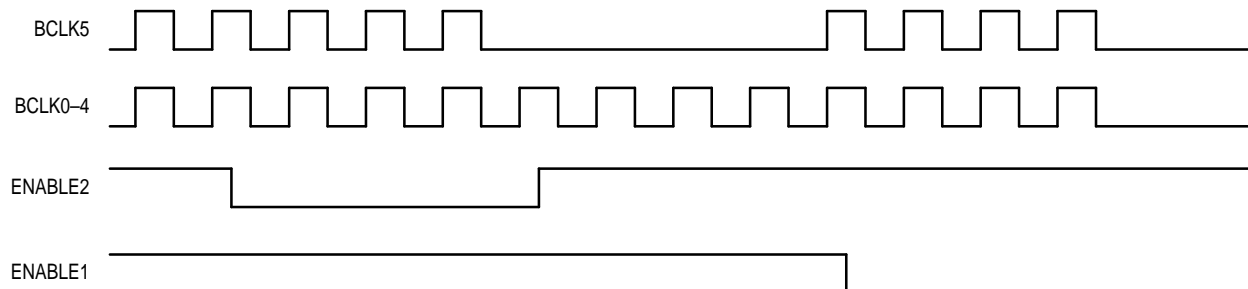
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$F_{\text{max}}$	Maximum Operating Frequency Using External Crystal Using External Clock Source	TBD DC		50 100	MHz	
$t_{\text{pw}}$	Output Pulse Width HIGH (Above 2.0V) LOW (Below 0.8V) HIGH (Above 2.0V) LOW (Below 0.8V)	$0.40T^1$ $0.40T^1$ $0.45T^2$ $0.45T^2$		$0.60T^1$ $0.60T^1$ $0.55T^2$ $0.55T^2$		$T = \text{Periods}$
$t_{\text{per}}$	Output Period	$T - 400\text{ps}$				$T = \text{Desired Period}$
$t_{\text{os}}$	Output-to-Output Skew Rising Edges Falling Edges			400 500	ps	
$t_r, t_f$	Rise/Fall Times (Slew Rate)	1		4	V/ns	Series Terminated Transmission Lines
$t_{\text{EN}}$	Enable Time Enable1 Enable2			5 4	ms Cycles	
$t_{\text{DIS}}$	Disable Time Enable1 Enable2			4 4	Cycles	
$A_{\text{osc}}$	XTAL_IN to XTAL_OUT Oscillator Gain	6			db	
Phase	Loop Phase Shift Modulo $360^{\circ} +$	30			Degrees	

1 Assuming input duty cycle specs from Recommended Operating Conditions table are met.

2 Assuming external crystal or 50% duty cycle external reference is used.



**Figure 1. Crystal Oscillator Interface**



**Figure 2. Enable Timing Diagram**

## APPLICATIONS INFORMATION

## Driving Transmission Lines

The MPC903/904 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than  $10\Omega$  the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a  $50\Omega$  resistance to  $VCC/2$ . This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC903/904 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel.

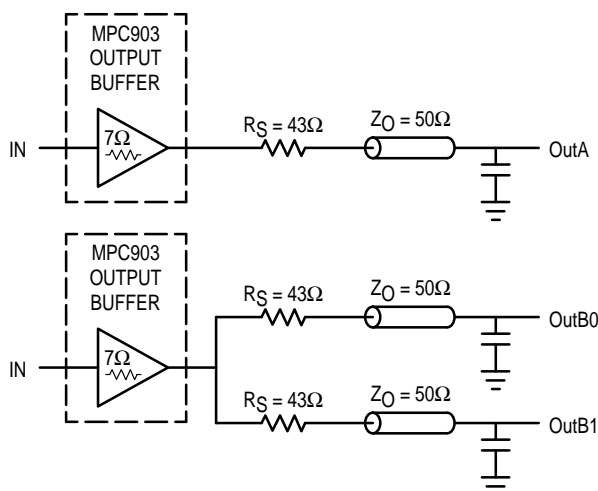


Figure 3. Single versus Dual Transmission Lines

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC903/904 output buffers is more than sufficient to drive  $50\Omega$  transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC903. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the  $43\Omega$  series resistor plus the output impedance does not match the parallel combination of the

line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / R_S + R_O + Z_0) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

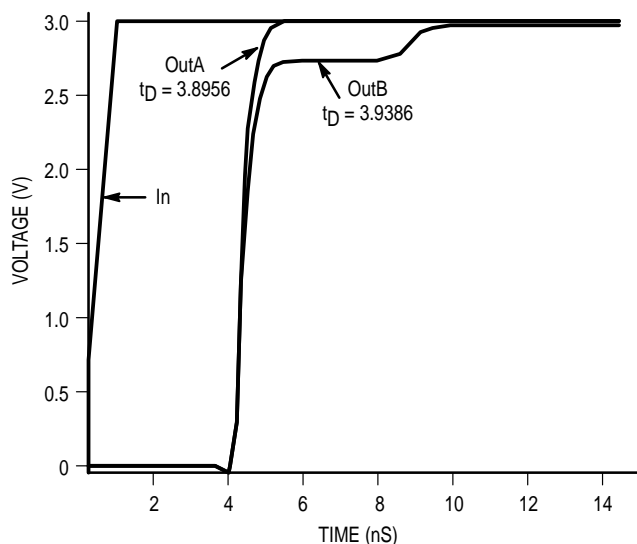


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

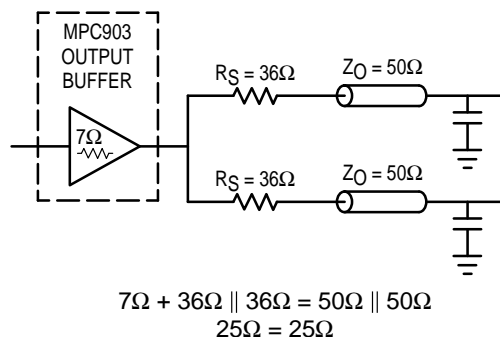
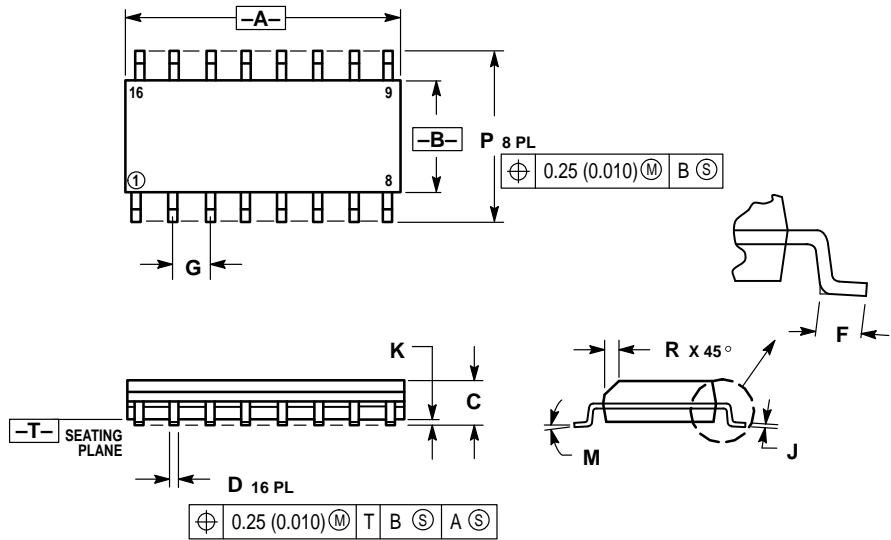


Figure 5. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.


OUTLINE DIMENSIONS

D SUFFIX  
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ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MPC903/D

