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by MPC2004/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MPC2004
MPC2005
MPC2011
MPC2012
MPC2014
MPC2015

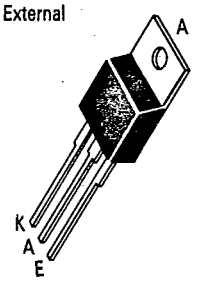
Advance Information

SMARTMOS™ Series Overvoltage/Overtemperature Protector Power Integrated Circuits

These protection circuits protect sensitive electronics from overvoltage transients and excessive temperature. They sense the fault condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limit/foldback, opening a fuse or tripping a circuit breaker.

7.5 AND 15 AMPERE OVERVOLTAGE AND OVERTEMPERATURE PROTECTOR 5, 12 AND 15 VOLTS

K — Cathode
A — Anode
E — External



CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	MPC 2004 2011 2014	MPC 2005 2012 2015	Unit
Anode-to-Cathode Voltage	V_{AK}	20		Vdc
Continuous Anode Current	I_A	7.5	15	Adc
Peak Capacitive Discharge Current (1)	I_{TM}	75	150	A
Circuit Fusing Considerations (T_J = 0 to 125°C, t = 1 to 8.3 ms)	I^2t	25	34	A^2S
Critical Rate-of-Rise of Current (2)	di/dt	100		A/μs
Operating Junction Temperature Range	T_J	0 to +125		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{AK} per Note 4 unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Anode-to-Cathode Voltage		V_{AK}	4	—	20	Vdc
Trip Voltage	MPC2004, MPC2005 MPC2011, MPC2012 MPC2014, MPC2015	V_{TRIP}	5.9 13 16.2	6.2 13.7 17.1	6.5 14.4 18	Vdc
Trip Temperature	All Types	T_{trip}	—	83	—	°C
External Trip Voltage		V_{EXT}	2.2	2.4	2.6	Vdc
Response Time		t_{rt}	—	2	3	μs
Quiescent Current (See Note 4)	MPC2004, MPC2005 MPC2011, MPC2012 MPC2014, MPC2015	I_Q	— — —	— — —	0.75 1 1.2	mA
Critical Rate-of-Rise of Off-State Voltage (See Note 4)	All Types	dv/dt	1	—	—	V/μsec
Average Temperature Coefficient of Trip Voltage		TCV_{TRIP}	—	0.06	—	%/°C

(1) Rating applies for t_w = 1 ms. t_w is defined as five time constants of an exponentially decaying current pulse.
(2) Test Conditions: V_{in} = V_{TRIP}, I_{TM} = Rated Value, T_J = 85°C.
(3) Consult factory for availability of devices which include thermal trip protection.
(4) V_{AK} = 5 V for MPC2004, 2005
V_{AK} = 12 V for MPC2011, 2012
V_{AK} = 15 V for MPC2014, 2015.

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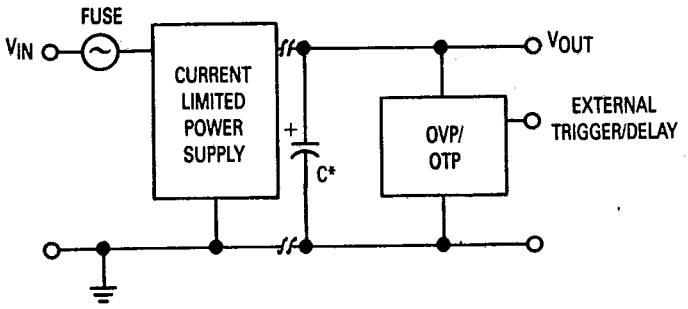
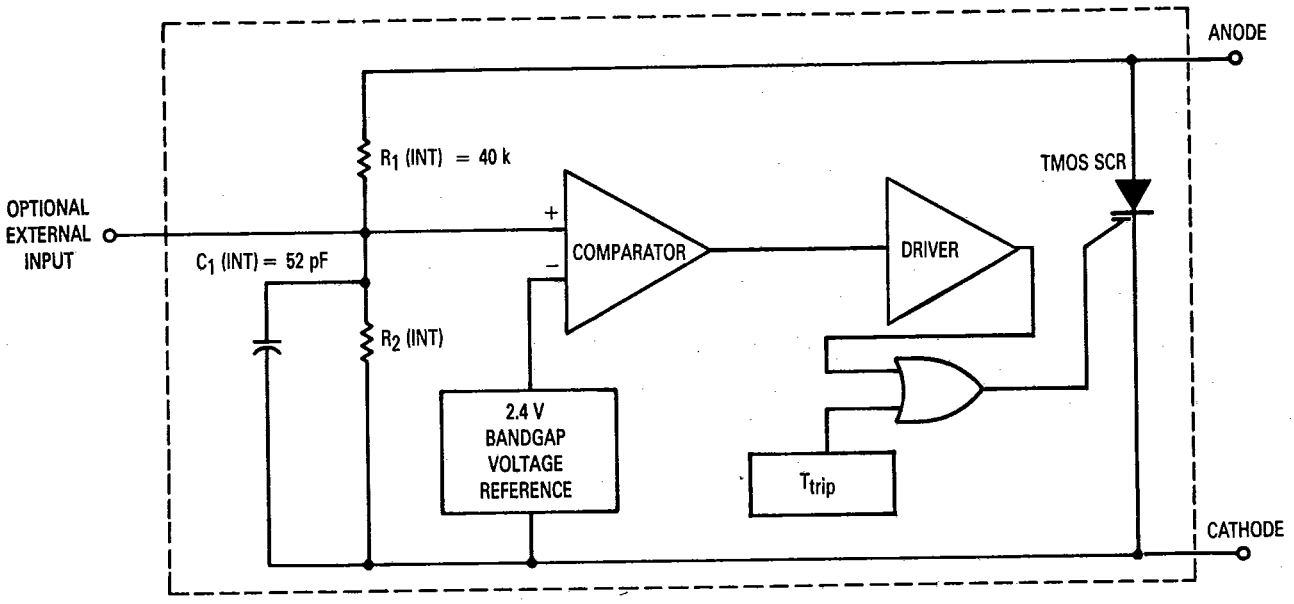
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA



*Use low ESL capacitor as close as possible to the OVP to minimize the effect of lead inductance.

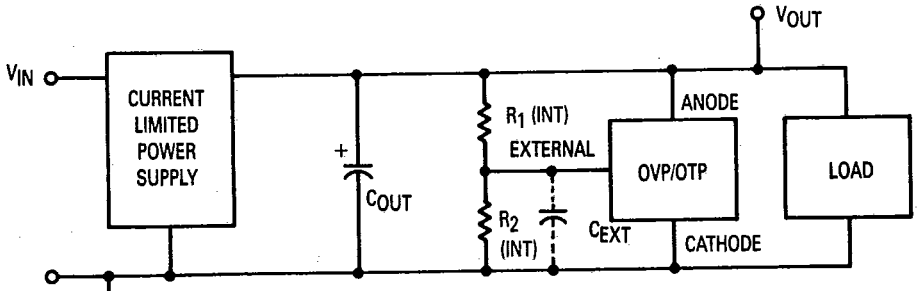
Figure 1. Typical Application



Device	R_2 (int)* (kΩ)
MPC2004, MPC2005	25
MPC2011, MPC2012	8
MPC2014, MPC2015	6.5

*Indicates nominal values.

Figure 2. Block Diagram



$$V_{TRIP} = \frac{2.4\ V\ [R_1\ (INT) + R_2\ (INT)]}{R_2\ (INT)}$$

; CHOOSE R_2 (INT) AND R_1 (INT) SMALLER THAN INTERNAL DIVIDER FOR ACCURATE TRIP VOLTAGES AND ONLY ADJUST TRIP VOLTAGE UP.

Figure 3. Typical Application — Changing the Trip Point

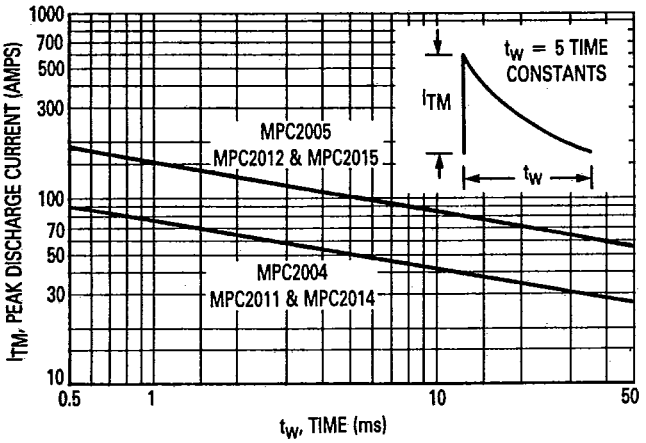


Figure 4. Peak Capacitor Discharge Current

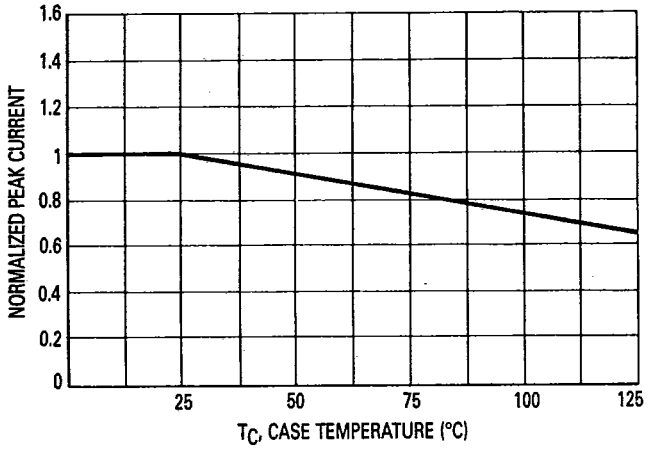


Figure 5. Peak Capacitor Discharge Current Derating

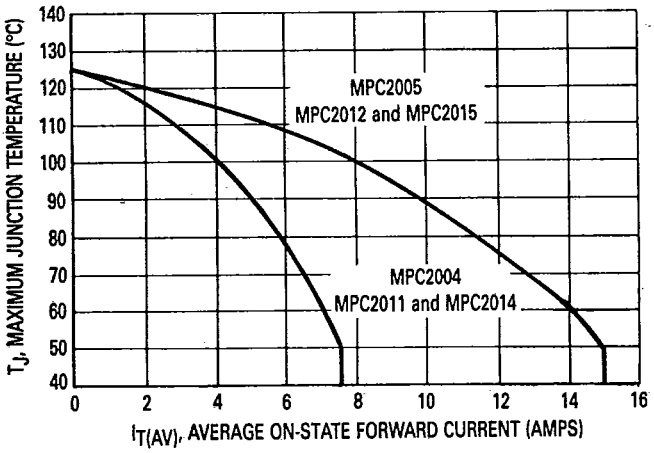


Figure 6. Average Current Derating

Note 1
High-Frequency noise spikes are usually present on output busses and long wires in systems having switching regulators or dc/dc converters. The devices are designed to roll off noise sensitivity at $f_s \sim 200$ kHz. If this is too high and noise is a problem of external capacitor (C_{EXT}) may be added to the external connection and the lower desired frequency (f_C) can be obtained by the following equation $C_{EXT} = [(R_1 + R_2)/(2 \pi f_C R_1 R_2)] - C_1$ (int).

Note 2
When the devices are activated in a typical application the TMOS SCR can be subjected to large current surges from the power supply capacitors. This surge current if excessive can cause TMOS SCR failure or degradation by one of three mechanisms: di/dt, absolute peak surge, or I^2t. It is recommended that the designer empirically determine optimum circuit resistance, inductance and capacitance coupled with device placement which result in reliable and effective operation.

Note 3
Additional operation and application of these OVPs can be found on Application Note AN956, which is available from the Literature Distribution Centers in the USA, Europe and Asia Pacific.

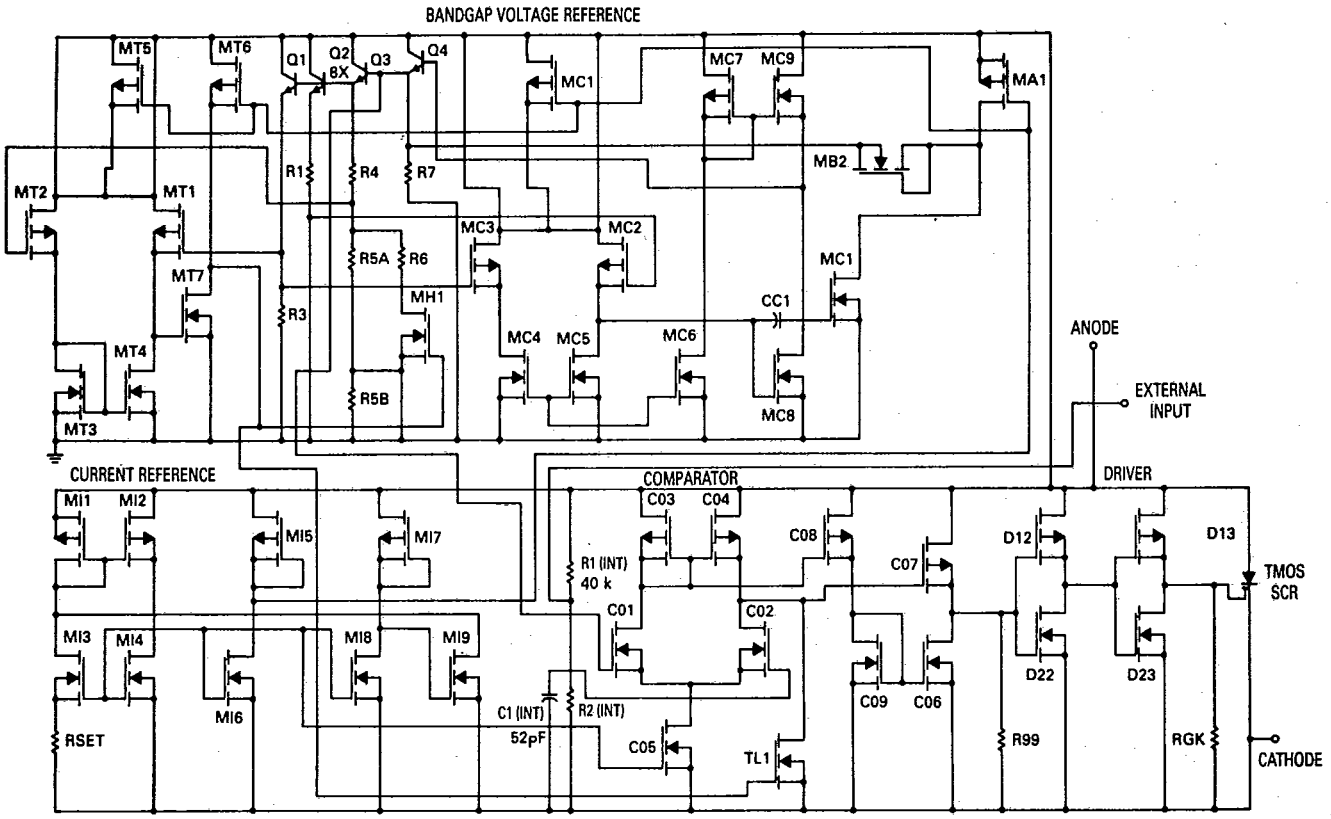
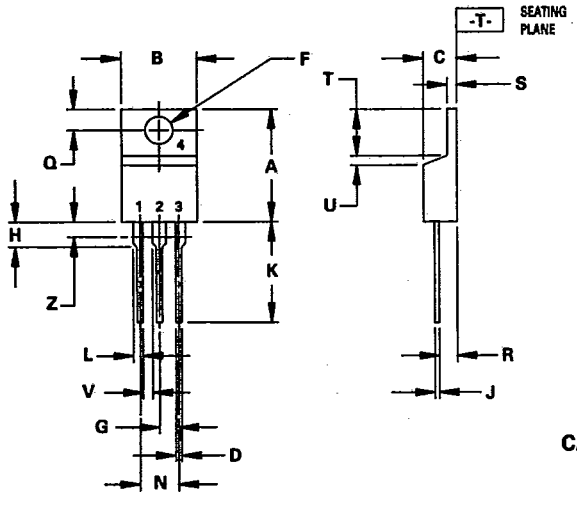


Figure 7. Circuit Diagram
Overvoltage Protector

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

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Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands Milton Keynes, MK145BP, England.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; P.O. Box 80300; Cheung Sha Wan Post Office; Kowloon Hong Kong.