

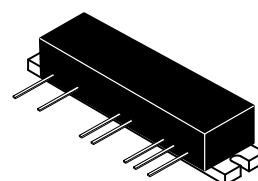
## The RF Line UHF Power Amplifiers

Designed specifically for portable radio applications. The MHW804 is capable of wide power range control, operates from a 7.5 volt supply and requires only 1.0 mW of RF input power.

- Specified 7.5 Volt Characteristics:
  - RF Input Power — 1.0 mW (0 dBm)
  - RF Output Power — 4.0 W
  - Minimum Gain — 36 dB
  - Harmonics — -45 dBc Max @ 2.0  $f_o$
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**MHW804-1**

**4.0 WATTS  
800 to 870 MHz  
RF POWER  
AMPLIFIERS**



**CASE 301F-03, STYLE 1**

### MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_s$	10	Vdc
DC Control Voltage	$V_{cont}$	4.0	Vdc
RF Input Power	$P_{in}$	5.0	mW
RF Output Power	$P_{out}$	6.0	W
Operating Case Temperature Range	$T_C$	- 30 to +100	°C
Storage Temperature Range	$T_{stg}$	- 30 to +100	°C

### ELECTRICAL CHARACTERISTICS ( $T_C = +25^\circ\text{C}$ , 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	800	870	MHz
Power Gain ( $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5} = 7.5\text{ V}$ ; $V_{cont} = 3.75\text{ V}$ )	$G_p$	36	—	dB
Control Voltage ( $P_{in} = 0\text{ dBm}$ , $P_{out} = 4.0\text{ W}$ , $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5} = 7.5\text{ V}$ , Adjust $V_{cont}$ for specified $P_{out}$ )	$V_{cont}$	—	3.75	Vdc
Efficiency (Same condition as for $V_{cont}$ )	$\eta$	32	—	%
Current Drain (Same conditions as for $V_{cont}$ )	$I_D$	—	210	mA
IS1 + IS4 (Pins 2, 5)		—	1430	
IS2 + IS3 + IS5 (Pins 3, 4, 6)		—	0.2	
$I_{control}$ (Pin 1)		—	—	
Input VSWR (Same conditions as for $V_{cont}$ )	$VSWR_{in}$	—	2.0:1	—
Harmonic Content (Same conditions as for $V_{cont}$ )		—	- 45	dBc
2.0 $f_o$		—	- 50	
3.0 $f_o$		—	—	
Leakage Current — $I_{s2} + I_{s3} + I_{s5}$ ( $V_{s2} = V_{s3} = V_{s5} = 7.5\text{ V}$ ; $V_{s1} = V_{s4} = 0\text{ V}$ , $V_{cont} = 0\text{ V}$ ; $P_{in} = 0\text{ mW}$ )	$I_L$	—	0.3	mA
Standby Current — $I_{s1} + I_{s4}$ ( $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5} = 7.5\text{ V}$ , $V_{cont} = 4.0\text{ V}$ ; $P_{in} = 0\text{ mW}$ )	$I_s$	—	220	mA
Load Mismatch Stress ( $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5} = 9.0\text{ V}$ ; $P_{in} = 2.0\text{ mW}$ ; $P_{out} = 6.0\text{ W}$ ; Load VSWR = 20:1, All Phase Angles. Adjust $V_{cont}$ for Specified $P_{out}$ )	$\psi$	No Degradation in Output Power		
Stability ( $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5} = 6.0\text{ to }9.0\text{ V}$ ; $P_{in} = -1.0\text{ dBm to }+3.0\text{ dBm}$ ; $P_{out} = 1.0\text{ W to }4.0\text{ W}$ ; Load VSWR = 6:1, All Phase Angles; Adjust $V_{cont}$ for Specified $P_{out}$ )	—	All Spurious Outputs More Than 60 dB Below Desired Signal		



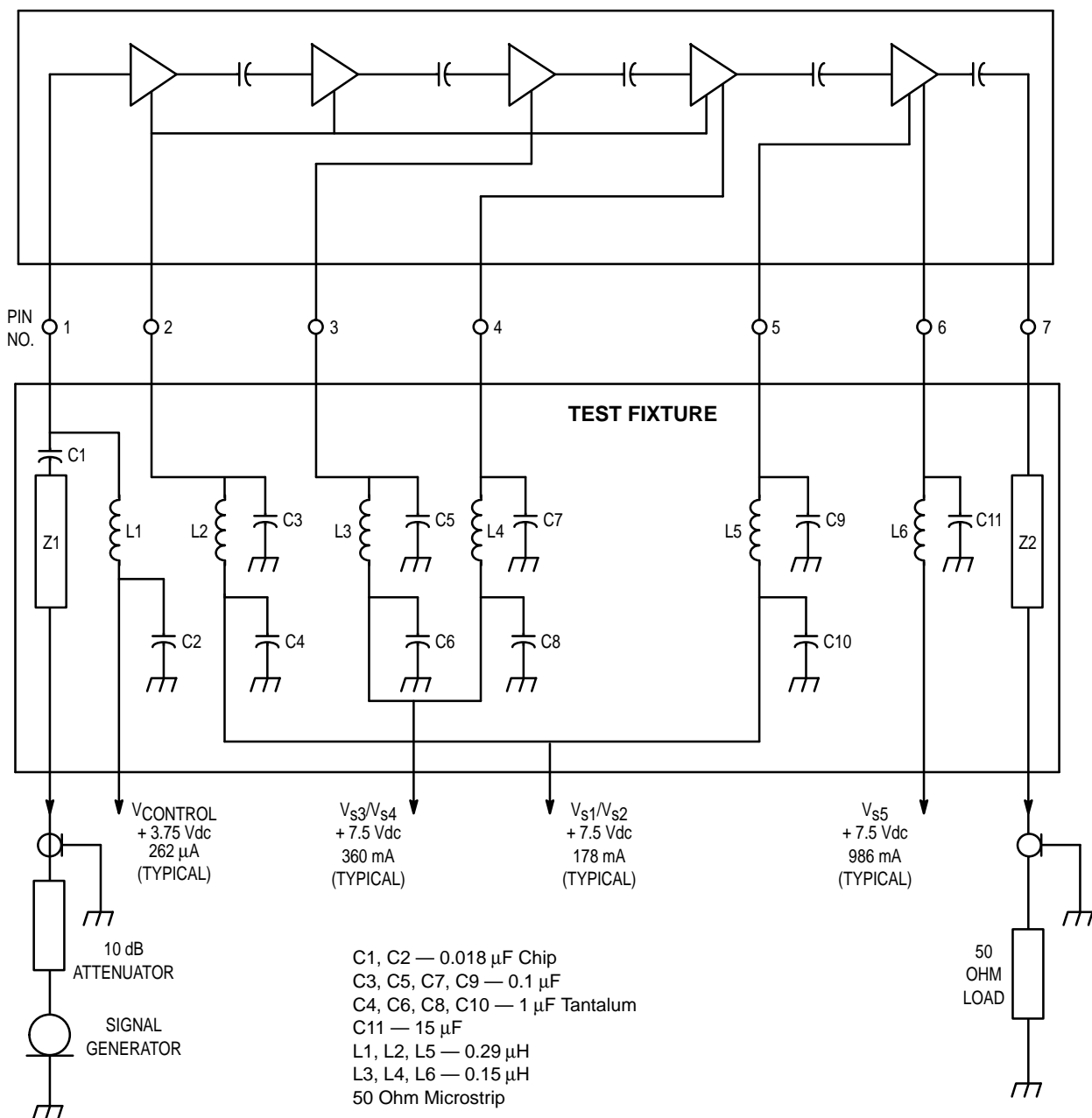
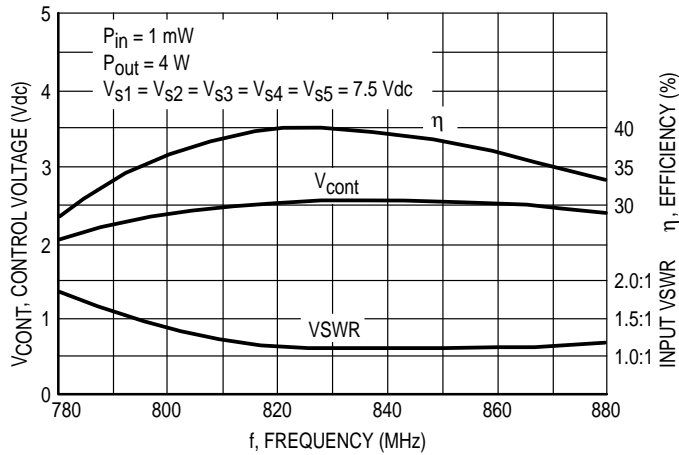
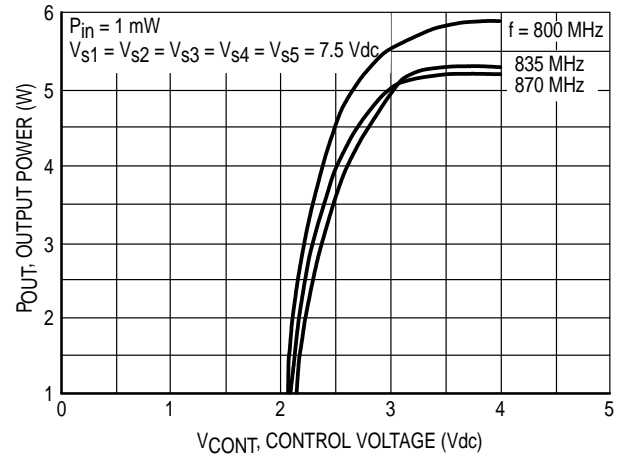


Figure 1. Power Module Test System Block Diagram

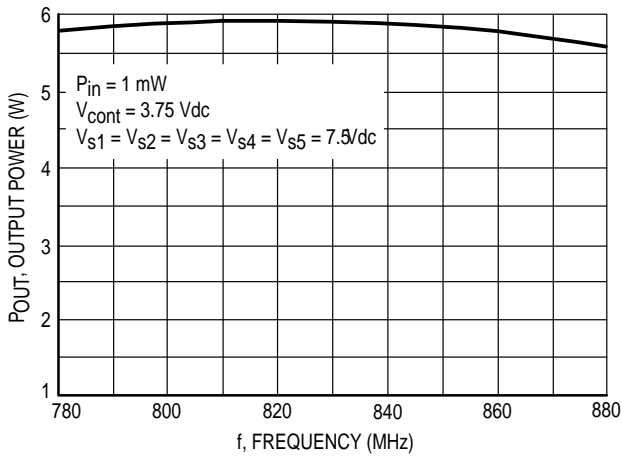
## TYPICAL CHARACTERISTICS



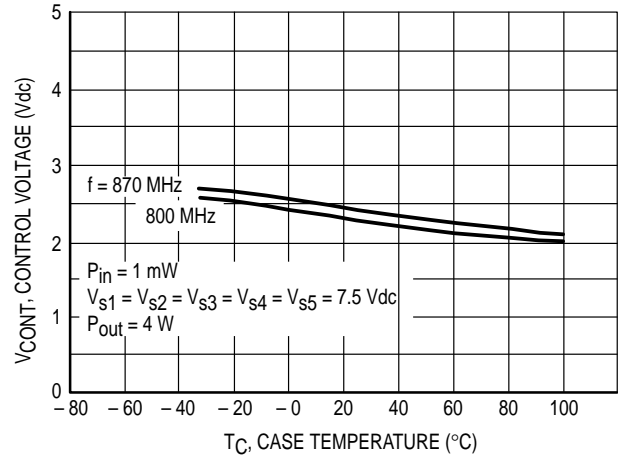
**Figure 2. Control Voltage, Efficiency and VSWR versus Frequency**



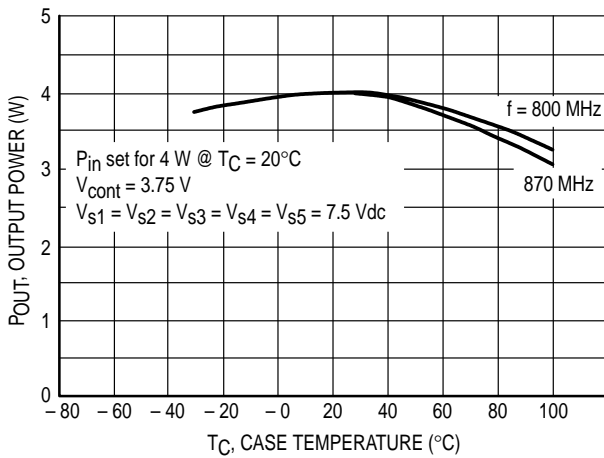
**Figure 3. Output Power versus Control Voltage**



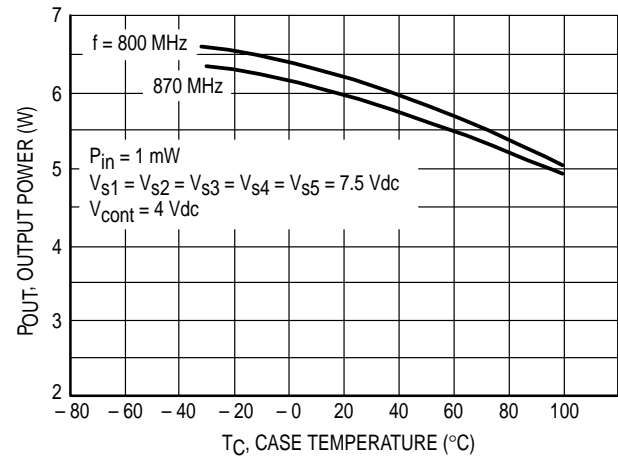
**Figure 4. Output Power versus Frequency**



**Figure 5. Control Voltage Case Temperature**



**Figure 6. Output Power versus Case Temperature**



**Figure 7. Output Power versus Case Temperature at Maximum Control Voltage**

## APPLICATIONS INFORMATION

### NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of  $V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = 7.5$  Vdc (Pins 2, 3, 4, 5, 6) and  $P_{Out}$  equal to 4.0 watts. With these conditions, maximum current density on any device is  $1.5 \times 10^5$  A/cm<sup>2</sup> and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

### GAIN CONTROL

The module output should be limited to 4.0 watts. The preferred method of power output control is to fix  $V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = 7.5$  Vdc (Pins 2, 3, 4, 5, 6),  $P_{In}$  (Pin 1) at 1.0 mW, and vary  $V_{Cont}$  (Pin 1) voltage.

### DECOUPLING

Due to the high gain of the four stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3, 4, and 6 are internally bypassed with a 0.018  $\mu$ F chip capacitor which is effective for frequencies from 5.0 MHz through 925 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

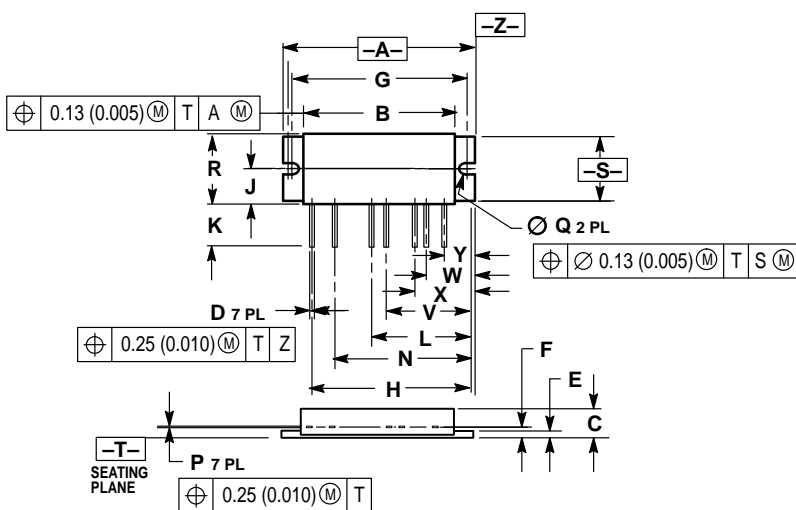
### LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are  $V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5}$  equal to 9.0 V, VSWR equal to 20:1, and output power equal to 6.0 watts.

## PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.380	2.395	60.46	6.083
B	1.970	1.990	50.04	50.54
C	0.250	0.265	6.35	6.73
D	0.018	0.022	0.46	0.55
E	0.085	0.100	2.16	2.54
F	0.132 BSC		3.35 BSC	
G	2.260 BSC		57.40 BSC	
H	2.042 BSC		51.87 BSC	
J	0.267	0.278	6.78	7.06
K	0.230	0.300	5.85	7.62
L	1.242 BSC		31.55 BSC	
N	1.742 BSC		44.25 BSC	
P	0.008	0.012	0.21	0.30
Q	0.120	0.130	3.05	3.30
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
V	1.142 BSC		29.01 BSC	
W	0.542 BSC		13.77 BSC	
X	0.642 BSC		16.31 BSC	
Y	0.342 BSC		8.69 BSC	

STYLE 1:

- PIN 1. RF INPUT/V CONT**
2. VS1
  3. VS2
  4. VS3
  5. VS4
  6. VS5

CASE: GROUND

**CASE 301F-03  
ISSUE C**

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**How to reach us:**

**USA / EUROPE:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,  
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**MFAX:** RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609  
**INTERNET:** <http://Design-NET.com>

**HONG KONG:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



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