MECL 10H
INTEGRATED CIRCUITS

MC10H100 SERIES
0 TO 75°C

Function Selection — (0 to +75°C)

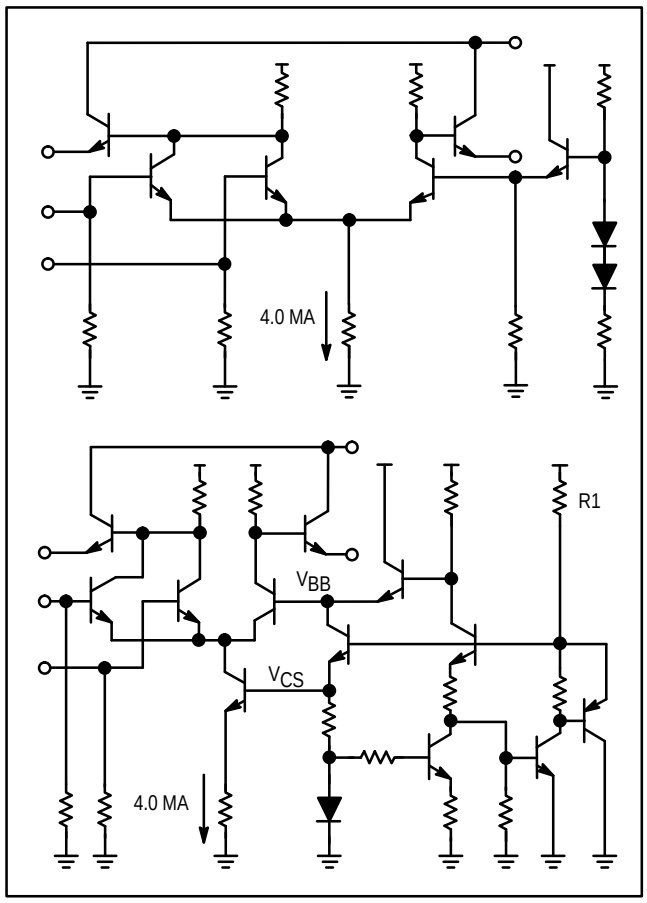
Function	Device	Case
NOR Gate		
Quad 2–Input with Strobe	MC10H100	620, 648, 775
Quad 2–Input	MC10H102	620, 648, 775
Triple 4–3–3 Input	MC10H106	620, 648, 775
Dual 3–Input 3–Output	MC10H211	620, 648, 775
OR Gate		
Quad 2–Input	MC10H103	620, 648, 775
Dual 3–Input 3–Output	MC10H210	620, 648, 775
AND Gates		
Quad AND	MC10H104	620, 648, 775
Complex Gates		
Quad OR/NOR	MC10H101	620, 648, 775
Triple 2–3–2 Input OR/NOR	MC10H105	620, 648, 775
Triple Exclusive OR/NOR	MC10H107	620, 648, 775
Dual 4–5 Input OR/NOR	MC10H109	620, 648, 775
Quad Exclusive OR	MC10H113	620, 648, 775
Dual 2–Wide OR–AND/OR–AND INVERT	MC10H117	620, 648, 775
4–Wide OR–AND/OR–AND INVERT	MC10H121	620, 648, 775
Hex Buffer w/Enable	MC10H188	620, 648, 775
Hex Inverter w/Enable	MC10H189	620, 648, 775
Translators		
Quad TTL to MECL	MC10H124	620, 648, 775
Quad MECL to TTL	MC10H125	620, 648, 775
Quad MECL–to–TTL Translator, Single Power Supply (–5.2 V or +5.0 V)	MC10H350	620, 648, 775
Quad TTL/NMOS to MECL Translator	MC10H351	732, 738, 775
Quad CMOS to MECL Translator	MC10H352	732, 738, 775
Quad TTL to MECL, ECL Strobe	MC10H424	620, 648, 775
9–Bit TTL–ECL Translator	MC10H/100H600	776
9–Bit ECL–TTL Translator	MC10H/100H601	776
9–Bit Latch/TTL–ECL Translator	MC10H/100H602	776
9–Bit Latch/ECL–TTL Translator	MC10H/100H603	776
Registered Hex TTL–ECL Translator	MC10H/100H604	776
Registered Hex ECL–TTL Translator	MC10H/100H605	776
Registered Hex TTL–PECL Translator	MC10H/100H606	776
Registered Hex PECL–TTL Translator	MC10H/100H607	776
Receivers		
Quad Line Receiver	MC10H115	620, 648, 775
Triple Line Receiver	MC10H116	620, 648, 751B, 775
Flip–Flop Latches		
Dual D Latch	MC10H130	620, 648, 775
Dual D Master Slave Flip–Flop	MC10H131	620, 648, 775
Dual J–K Master Slave Flip–Flop	MC10H135	620, 648, 775
Hex D Flip–Flop	MC10H176	620, 648, 775
Quint Latch	MC10H175	620, 648, 775
Hex D Flip–Flop w/Common Reset	MC10H186	620, 648, 775
Encoders Decoders		
Binary to 1–8 (Low)	MC10H161	620, 648, 775
Binary to 1–8 (High)	MC10H162	620, 648, 775
Dual Binary to 1–4 (Low)	MC10H171	620, 648, 775
Dual Binary to 1–4 (High)	MC10H172	620, 648, 775
8–Input Priority Encoder	MC10H165	620, 648, 775
Parity Checker		
12–Bit Parity Generator/Checker	MC10H160	620, 648, 775

Function	Device	Case
Transceivers		
4–Bit Differential ECL Bus to TTL Bus Transceiver	MC10/10H680	776
Hex ECL–TTL Transceiver w/Latches	MC10/10H681	776
Data Selector Multiplexer		
Quad Bus Driver/Receiver with 2–to–1 Output Multiplexers	MC10H330	758, 724, 776
Quad 2–Input Multiplexers (Noninverting)	MC10H158	620, 648, 775
Quad 2–Input Multiplexers (Inverting)	MC10H159	620, 648, 775
8–Line Multiplexer	MC10H164	620, 648, 775
Quad 2–Input Multiplexer Latch	MC10H173	620, 648, 775
Dual 4–1 Multiplexer	MC10H174	620, 648, 775
Counters		
Universal Hexadecimal	MC10H136	620, 648, 775
Binary Counter	MC10H016	620, 648, 775
Arithmetic Functions		
Look Ahead Carry Block	MC10H179	620, 648, 775
Dual High Speed Adder/Subtractor	MC10H180	620, 648, 775
4–Bit ALU	MC10H181	724, 758, 776
Special Function		
4–Bit Universal Shift Register	MC10H141	620, 648, 775
16 x 4 Bit Register File	MC10H145	620, 648, 775
5–Bit Magnitude Comparator	MC10H166	620, 648, 775
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738, 775
4–Bit ECL–TTL Load Reducing DRAM Driver	MC10H/100H660	776
Memories		
16 x 4 Bit Register File	MC10H145	620, 648, 775
Bus Driver (25 ohm outputs)		
Triple 4–3–3 Input Bus Driver (25 Ohms)	MC10H123	620, 648, 775
Quad Bus Driver/Receiver with 2–to–1 Output Multiplexers	MC10H330	724, 758, 776
Dual Bus Driver/Receiver with 4–to–1 Output Multiplexers	MC10H332	732, 738, 775
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738, 775
OR/NOR Gate		
Dual 4–5 Input OR/NOR Gate	MC10H209	620, 648, 775
Clock Drivers		
68030/40 ECL–TTL Clock Driver	MC10/100H640	776
Single Supply PECL–ECL 1:9 Clock Distribution	MC10/100H641	776
68030/40 ECL–TTL Clock Driver	MC10/100H642	776
Dual Supply ECT–TTL 1:8 Clock Driver	MC10/100H643	776
68030/40 PECL–TTL Clock Driver	MC10/100H644	775
1:9 TTL Clock Driver	MC10H645	776
PCL–TTL–TTL 1:8 Clock Distribution Chip	MC10/100H646	776

MECL 10H INTRODUCTION

Motorola's MECL 10H family features 100% improvement in propagation delay and clock speeds while maintaining power supply current equal to MECL 10K. This MECL family is voltage compensated which allows guaranteed dc and switching parameters over a ±5% power supply range. Noise margins of MECL 10H are 75% better than the MECL 10K series over the ±5% power supply range. MECL 10H is compatible with MECL 10K and MECL III, a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pinout/functional duplications of the MECL 10K series devices.

FIGURE 1 — MECL 10K versus MECL 10H GATE DESIGN



The schematics in Figure 1 compare the basic gate structure of the MECL 10H to that of MECL 10K devices. The gate switch current is established with a current source in the MECL 10H family as compared to a resistor source in MECL 10K. The bias generator in the MECL 10K device has been replaced with a voltage regulator in the MECL 10H series. The advantages of these design changes are: current–sources permit–matched collector resistors that yield correspondingly better matched delays, less variation in the output–voltage level with power supply changes, and matched output–tracking rates with temperature. These circuit changes increase complexity at the gate level; however, the added performance more than compensates.

The MECL 10H family is being fabricated using Motorola's MOSAIC I (Motorola Oxide Self Assigned Implanted Circuits). The switching transistor's geometries obtained in the MOSAIC I process show a two–fold improvement in fτ, a reduction of more than 50% in parasitic capacitance and a decrease in device area of almost 76%.

FIGURE 2 — MOSAIC versus MECL 10K SWITCHING TRANSISTOR GEOMETRY

With improved geometry, the MECL10H switching transistors (left) are one–seventh the size of the older MECL 10K transistors (right). Along with the smaller area comes an improved f_T and reduced parasitic capacitances.

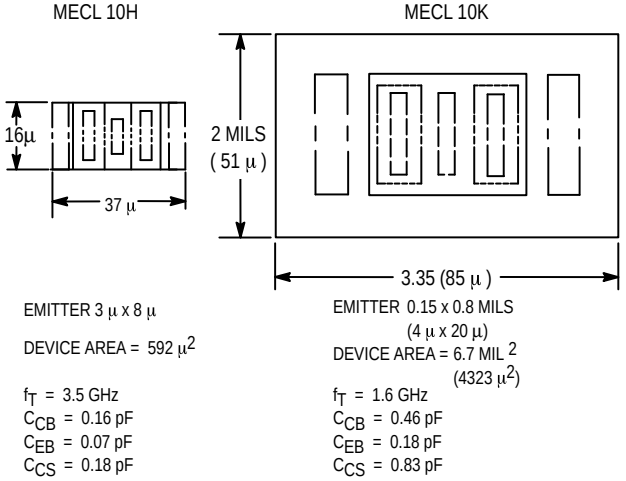


Figure 2 illustrates the relative size difference between the junction isolated transistor of MECL 10K and the MOSAIC I transistor of MECL 10H. This suggests that performance could be improved twofold at lower power levels. However, at the gate level, the power of the output transistor cannot be reduced without sacrificing output characteristics because of the 50 ohm drive requirements of MECL. In more complex functions, where part of the delay is associated with internal gates, MECL 10H devices use less power than the equivalent MECL 10K devices and provide an even more significant improvement in ac performance.

Table 1. — TYPICAL FAMILY CHARACTERISTICS FOR 10K AND 10H CIRCUITS

	10K	10H
Propagation delay (ns)	2.0	1.0
Power (mW)	25	25
Power–speed product (pJ)	50	25
Rise/fall times (ns) (20–80%)	2.0	1.0
Temperature range (°C)	–30 to +85	0 to +75
Voltage regulated	No	Yes
Technology	Junction isolated	Oxide isolated
V_{EE} = –5.2 V		

Supply & Temperature Variation

MECL 10H temperature and voltage compensation is designed to guarantee compatibility with MECL 10K, MECL III, MECL Memories and the MC10900 and Macrocell Array products. Table 1 summarizes some performance characteristics of the MECL 10K and 10H logic families in a 16–pin DIP. The MECL 10H devices offer typical propagation delays of 1.0 ns at 25 mW per gate when operated from a V_{EE} of –5.2 V. The resulting speed–power product of 25 picojoules is one of the best of any ECL logic family available today.

The operating temperature range is changed from –30°C to +85°C of the MECL 10K family to the narrower range of 0°C to 75°C for MECL 10H. This change matches the constraints established by the memory and array products. Operation at –30°C would require compromises in performance and power. With few exceptions, commercial applications are satisfied by 0°C min.

Table 2. — MECL 10H AC SPECIFICATIONS AND TRACKING

Parameter		0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	75°C Min	75°C Typ	75°C Max	Units
t_{PD}			0.4	1.0	1.5	0.4	1.0	1.6	0.4	1.0	1.7	ns
		Min		Max	Min		Max	Min		Max	
t_R (20–80%)		0.5		1.5	0.5		1.6	0.5		1.7	ns
t_F (20–80%)		0.5		1.5	0.5		1.6	0.5		1.7	ns
V_{EE} = –5.2 V ±5%											
Parameter		Propagation delay (ns)*			Delay variation vs temp (ps/°C)			Delay variation vs supply (ps/V)			
		Typ		Max	Typ		Max	Typ			Max
t_{PD}	10K	2.0		2.9	2.0		7.0	80			
	10H	1.0		1.5	0.5		4.0	0			0

*V_{EE} = –5.2 V, Temp = 25°C

AC specifications of MECL 10H products appear in Table 2. In the MECL 10H family, all ac specifications have guaranteed minimums and maximums for extremes of both temperature and supply — a first in ECL logic. In addition, flip flops, latches and counters will have guaranteed limits for setup time, hold time, and clock pulse width. The limits in Table 2 are guaranteed for a power supply variation of ±5%. MECL 10K typically has a propagation delay (t_{PD}) variation of 80 ps/V with no guaranteed maximum. The typical variation in t_{PD} for MECL 10H circuits is only 38 ps typically over the entire specified temperature range and power–supply tolerance, and is guaranteed not to exceed 300 ps.

The improved performance in temperature over MECL 10K are a result of the internal voltage regulator. The primary difference being the flatter tracking rate of the output “0” level voltage (V_{OL}). This difference does not affect the compatibility with existing MECL families.

Changes in output “1” level voltages (V_{OH}) with supply variations are 10 mV/V less for the MECL 10H family. V_{OH} varies with the supply, primarily because of changes in chip temperature caused by the changes in power dissipation. However, the current in the MECL 10H circuits remains almost constant with supply changes, since the circuits are voltage compensated and use current sources for all internal emitter followers. Threshold voltage (V_{BB}) and output “0” level voltage (V_{OL}) variations are shown with respect to MECL 10K in Table 3. In both cases voltage compensation has reduced the variations significantly.

Table 3. — LOGIC LEVEL DC TRACKING RATE FOR 10K AND 10H CIRCUITS

		Min	Typ	Max
$\Delta V_{OH}/\Delta T$ (mV/°C)	10H	1.2	1.3	1.5
	10K	1.2	1.3	1.5
$\Delta V_{BB}/\Delta T$ (mV/°C)	10H	0.8	1.0	1.2
	10K	0.8	1.0	1.2
$\Delta V_{OL}/\Delta T$ (mV/°C)	10H	0	0.4	0.6
	10K	0.35	0.5	0.75
		0.75	1.0	1.55
$\Delta V_{OH}/\Delta V_{EE}$ (mV/V)	10H	–20		0
	10K	–30		0
$\Delta V_{BB}/\Delta V_{EE}$ (mV/V)	10H	0	10	25
	10K	110	150	190
$\Delta V_{OL}/\Delta V_{EE}$ (mV/V)	10H	0	20	50
	10K	200	250	320

Noise Margin Considerations

Specification of input voltage levels (V_{IHA}, V_{ILA}) are changed from those of MECL 10K resulting in improved noise margins for MECL 10H.

The MECL 10K circuits have two sets of output voltage specifications (V_{OH}, V_{OHA}, and V_{OL}, V_{OLA}). The first output voltage specification in each set (V_{OH} and V_{OL}) are guaranteed maximum and minimum output levels for typical input levels. The second specification in each set (V_{OHA} and V_{OLA}) is the guaranteed worst–case output level for input threshold voltages. System analysis for worst–case noise margin considers V_{OHA} and V_{OLA} only. The MECL 10H family has only one set of output voltages (V_{OH} and V_{OL}) with minimum and maximum values specified. The minimum value of V_{OH} and the maximum value for V_{OL} of the MECL 10H family is synonymous with the V_{OHA} and V_{OLA} specifications of MECL 10K family.

The V_{OH} values for the MECL 10H circuits are equal to or better than the MECL 10K levels at all temperatures. Input threshold voltages (V_{IHA} and V_{ILA}, which are synonymous with $V_{IH\ min}$ and $V_{IL\ max}$ for 10H) are also improved and

Table 4. — NOISE MARGIN versus POWER–SUPPLY CONDITIONS

Parameter		V_{EE} –10% Typ	V_{EE} –10% Min	V_{EE} –5% Typ	V_{EE} –5% Min	V_{EE} Typ	V_{EE} Min	V_{EE} +5% Typ	V_{EE} +5% Min
Noise Margin High	10H	224	150	227	150	230	150	233	150
V_{NH} (mV)	10K	127	47	166	86	205	125	241	164
Noise Margin Low	10H	264	150	267	150	270	150	273	150
V_{NL} (mV)	10K	223	103	249	129	275	155	301	181

*Temp = 0 to 75°C

guaranteed V_{IHA} has been decreased by 25 mV over the entire operating temperature range, resulting in a “1” level noise margin of 150 mV (compared to 125 mV for MECL 10K circuits). V_{ILA} has been decreased by 5.0 mV, providing a “0” level noise margin equal to the “1” level noise margin. The V_{OL} minimum of the MECL 10H is more negative than for MECL 10K (–1950 mV instead of –1850 mV). The V_{OL} level for the MECL 10K family was selected to ensure that the gate would not saturate at high temperatures and high supply voltages. The reduction in operating temperature range for the MECL 10H family and the improvement in tracking rate allow the lower V_{OL} level. The change in this level does not affect system noise margins. Although some of the interface levels change with temperature, the changes in voltage levels are well within the tolerance ranges that would keep the families compatible. Table 4 lists some noise margins for V_{EE} supply variations.

The compatibility of MECL 10H with MECL 10K may be demonstrated by applying the tracking rates in Table 3 to the dc specifications. The method for determining compatibility is to show acceptable noise margins for MECL 10H, MECL 10K and mixed MECL 10K/MECL 10H systems. The assumption is that the families are compatible if the noise margin for a mixed system is equal to or better than the same system using only the MECL 10K series.

Using an all MECL 10K system as a reference, three possible logic mixes must be considered: MECL 10K driving MECL 10H; MECL 10H driving MECL 10K; and MECL 10H driving MECL 10H. The system noise margin for the three configurations can now be calculated for the following cases (See Figure 3):

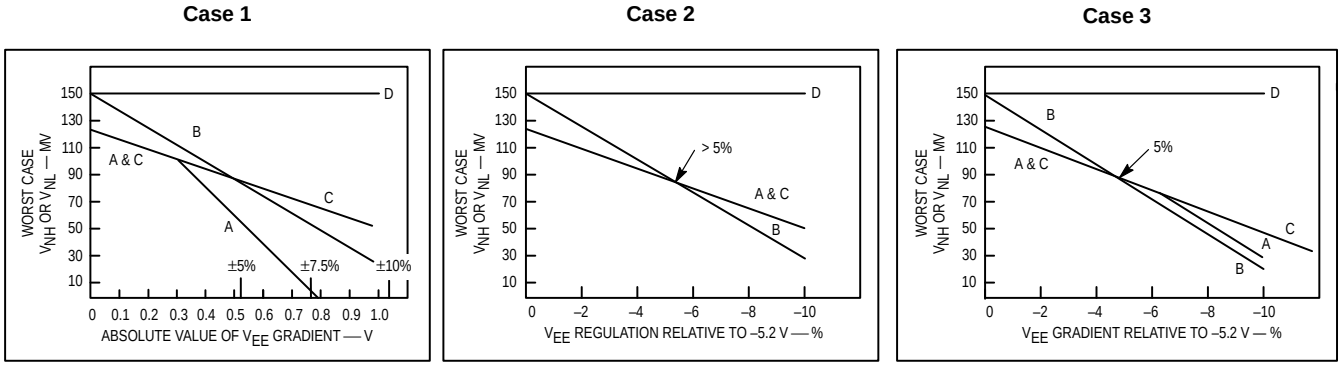
In Case 1, the system uses multiple power supplies, each independently voltage regulated to some percentage tolerance. Worst–case is where one device is at the plus extreme and the other device is at the minus extreme of the supply tolerance.

In Case 2, a system operates on a single supply or several supplies slaved to a master supply. The entire system can drift, but all devices are at the same supply voltage.

In Case 3, a system has excessive supply drops throughout. Supply gradients are due to resistive drops in V_{EE} bus.

The analysis indicates that the noise margins for a MECL 10K/10H system equal or exceed the margins for an all 10K system for supply tolerance up to ±5%. The results of the analysis are shown in Figure 3.

FIGURE 3 — NOISE MARGIN versus POWER–SUPPLY VARIATION



A. MECL 10K DRIVING MECL 10K B. MECL 10K DRIVING MECL 10H C. MECL 10H DRIVING MECL 10K D. MECL 10H DRIVING MECL 10H