# MCM6926

*Product Preview*

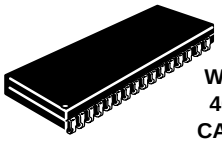
# 128K x 8 Bit Fast Static Random Access Memory

The MCM6926 is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

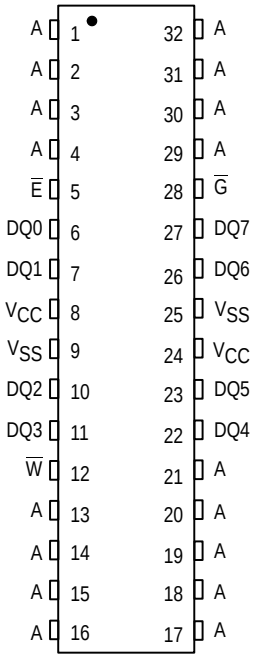
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS



**WJ PACKAGE**
**400 MIL SOJ**
**CASE 857A–02**

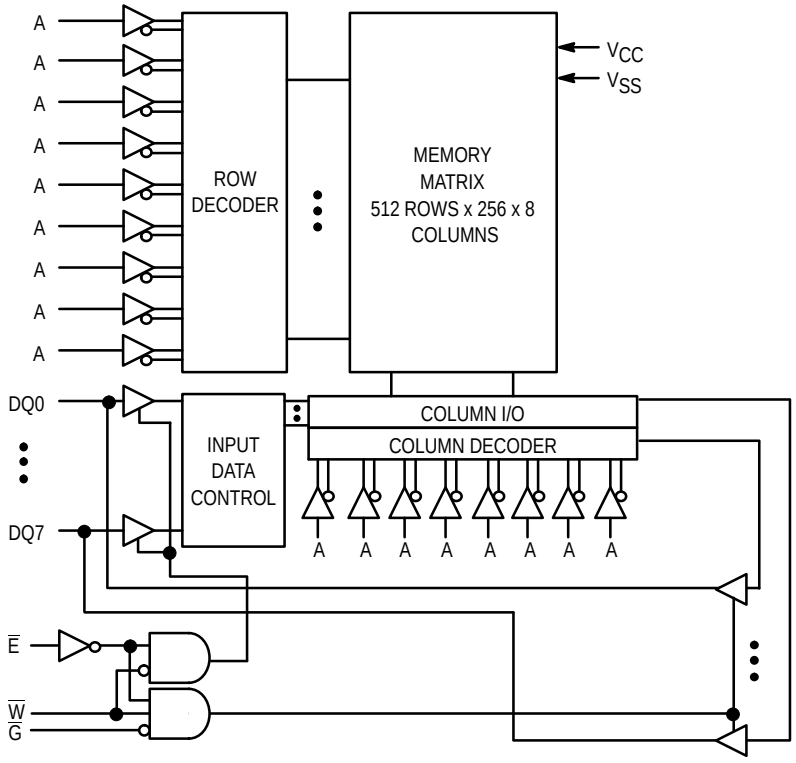
**PIN ASSIGNMENT**




**PIN NAMES**

| | |
|---|---|
| A0 – A16 | Address Input |
| $\overline{E}$ | Chip Enable |
| $\overline{W}$ | Write Enable |
| $\overline{G}$ | Output Enable |
| DQ0 – DQ7 | Data Input/Output |
| $V_{CC}$ | + 3.3 V Power Supply |
| $V_{SS}$ | Ground |

**BLOCK DIAGRAM**




This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

**REV 1**
**1/2/96**



MOTOROLA

**TRUTH TABLE** (X = Don't Care)

| $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | Mode | $V_{CC}$ Current | Output | Cycle |
|---|---|---|---|---|---|---|
| H | X | X | Not Selected | $I_{SB1}$, $I_{SB2}$ | High–Z | — |
| L | H | H | Output Disabled | $I_{CCA}$ | High–Z | — |
| L | L | H | Read | $I_{CCA}$ | $D_{out}$ | Read Cycle |
| L | X | L | Write | $I_{CCA}$ | High–Z | Write Cycle |

**ABSOLUTE MAXIMUM RATINGS** (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | – 0.5 to + 4.6 | V |
| Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$ | $V_{in}$, $V_{out}$ | – 0.5 to $V_{CC}$ + 0.5 | V |
| Output Current | $I_{out}$ | ± 30 | mA |
| Power Dissipation | $P_D$ | 0.6 | W |
| Temperature Under Bias | $T_{bias}$ | – 10 to + 85 | °C |
| Operating Temperature | $T_A$ | 0 to + 70 | °C |
| Storage Temperature — Plastic | $T_{stg}$ | – 55 to + 125 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 3.3 V + 10%, – 5%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$ | 3.135 | 3.3 | 3.6 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.3** | V |
| Input Low Voltage | $V_{IL}$ | – 0.5* | — | 0.8 | V |

* $V_{IL}$ (min) = –0.5 V dc; $V_{IL}$ (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** $V_{IH}$ (max) = $V_{CC}$ + 0.3 V dc; $V_{IH}$ (max) = $V_{CC}$ + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

**DC CHARACTERISTICS**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Leakage Current (All Inputs, $V_{in}$ = 0 to $V_{CC}$) | $I_{lkg(I)}$ | — | ± 1.0 | µA |
| Output Leakage Current ($\overline{E}$ = $V_{IH}$, $V_{out}$ = 0 to $V_{CC}$) | $I_{lkg(O)}$ | — | ± 1.0 | µA |
| Output Low Voltage ($I_{OL}$ = + 8.0 mA) | $V_{OL}$ | — | 0.4 | V |
| Output High Voltage ($I_{OH}$ = – 4.0 mA) | $V_{OH}$ | 2.4 | — | V |

**POWER SUPPLY CURRENTS** (See Note 1)

| Parameter | Symbol | 6926–8 | | 6926–10 | | 6926–12 | | 6926–15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Max | Typ | Max | Typ | Max | Typ | Max | | |
| AC Active Supply Current ($I_{out}$ = 0 mA) ($V_{CC}$ = max, f = $f_{max}$) | $I_{CCA}$ | — | 150 | — | 130 | — | 120 | — | 110 | mA | 2, 3, 4 |
| Active Quiescent Current ($\overline{E}$ = $V_{IL}$, $V_{CC}$ = max, f = 0 MHz) | $I_{CC2}$ | — | 80 | — | 80 | — | 80 | — | 80 | mA | |
| AC Standby Current ($\overline{E}$ = $V_{IH}$, $V_{CC}$ = max, f = $f_{max}$) | $I_{SB1}$ | — | 50 | — | 45 | — | 40 | — | 35 | mA | 2, 3, 4 |
| CMOS Standby Current ($V_{CC}$ = max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{CC} - 0.2$ V) | $I_{SB2}$ | — | 20 | — | 20 | — | 20 | — | 20 | mA | |

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing ($V_{IH}/V_{IL}$, $t_r/t_f$, pulse level 0 to 3.0 V, $V_{IH}$ = 3.0 V).
3. All address transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, $T_A$ = 25°C, Periodically Sampled Rather Than 100% Tested)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Address Input Capacitance | $C_{in}$ | — | 6 | pF |
| Control Pin Input Capacitance | $C_{in}$ | — | 6 | pF |
| Input/Output Capacitance | $C_{I/O}$ | — | 8 | pF |

## AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 3.3 V + 10%, – 5%, $T_A$ = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A

**READ CYCLE TIMING** (See Notes 1 and 2)

| Parameter | Symbol | 6926–8 | | 6926–10 | | 6926–12 | | 6926–15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | $t_{AVAV}$ | 8 | — | 10 | — | 12 | — | 15 | — | ns | 3 |
| Address Access Time | $t_{AVQV}$ | — | 8 | — | 10 | — | 12 | — | 15 | ns | |
| Enable Access Time | $t_{ELQV}$ | — | 8 | — | 10 | — | 12 | — | 15 | ns | |
| Output Enable Access Time | $t_{GLQV}$ | — | 4 | — | 5 | — | 6 | — | 7 | ns | |
| Output Hold from Address Change | $t_{AXQX}$ | 3 | — | 3 | — | 3 | — | 3 | — | ns | |
| Enable Low to Output Active | $t_{ELQX}$ | 3 | — | 3 | — | 3 | — | 3 | — | ns | 4,5,6 |
| Output Enable Low to Output Active | $t_{GLQX}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 4,5,6 |
| Enable High to Output High–Z | $t_{EHQZ}$ | — | 4 | 0 | 5 | 0 | 6 | 0 | 7 | ns | 4,5,6 |
| Output Enable High to Output High–Z | $t_{GHQZ}$ | — | 4 | 0 | 5 | 0 | 6 | 0 | 7 | ns | 4,5,6 |

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, $t_{EHQZ}$ max < $t_{ELQX}$ min, and $t_{GHQZ}$ max < $t_{GLQX}$ min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

### AC TEST LOADS

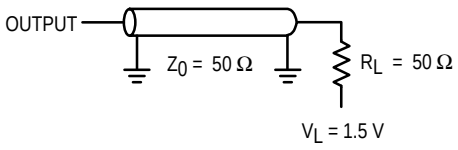



**Figure 1A**

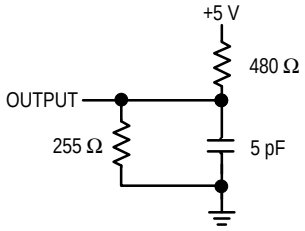
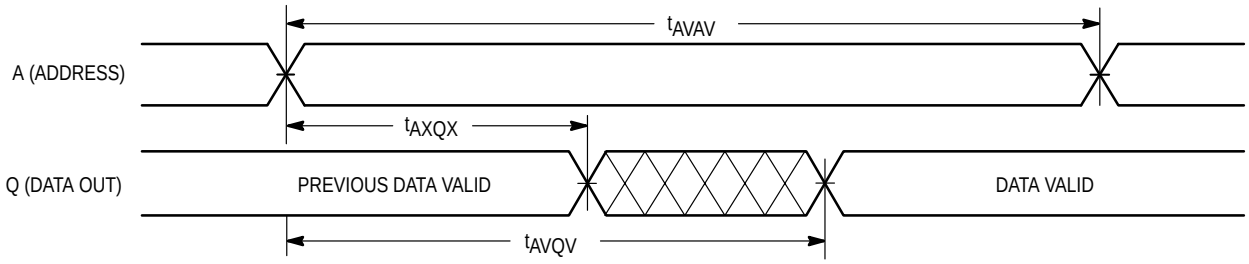



**Figure 1B**

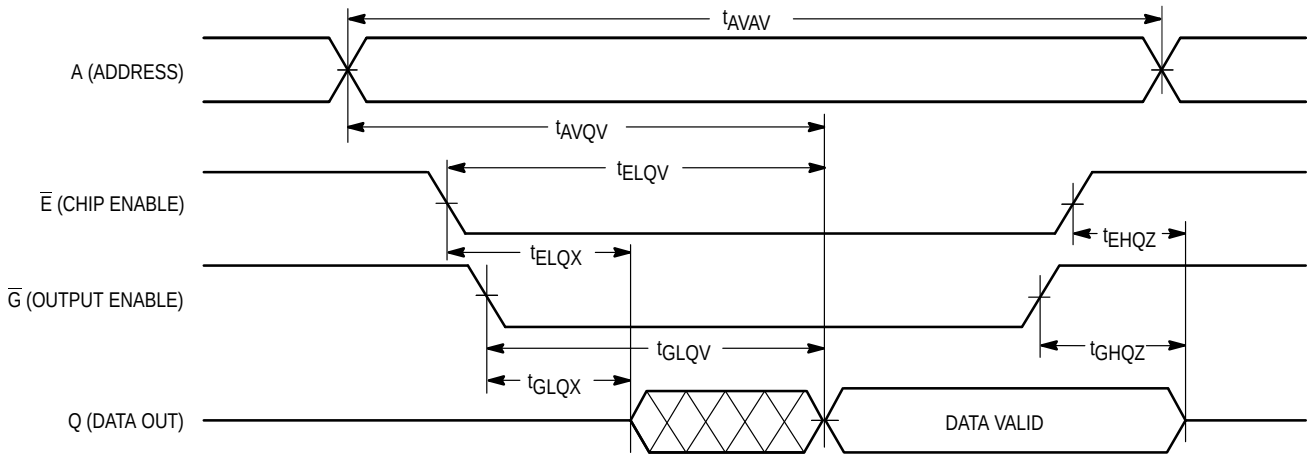
### TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1** (See Note 7)




**READ CYCLE 2** (See Note 8)

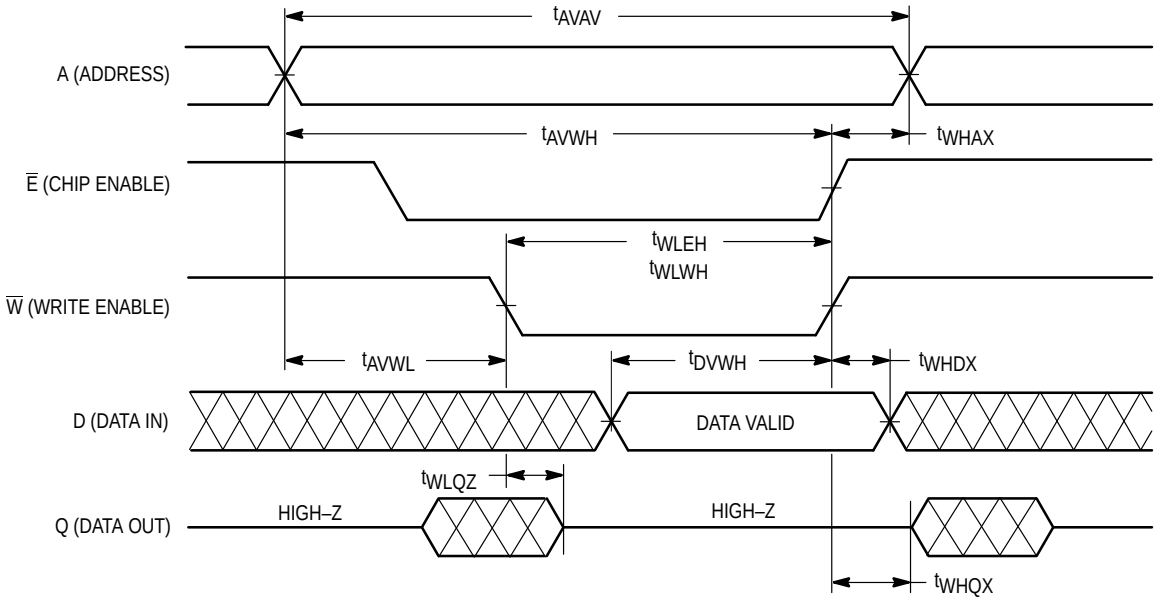


**WRITE CYCLE 1** ($\overline{W}$ Controlled, See Notes 1 and 2)

| Parameter | Symbol | 6926–8 | | 6926–10 | | 6926–12 | | 6926–15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | $t_{AVAV}$ | 8 | — | 10 | — | 12 | — | 15 | — | ns | 3 |
| Address Setup Time | $t_{AVWL}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Address Valid to End of Write | $t_{AVWH}$ | 8 | — | 9 | — | 10 | — | 12 | — | ns | |
| Address Valid to End of Write, $\overline{G}$ High | $t_{AVWH}$ | 7 | — | 8 | — | 9 | — | 10 | — | ns | |
| Write Pulse Width | $t_{WLWH}$, $t_{WLEH}$ | 8 | — | 9 | — | 10 | — | 12 | — | ns | |
| Write Pulse Width, $\overline{G}$ High | $t_{WLWH}$, $t_{WLEH}$ | 7 | — | 8 | — | 9 | — | 10 | — | ns | |
| Data Valid to End of Write | $t_{DVWH}$ | 4 | — | 5 | — | 6 | — | 7 | — | ns | |
| Data Hold Time | $t_{WHDX}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Write Low to Data High–Z | $t_{WLQZ}$ | 0 | 4 | 0 | 5 | 0 | 6 | 0 | 7 | ns | 4,5,6 |
| Write High to Output Active | $t_{WHQX}$ | 3 | — | 3 | — | 3 | — | 3 | — | ns | 4,5,6 |
| Write Recovery Time | $t_{WHAX}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, $t_{WLQZ}$ max < $t_{WHQX}$ min both for a given device and from device to device.

**WRITE CYCLE 1**

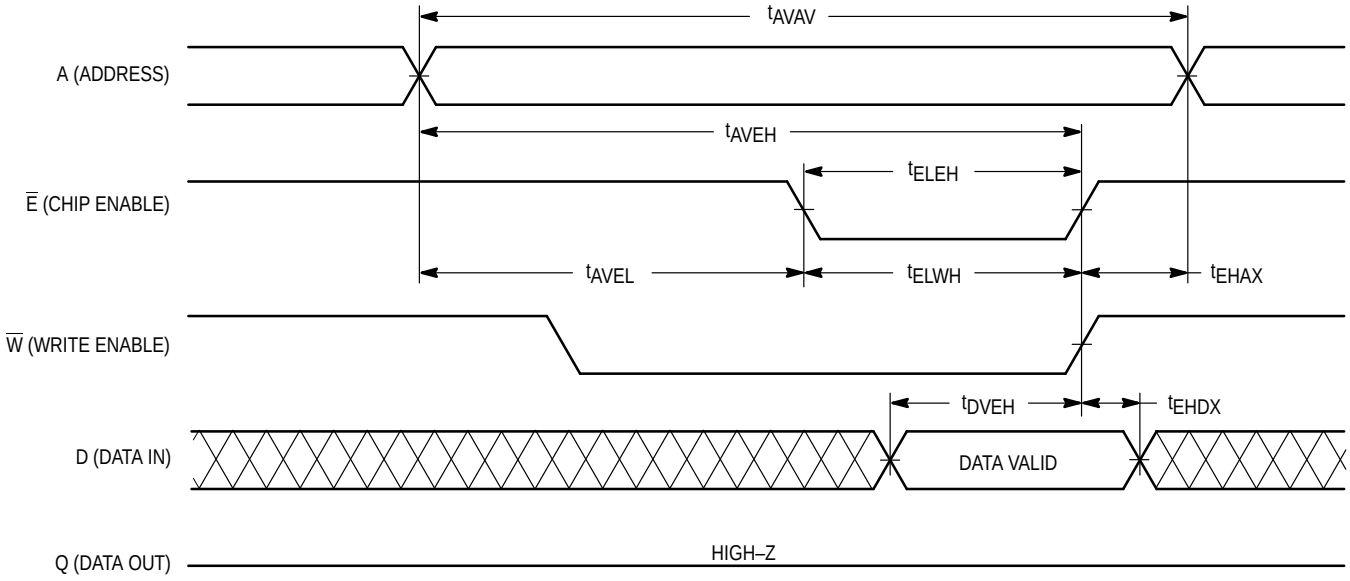


**WRITE CYCLE 2** ($\overline{E}$ Controlled, See Notes 1 and 2)

| Parameter | Symbol | 6926–8 | | 6926–10 | | 6926–12 | | 6926–15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | $t_{AVAV}$ | 8 | — | 10 | — | 12 | — | 15 | — | ns | 3 |
| Address Setup Time | $t_{AVEL}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Address Valid to End of Write | $t_{AVEH}$ | 7 | — | 8 | — | 9 | — | 10 | — | ns | |
| Enable to End of Write | $t_{ELEH}$, $t_{ELWH}$ | 7 | — | 8 | — | 9 | — | 10 | — | ns | 4,5 |
| Data Valid to End of Write | $t_{DVEH}$ | 4 | — | 5 | — | 6 | — | 7 | — | ns | |
| Data Hold Time | $t_{EHDX}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Write Recovery Time | $t_{EHAX}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |

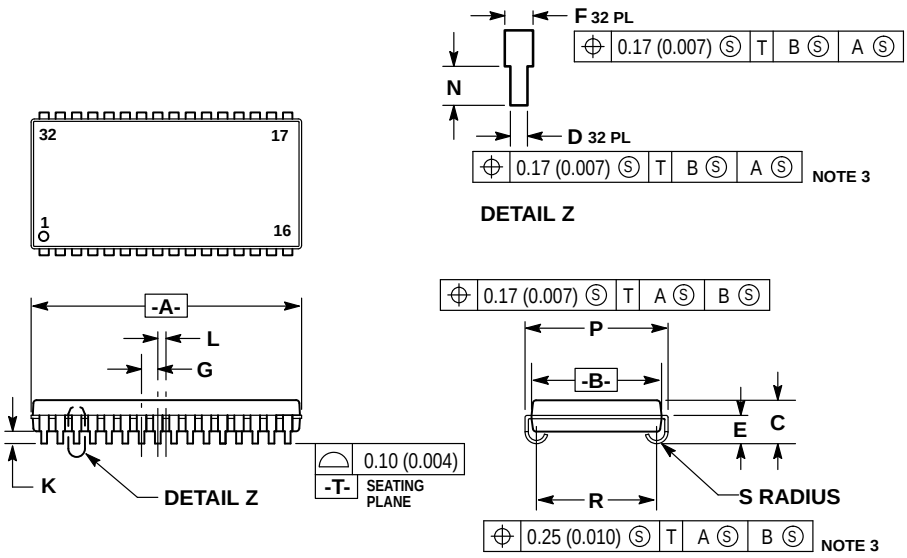
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

**WRITE CYCLE 2**



## PACKAGE DIMENSIONS

**32–LEAD**
**400 MIL SOJ**
**CASE 857A–02**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.820 | 0.830 | 20.83 | 21.08 |
| B | 0.395 | 0.405 | 10.03 | 10.29 |
| C | 0.128 | 0.148 | 3.26 | 3.75 |
| D | 0.016 | 0.020 | 0.41 | 0.50 |
| E | 0.088 | 0.098 | 2.24 | 2.48 |
| F | 0.026 | 0.032 | 0.67 | 0.81 |
| G | 0.050 BSC | | 1.27 BSC | |
| K | 0.035 | 0.045 | 0.89 | 1.14 |
| L | 0.025 BSC | | 0.64 BSC | |
| N | 0.030 | 0.045 | 0.76 | 1.14 |
| P | 0.435 | 0.445 | 11.05 | 11.30 |
| R | 0.365 | 0.375 | 9.27 | 9.52 |
| S | 0.030 | 0.040 | 0.77 | 1.01 |

## ORDERING INFORMATION
**(Order by Full Part Number)**

**MCM 6926 WJ XX X**

- MCM — Motorola Memory Prefix
- 6926 — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6926WJ8, MCM6926WJ8R, MCM6926WJ10, MCM6926WJ10R, MCM6926WJ12, MCM6926WJ12R, MCM6926WJ15, MCM6926WJ15R




**How to reach us:**
**USA / EUROPE**: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

**MFAX**: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
**INTERNET**: http://Design–NET.com

**JAPAN**: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

**HONG KONG**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298