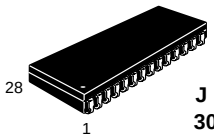
Synchronous Line Buffer: 8K x 8 Bit Fast Static Dual Ported Memory

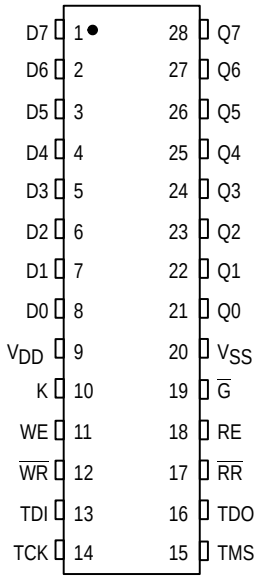
With IEEE Standard 1149.1 Test Access Port and Boundary–Scan (JTAG)

MCM62X308



J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



The MCM62X308 is a synchronous, dual ported memory organized as 8,192 words of 8 bits each, fabricated using Motorola's double–metal, double–poly, 0.65 μm CMOS process. It is intended for high speed video or other applications which process data on a line–by–line basis. Through the use of a single clock and port control inputs, separate read and write data ports provide simultaneous access to a common memory array. Simultaneous read/write access to the same address location is also allowed, with old data being read followed by a write of the new data. This allows multiple devices to be cascaded with the output of one directly driving the input of another. In this configuration the data stream can be tapped at strategic interconnect points to perform various digital filtering functions.

Since there are no external address inputs, separate internal read and write address counters are provided as a means of indexing the memory array. These counters are preloaded and then selectively incremented or decremented by asserting read enable (RE) and write enable (WE) inputs, allowing cycle to cycle control. The address counters can be reloaded back to their initial values through the use of the read reload ($\overline{RR}$) and write reload ($\overline{WR}$) control inputs. These inputs initiate the transfer of address reload register values into the address counters which index the memory array. When an address counter reaches 0000 (on down count) or FFFF (on up count), it will roll over on the next count. The TDI input is used to write the reload registers using special test access port instructions.

The read and write address counters are 16 bits long, and only 13 of the 16 bits are required to index the 8K deep memory array. The remaining three bits are used for depth expansion. These three bits are compared to the lower three bits in the control register, and as long as they are equal that port (i.e., read or write) will remain active. If the bits do not compare, the port will become inactive (i.e., for read outputs, high–z; for write inputs, disabled) however, the counter will continue to count on the rising edge of K as long as the port enable signal (RE or WE) is asserted. The TDI input is used to write the control register using special test access port instructions.

The output enable Input can be programmed to be either synchronous or asynchronous through the control register.

The MCM62X308 is available in a 28 pin SOJ package.

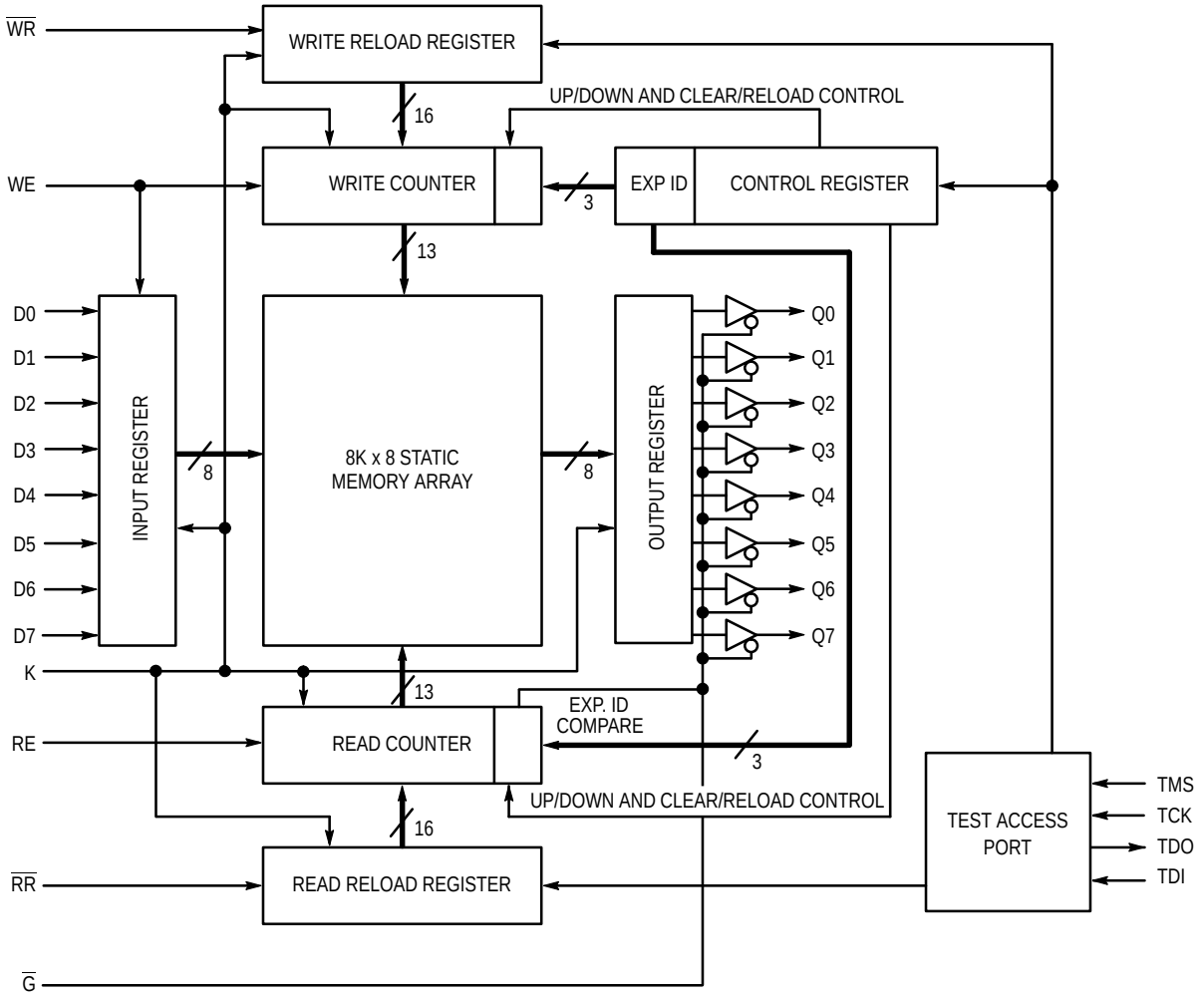
- 8K x 8 Fast Access Static Memory Array
- Single 5 V Power Supply — MCM62X308–15–5: ± 5%
  MCM62X308–17: ± 10%
- Synchronous, Simultaneous Read/Write Memory Access
- 50 MHz Maximum Clock Cycle Time, < 15 ns Read Access
- Single Clock Operation
- Separate Read/Write Address Counters with Reload Control
- Separate Up/Down Counter Control for Both Read and Write
- Programmable Output Enable Control (Synchronous or Asynchronous)
- Cascadable I/O Interface
- IEEE Standard 1149.1 Test Port (JTAG)
- Expand ID Register for Depth Expansion
- High Board Density SOJ Package
- Fully TTL Compatible

PIN NAMES

K	Clock Input
WE	Write Enable Input
$\overline{WR}$	Write Address Reload Input
RE	.Read Enable Input
$\overline{RR}$	Read Address Reload Input
$\overline{G}$	Output Enable Input
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
TCK	Test Clock Input
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
V_{DD}	+ 5 V Power Supply
V_{SS}	Ground

REV 1
5/95

BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

WE	$\overline{WR}$	RE	$\overline{RR}$	$\overline{G}$	Match EXP ID (Read/Write)	Mode (Read/Write)	Supply Current	Q0 – 7 Status
X	L	X	L	L	Match Read/Match Write	Reload, Read/Reload, Write Disable	I_{CC}	Data Out
H	H	H	H	L	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	Data Out
L	H	L	H	L	Match Read/Match Write	Read Count Disable/Write Disable	I_{CC}	Data Out
H	H	H	H	H	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	High–Z
H	H	H	H	X	No Match Read/No Match Write	Count, No Read/No Write, Count	I_{SB}	High–Z
H	H	H	H	X	No Match Read/Match Write	Count, No Read/Write, Count	I_{SB}	High–Z
H	H	H	H	L	Match Read/No Match Write	Count, Read/No Write, Count	I_{CC}	Data Out

PIN DESCRIPTIONS

SOJ Pin Locations	Symbol	Type	Description
10	K	Input	**CLOCK** – System clock input pin accepting a minimum 8 ns clock high or clock low pulse at a minimum 20 ns clock cycle. All other synchronous inputs excluding the test access port are captured on the rising edge of this signal.
11	WE	Input	**WRITE ENABLE** – Write enable is captured on K leading edge. When asserted this causes the input data D0 – D7 to be written into the RAM address controlled by the write address counter and increments the counter for the next write.
18	RE	Input	**READ ENABLE** – Read enable is captured on K leading edge. When asserted increments the counter for the next read operation. This causes a read access from the RAM address controlled by the read address counter to be inserted in the output register Q0 – Q7.
12	$\overline{WR}$	Input	**WRITE RELOAD** – Write reload is captured on K leading edge. When asserted this causes the write address counter to be initialized to the contents of the write reload register or “cleared” as specified by control register bit 3. See control register bit 3 for “cleared” description.
17	$\overline{RR}$	Input	**READ RELOAD** – Read reload is captured on K leading edge. When asserted this causes the read address counter to be initialized to the contents of the read reload register or “cleared” as specified by control register bit 5. See control register bit 5 for “cleared” description.
19	$\overline{G}$	Input	**OUTPUT ENABLE** – When asserted low causes the outputs Q0 – Q7 to become active and when deasserted high causes them to High–Z. This pin can be either synchronous with K leading edge or asynchronous as specified by control register bit 7.
8, 7, 6, 5, 4, 3, 2, 1	D0 – D7	Input	**DATA INPUT**– The levels on these pins are captured on the K leading edge. The value captured will be written into the RAM if WE is also asserted and the expand ID bits match the upper three bits of the write address counter.
21, 22, 23, 24, 25, 26, 27, 28	Q0 – Q7	Output	**DATA OUTPUT –** Data outputs are available from the read output register < 15 ns from the rising edge of K when RE or $\overline{RR}$ is asserted. outputs are disabled when the upper three bits of the read address counter do not match the three expand ID bits of the control register. $\overline{G}$ will also control the disabling of the outputs either synchronously or asynchronously. See $\overline{G}$ description.

TEST ACCESS PORT PIN DESCRIPTIONS (The Test Access Port Conforms with the IEEE Standard 1149.1. It is also Used to Load Device Specific Registers Used to Configure the MCM62X308.)

SOJ Pin Locations	Symbol	Type	Description
14	TCK	Input	**TEST CLOCK –** Samples and clocks all TAP events. All inputs are captured on TCK rising edge and all outputs propagate from TCK falling edge. It also can take the place of K in device operation in certain test conditions.
15	TMS	Input	**TEST MODE SELECT** – Sampled on the rising edge of TCK. Determines the movement through the TAP state machine (Figure 2). This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
13	TDI	Input	**TEST DATA IN** – Sampled on the rising edge of TCK. This is the input side of the serial register placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP state machine and what instruction is active in the TAP instruction register. This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
16	TDO	Output	**TEST DATA OU**T – Output that is active depending on the state of the TAP state machine. Output changes off the trailing edge of TCK. This is the output side of the serial register placed between TDI and TDO.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISITICS

(T_A = 0 to 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	MCM62X308–15–5	V_{DD}	4.75	5.0	5.25	V
	MCM62X308–17		4.50	5.0	5.50	
Input High Voltage		V_{IH}	2.2	—	V_{DD} + 0.3	V
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time = 20 ns)	I_{CCA}	—	150	mA
AC Standby Current (When Expand ID Bits Do Not Match the Read Address Counter, Cycle Time = 20 ns)	I_{SB}	—	100	mA
Output Low Voltage (I_{OL} = + 4.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance (Q0 – Q7, TDO)	C_{out}	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . Terminated 50 Ohm Transmission Line

READ/WRITE CYCLE TIMING

Parameter	Symbol	MCM62X308–15–5		MCM62X308–17		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	20	—	22	—	ns	
Clock High Time	t_{KHKL}	8	—	9	—	ns	
Clock Low Time	t_{KLKH}	8	—	9	—	ns	
Clock High to Output Valid	t_{KHQV}	5	15	5	17	ns	
Clock High to Output High–Z	t_{KHQZ}	5	15	5	15	ns	1
Output Enable Low to Output Valid	t_{GLQV}	3	10	3	10	ns	2, 4
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	5	ns	2, 3, 4
Setup Times: RE	t_{REVKH}	2	—	2	—	ns	5
WE	t_{WEVKH}						
$\overline{WR}$	t_{WRVKH}						
$\overline{G}$	t_{GVKH}						6
$\overline{RR}$	t_{RRVKH}	3	—	3	—		5
Data In	t_{DVKH}	1	—	1	—		5
Hold Times: RE	t_{KHREX}	2	—	2	—	ns	5
WE	t_{KHWEX}						
$\overline{RR}$	t_{KHRRX}						
$\overline{WR}$	t_{KHWRX}						
$\overline{G}$	t_{KHGX}						6
Data In	t_{KHDX}						

NOTES:
1. The outputs High–Z from a clock high edge when the upper three bits of the Read Address Counter do not match the 3 ID Expansion bits.
2. $\overline{G}$ is a don't care when the three ID expansion bits do not match the upper three bits of the Read Address Counter.
3. t_{GLQV} and t_{GHQZ} only apply when $\overline{G}$ is programmed as Asynchronous. (See TAP LDCONT instruction).
4. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQV} min for a given device and from device to device.
5. This is a synchronous device. All inputs must meet the specified setup and hold times for ***ALL*** rising edges of Clock except for $\overline{G}$ when it is programmed to be asynchronous.
6. t_{GVKH} and t_{KHGX} only apply when $\overline{G}$ is programmed as synchronous.

AC TEST LOADS

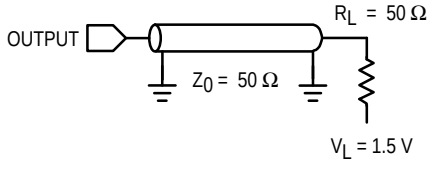


Figure 1A

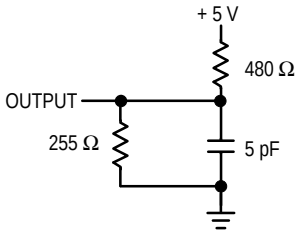
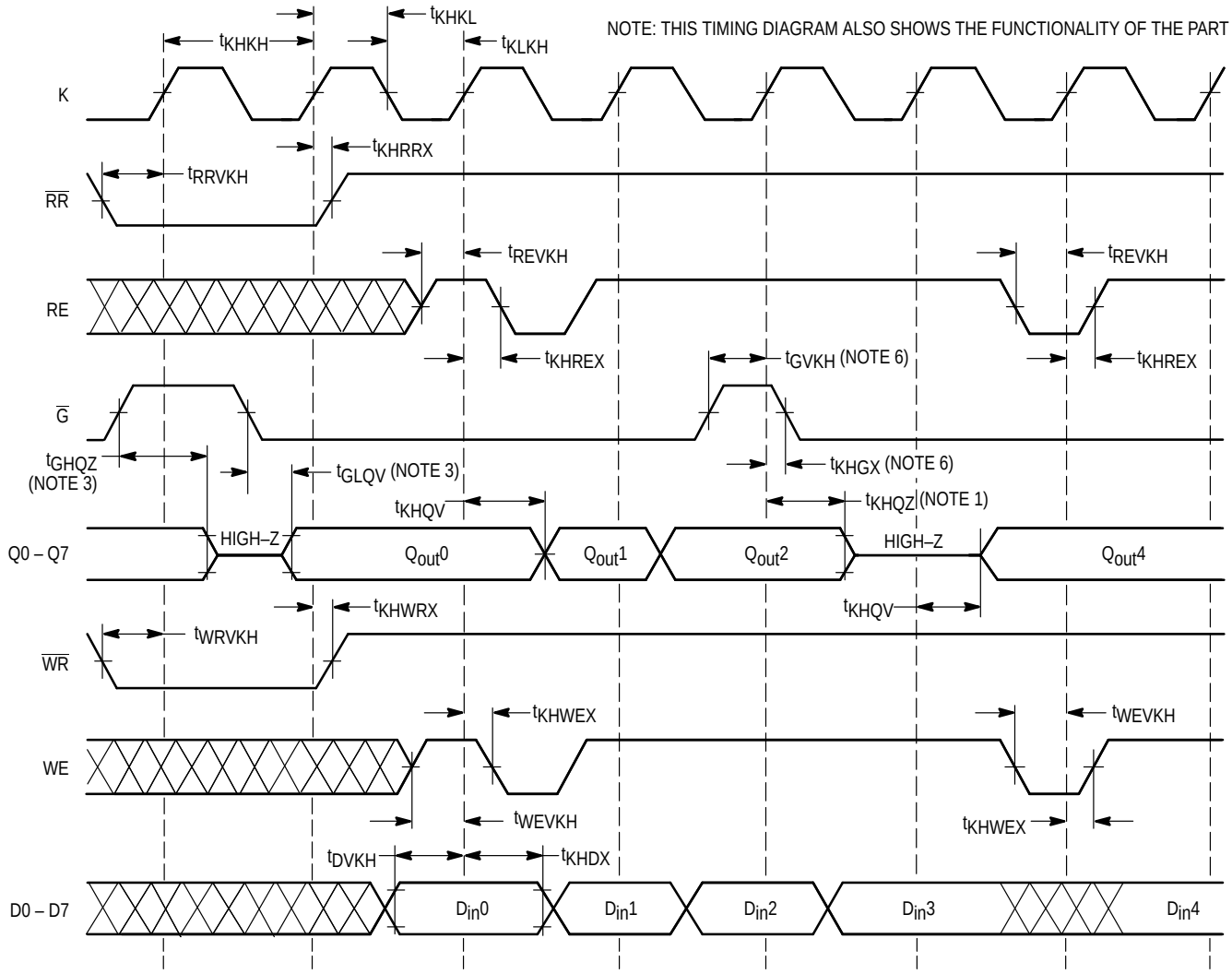


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ/WRITE CYCLE TIMING DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_A = 0 to + 70°C, Unless Otherwise Noted)

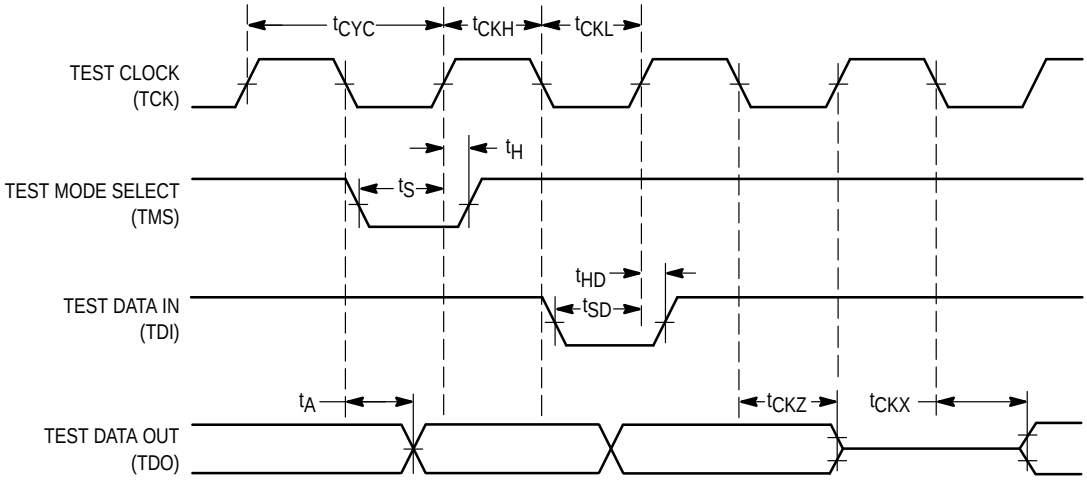
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . 50 Ohm Transmission Line

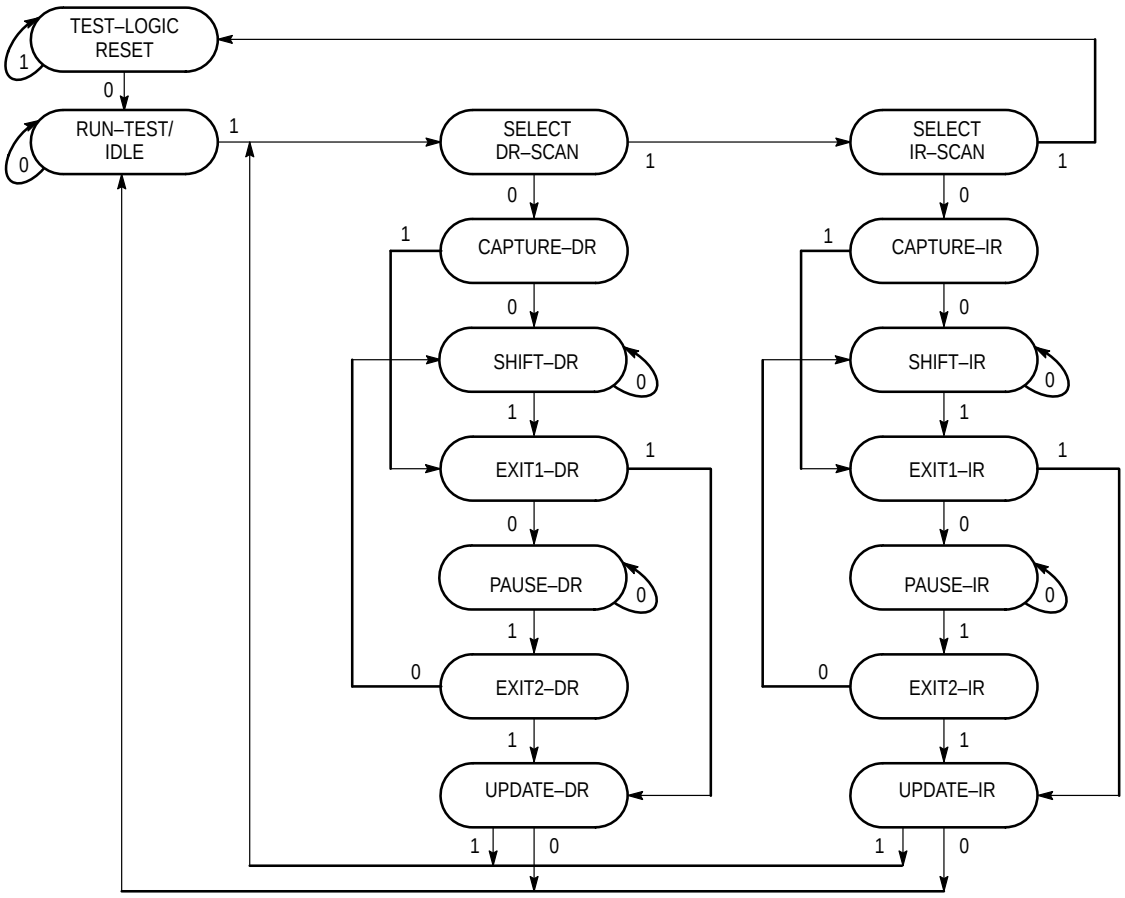
TAP CONTROLLER TIMING

Parameter	Symbol	MCM62X308–15–5		MCM62X308–17		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CYC}	30	—	30	—	ns	
Clock High Time	t_{CKH}	12	—	12	—	ns	
Clock Low Time	t_{CKL}	12	—	12	—	ns	
Clock Low to Output Valid	t_A	5	9	5	9	ns	
Clock Low to Output High–Z	t_{CKZ}	0	9	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	0	9	ns	2, 3
Setup Time, Test Mode Select	t_S	2	—	2	—	ns	
Setup Time, Test Data In	t_{SD}	2	—	2	—	ns	
Hold Time, Test Mode Select	t_H	2	—	2	—	ns	
Hold Time, Test Data In	t_{HD}	2	—	2	—	ns	

NOTES:
1. Test Data Out will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. Test Data Out is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

TAP CONTROLLER TIMING DIAGRAM





NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 2. TAP Controller State Diagram

TEST ACCESS PORT DESCRIPTIONS

INSTRUCTION SET

A four pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. There are two classes of instructions; standard instructions as defined in the IEEE 1149.1 standard and device specific, or public, instructions that are used to control the functionality of the device. When the TAP (Test Access Port) controller is in the Shift–IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction would be serially loaded through the TDI input (while 0101 will be shifted out of TDO). The TAP instruction set for this device is listed in Table 1.

TAP STANDARD INSTRUCTION SET

NOTE: The descriptions in this section are not intended to be used without the supporting IEEE 1149.1–1993 Standard.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instuction is used to allow scanning of the boudary–scan register without causing interference to the normal operation of the chip logic. The 22 bit boundary scan register contains bits for all device signal and clock pins and associated control signals (Table 2). This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the Shift–IR state. When the TAP controller is then moved to the Shift–DR state, the boundary scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. See the EXTEST instruction explanation below. It could also be used prior to the INTEST instruction to preload values into the input pins. As data is written into TDI, data also streams out of TDO which can be used to pre–sample the inputs and outputs. SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

Table 2 shows the boundary–scan bit definitions. The first column defines the bit's ordinal position in the boundary–scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted is 21. The second column is the pin name and the third column is the pin type.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins (i.e., Q0 – Q7). The EXTEST instruction would then be loaded.

During EXTEST the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). Once the EXTEST instruction is loaded, the TAP controller would then be moved to the Run–Test/Idle state. In this state one cycle of TCK would cause the preloaded data on the ouput pins to be driven while the values on the input pins would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero). Note that TCK, not the Clock pin, K, is used as the clock input while K is only sampled during EXTEST. The input pins are sampled in the Captor–DR state. After one clock cycle of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). While in the Shift–DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run–Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary–scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will be sampled regardless of $\overline{G}$). Only one action will be performed in the Run–Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

Since device functionality can only be verified through sampling the outputs of the device, the most likely use of INTEST would be to first load up the boundary–scan register for a Write Reload and execute the reload in the Run–Test/Idle state. Then a write of the first address would be performed again using the boundary scan register to load up the input registers and executing the write in the Run–Test/Idle state. Lastly, a Read Reload would be executed in the same manner so that the data that had just been written in the first address would be read from the memory array and written into the output registers which would then be shifted out of TDO in the Shift–DR state.

Table 1. TAP Instruction Set

Instruction	Code (Binary)	Description
Standard Instructions:		
BYPASS	1111*	Bypass Instruction
INTEST	0111	Intest Instruction
SAMPLE/PRELOAD	1100	Sample and/or Preload Instruction
EXTEST	0000	Extest Instruction
HIGHZ	1010	High–Z all Output pins while bypass reg. is between TDI and TDO
CLAMP	1001	Clamp Output pins while bypass reg. is between TDI and TDO
Device Specific (Public) Instructions:		
LDRREG	0001	Load Read Address Reload Register
LDWREG	0100	Load Write Address Reload Register
LDBREG	0101	Load both Address Reload Registers (Write then Read)
LDCONT	0010	Load Control Register
RDCOUNT	1000	Read the values of the Read and Write Address Counters
EZWRITE	0011	Serial Write (using Write Address Counter)
EZREAD	0110	Serial Read (using Read Address Counter)
EZREADZ	1110	Serial Read, outputs High–Z

*Default state at power–up.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary–scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values to be driven on the output pins when the CLAMP instruction is active. Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero.

HIGH–Z TAP INSTRUCTION

The High–Z instruction is provided to allow all the outputs to be placed in an inactive drive state (High–Z). During the High–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The Bypass instruction is the default instruction loaded in at power up. This instruction will place a single shift register between TDI and TDO during the Shift–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

Table 2. Sample/Preload Boundary Scan Register Bit Definitions

Bit Number	Pin Name	Pin Type
0	$\overline{RR}$	Input
1	RE	Input
2	$\overline{G}$	Input
3	Q0	Output
4	Q1	Output
5	Q2	Output
6	Q3	Output
7	Q4	Output
8	Q5	Output
9	Q6	Output
10	Q7	Output
11	D7	Input
12	D6	Input
13	D5	Input
14	D4	Input
15	D3	Input
16	D2	Input
17	D1	Input
18	D0	Input
19	K	Input
20	WE	Input
21	$\overline{WR}$	Input

NOTE: K is a sample–only scan bit. It cannot be pre–loaded for control purposes.

DEVICE SPECIFIC (PUBLIC) INSTRUCTIONS

LDCONT INSTRUCTION

The Control Register is an eight bit register that contains the control bits for the Address Registers and Counters and the Output Enable pin. When the LDCONT TAP instruction is loaded into the Instruction Register, the Control Register is placed between TDI and TDO when the TAP controller is in the Shift–DR state (Table 10). The power–up/preload state and function of the Control bits are found in Table 3.

The Expand ID bits provide system depth expansion. These three bits are compared to the upper three bits in the address counters. As long as the three Expand–ID bits match the three upper bits in the address counters the port will stay active. If they do not match, the port will deactivate (i.e., outputs will High–Z or write will be disabled); however, the counters will continue counting as long as RE and WE remain asserted (i.e., high) at the rising edge of Clock.

The Reload Control bits (3 and 5) are used to control either reloading the Read and Write Address Counters from the Reload Registers or clearing the counter when $\overline{RR}$ or $\overline{WR}$ is asserted. If these bits are set low the counters they control will be cleared to all zeroes if the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted and any value in the Reload Register is ignored. This means that if the initial address value desired is address 0000 (or FFFF when counting down) then there is no need to load the Address Reload Registers using the LDRREG, LDWREG, or the LDBREG instructions in the following description. If these bits are set high the counters are loaded up with the values in the Reload Registers when the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted.

The Up/Down count bits (4 and 6) determine the direction in which the respective Address Counter will count; if the bit is set low the counter will count up and if set high the counter will count down. If the counters are set to count down and the Reload control is set to the clear counter mode, then the initial value in the counters will be FFFF. To ensure that the counter will function properly, a reload (using $\overline{RR}$ or $\overline{WR}$) is required after the count direction is switched.

The Output Enable control bit (7) determines the functionality of the Output Enable pin, $\overline{G}$. When the bit is low, $\overline{G}$ functions asynchronously. When set high, $\overline{G}$ functions synchronously and must meet the specified setup and hold times to the Clock K.

The Control Register will also be preloaded. When the instruction 0010 (LDCONT) is in the Instruction Register and the controller is in the Capture–DR state the above preload values (all zeroes) will be loaded into the Control Register. All zeroes will also be loaded in the Control Register at power–up.

While new values are shifted in from TDI in the Shift–DR state, all zeroes will be output on TDO for the first eight bits.

LDRREG, LDWREG, AND LDBREG TAP INSTRUCTIONS

There are three instructions that may be used to load the 16 bit address reload registers: LDRREG (Load Read Address Reload Register), LDWREG (Load Write Address Reload Register), and LDBREG (Load both Address Reload Registers, Write followed by Read). Figure 3 illustrates how the Reload registers are placed between TDI and TDO. Tables 7, 8, and 9 describe each register. These instructions would be used only if the user needed to load the Reload Registers with a non–zero value. If the Address Counters are to always be reset to zeroes (or all 1s if counting down) then only the Control Register need be loaded to affect a reset of the counters.

The TAP controller has been set up to make it easier for the user to serially load the Reload Registers. When the TAP controller is clocked into the Capture–IR state (see state diagram) the instruction for loading both registers (0101) will be preloaded into the shift register. This allows the user to go directly to the Update–IR state instead of having to serially shift this instruction in through the TDI port. Once the load instruction has been entered the user can then clock over to the Capture–DR state where the value for the reload register(s) is serially loaded (see Figure 3).

RDCOUNT TAP INSTRUCTION

The RDCOUNT scan register is accessible after the RDCOUNT instruction is loaded into the TAP instruction register in the Shift–IR state and the TAP controller is then moved to the Shift–DR state. This scan register can then be used to shift out the values of the Read and Write Address Counters The RDCOUNT scan–register is a sample only register and can not be used to load values into the counters. See Table 4.

EZWRITE TAP INSTRUCTION AND SCAN PATH

The EZWRITE TAP instruction is provided to allow the user to more easily and quickly write a large number of bytes to the

device serially through the TDI port. EZWRITE shortens the scan path for a serial write to just the 8 bit Data in register (see Table 5).

The most likely use of this instruction is as follows: the user would first load the Control Register using the LDCONT instruction. This would initialize the Expand ID bits and the Write Counter. The Write Reload Register will need to be loaded using the LDWREG instruction if a non–zero starting address is desired. If 0000 was the first desired count, setting up the Control Register to "clear" the Write counter is all that is required (Bit 3 set to zero). A reload cycle using SAMPLE/PRELOAD ($\overline{WR}$ preloaded low) and INTEST would also have to be run in order to initialize the counter. While still in the INTEST instruction at the Shift–DR state, the proper values of WE and $\overline{WR}$ would then need to be preloaded for proper operation of EZWRITE (WE high and $\overline{WR}$ high). After all this initializing is done, the EZWRITE instruction would be loaded into the TAP instruction register in the Shift–IR state. When the TAP controller is then moved to the Shift–DR state the EZWRITE scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data In register (see Table 5). The 8 bits to be written into the first address would be scanned in (sampled values from the Data In pins would be streaming out of TDO at the same time), then the TAP controller would be moved to the Run–Test/Idle state where one cycle of TCK would write the 8 bits into the address and increment the counter. The TAP controller would then move back to the Shift–DR state so that the next byte to be written can be serially loaded and the process would be repeated until all desired bytes were written. During EZWRITE the Q0 – Q7 pins will be in a High–Z state.

Table 3. Control Register Bit Description

Bit No.	Power Up and Preload State	Function
0 – 2	000	Expand ID bits for comparison with the upper 3 bits of the Read and Write Address counters
3	0	Reload Control of Write Address Counter (0 = clear counter, 1 = reload)
4	0	Up/Down count bit for Write Address Counter (0 = count up, 1 = count down)
5	0	Reload Control of Read Address Counter (0 = clear counter, 1 = reload)
6	0	Up/Down count bit for Read Address Counter (0 = count up, 1 = count down)
7	0	$\overline{G}$ Control (0 = asynchronous, 1 = synchronous)

EZREAD TAP INSTRUCTION AND SCAN PATH

The EZREAD TAP instruction is provided to allow the user to more easily and quickly read a large number of bytes from the device serially through the TDO port. EZREAD shortens the scan path for a serial read to just the 8 bit Data Out register (see Table 6).

To serially read the device the following would occur: initialization would be much like EZWRITE except that the Read Address Counter should be reladed with the count BEFORE the first one desired. So, if the first read needed to be address 0000 (and the counter is counting up), the Read Reload Register would have to be preloaded with FFFF using the LDRREG instruction. Again, SAMPLE/PRELOAD and INTEST instructions would need to be run to perform a reload cycle followed by another Boundary–scan that set RE and $\overline{RR}$ high in anticipation of the EZREAD instruction. Also, WE should be set low to prevent any unintended writes while reading. After this initializing, the EZREAD instruction would be loaded into the TAP instruction register in the Shift–IR state. The TAP controller would move to the Run–Test/Idle state where one cycle of TCK would increment the counter, read the 8 bits from that address, and load them into the Data Output register. The TAP controller would then move to the Shift–DR state and the EZREAD scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data Out register (see Table 6). In the Shift–DR state the Data Out register would be serially scanned out of the TDO port. This sequence through the TAP state machine would then be repeated until all desired bytes were read. EZREAD keeps the Q0 – Q7 pins active (if $\overline{G}$ is preloaded low) to allow parallel reading of the data out if desired.

EZREADZ TAP INSTRUCTION AND SCAN PATH

The EZREADZ TAP instruction behaves exactly like the EZREAD instruction except that the all outputs are held in a High–Z mode once the instruction is loaded.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the IEEE 1149.1 Test Access Port. To circuit disable the TAP controller without interfering with normal operation of the device TCK must be tied to V_{SS} to preclude midlevel inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response identical to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1 k resistor. TDO should remain unconnected.

With the four Test Access Port pins disabled, the device can only be used in its default power–up state. At power up, the device is configured to count up starting at address 0, the reload pins ($\overline{RR}$ and $\overline{WR}$) will clear the counters, the Expand ID bits are set to 000, and the Output Enable pin ($\overline{G}$) is configured as an asynchronous input.

Table 4. RDCOUNT Scan Register Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RAC0	Input
1	RAC1	Input
2	RAC2	Input
3	RAC3	Input
4	RAC4	Input
5	RAC5	Input
6	RAC6	Input
7	RAC7	Input
8	RAC8	Input
9	RAC9	Input
10	RAC10	Input
11	RAC11	Input
12	RAC12	Input
13	RAC13#	Input
14	RAC14#	Input
15	RAC15#	Input
16	WAC0	Input
17	WAC1	Input
18	WAC2	Input
19	WAC3	Input
20	WAC4	Input
21	WAC5	Input
22	WAC6	Input
23	WAC7	Input
24	WAC8	Input
25	WAC9	Input
26	WAC10	Input
27	WAC11	Input
28	WAC12	Input
29	WAC13#	Input
30	WAC14#	Input
31	WAC15#	Input

* RAC = Read Address Counter
WAC = Write Address Counter

\# These register bits are compared to the three Expand ID bits in the Control Register. (EX0 – 2). Only when there is a match is the read or write allowed to occur.

NOTE: Bit 0 closest to TDO.

Table 5. EZWRITE Scan Path Bit Definitions

Bit Number	Pin Name	Pin Type
0	D7	Input
1	D6	Input
2	D5	Input
3	D4	Input
4	D3	Input
5	D2	Input
6	D1	Input
7	D0	Input

Table 6. EZREAD and EZREADZ Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	Q0	Output
1	Q1	Output
2	Q2	Output
3	Q3	Output
4	Q4	Output
5	Q5	Output
6	Q6	Output
7	Q7	Output

Table 7. LDRREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit

* RRR = Read Reload Register

Table 8. LDBREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit
16	WRR0	Register bit
17	WRR1	Register bit
18	WRR2	Register bit
19	WRR3	Register bit
20	WRR4	Register bit
21	WRR5	Register bit
22	WRR6	Register bit
23	WRR7	Register bit
24	WRR8	Register bit
25	WRR9	Register bit
26	WRR10	Register bit
27	WRR11	Register bit
28	WRR12	Register bit
29	WRR13	Register bit
30	WRR14	Register bit
31	WRR15	Register bit

* RRR = Read Reload Register
WRR = Write Reload Register
NOTE: Bit 0 closest to TDO.

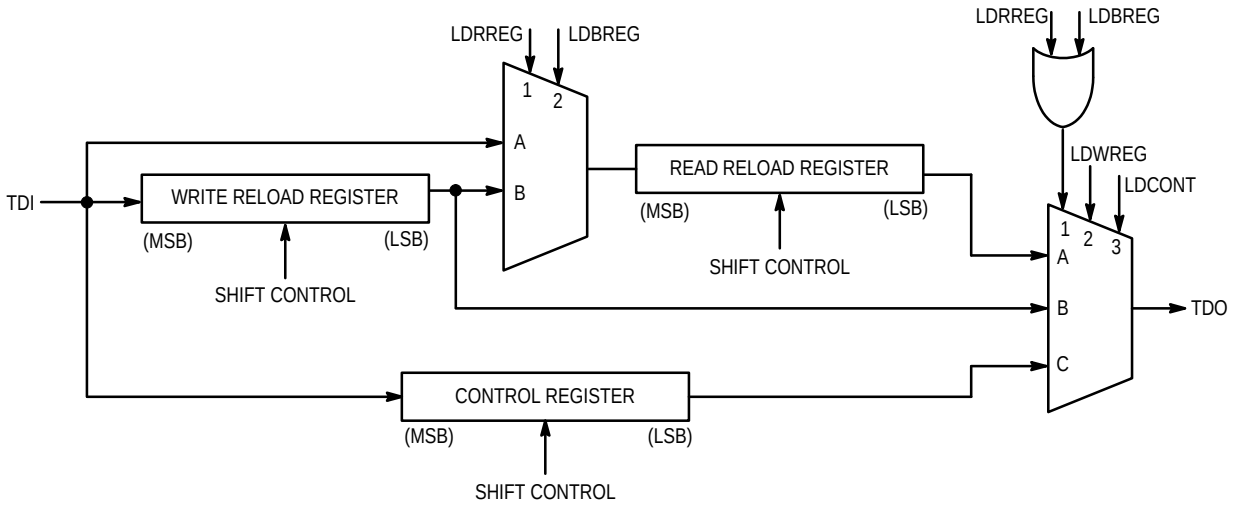
Table 9. LDWREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	WRR0	Register bit
1	WRR1	Register bit
2	WRR2	Register bit
3	WRR3	Register bit
4	WRR4	Register bit
5	WRR5	Register bit
6	WRR6	Register bit
7	WRR7	Register bit
8	WRR8	Register bit
9	WRR9	Register bit
10	WRR10	Register bit
11	WRR11	Register bit
12	WRR12	Register bit
13	WRR13	Register bit
14	WRR14	Register bit
15	WRR15	Register bit

* WRR = Write Reload Register

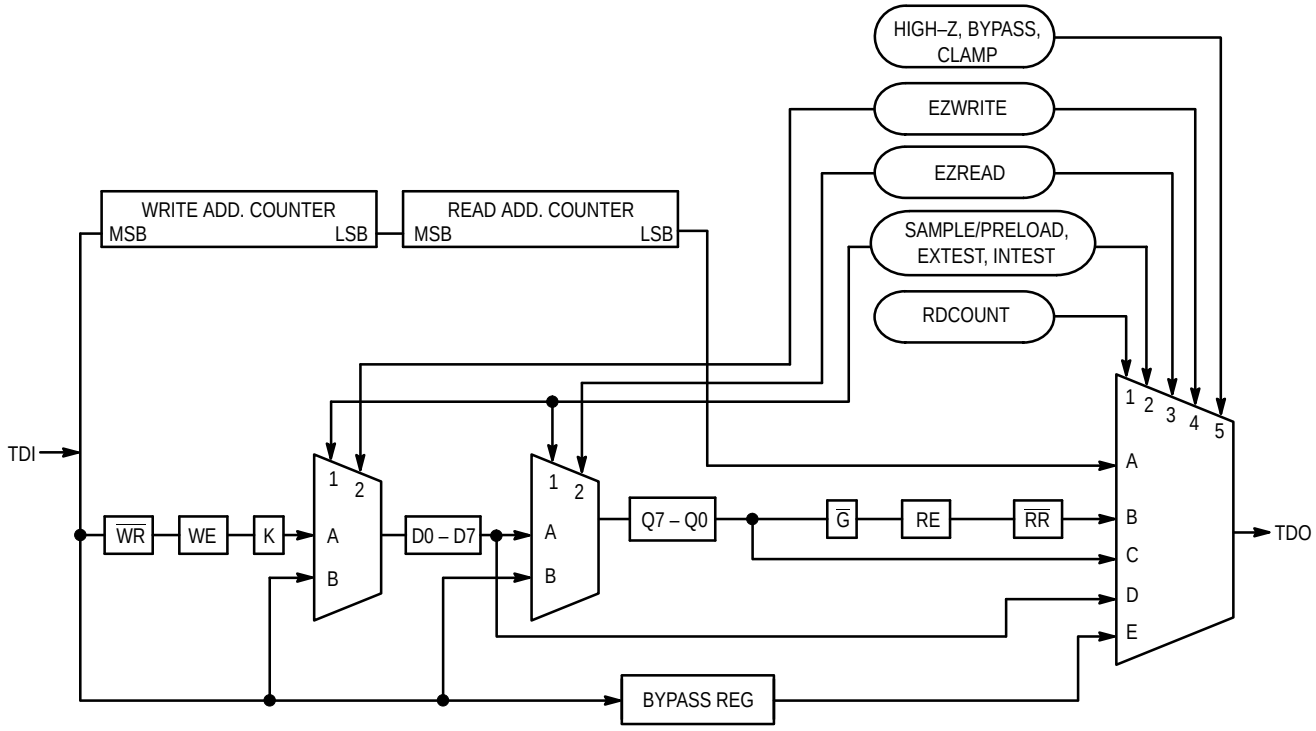
Table 10. LDCONT Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	EX0	Register bit
1	EX1	Register bit
2	EX2	Register bit
3	WCC	Register bit
4	UDW	Register bit
5	RCC	Register bit
6	UDR	Register bit
7	G CONT	Register bit



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 3. Register Load Paths



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFTSIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 4. Boundary Scan Paths

APPLICATIONS

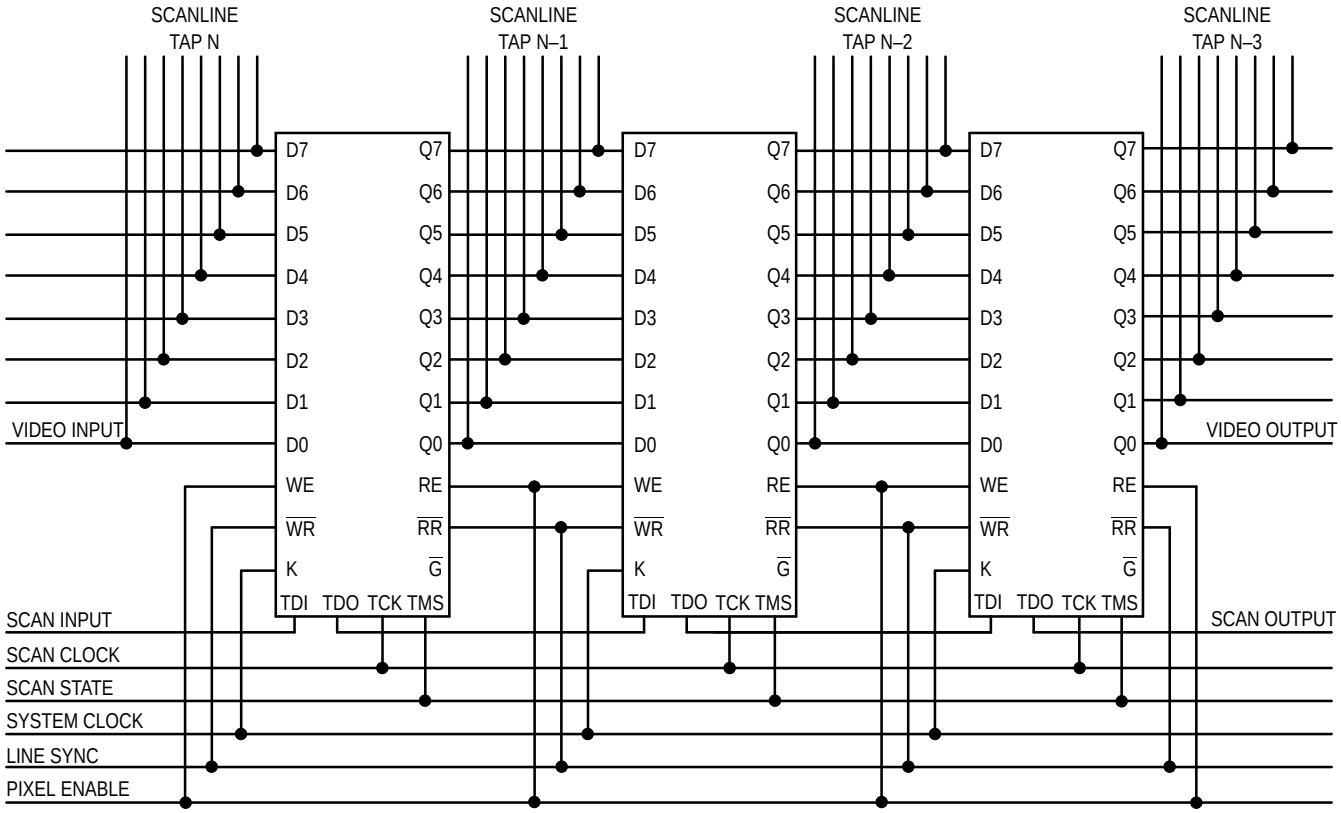


Figure 5. Multi–Stage 8–Bit Video Scanline Delay (8192 Pixels Maximum)

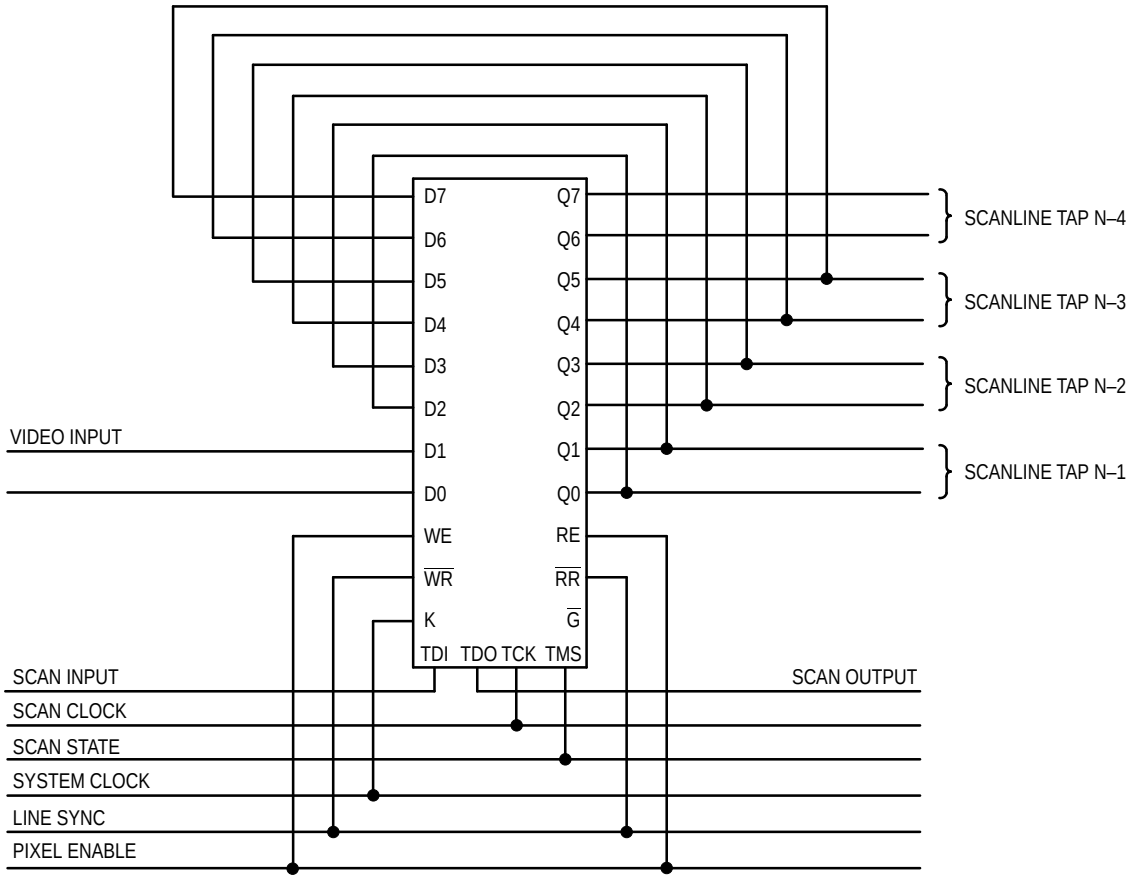


Figure 6. Multi–Stage 2–Bit Video Scanline Delay (8192 Pixels Maximum)

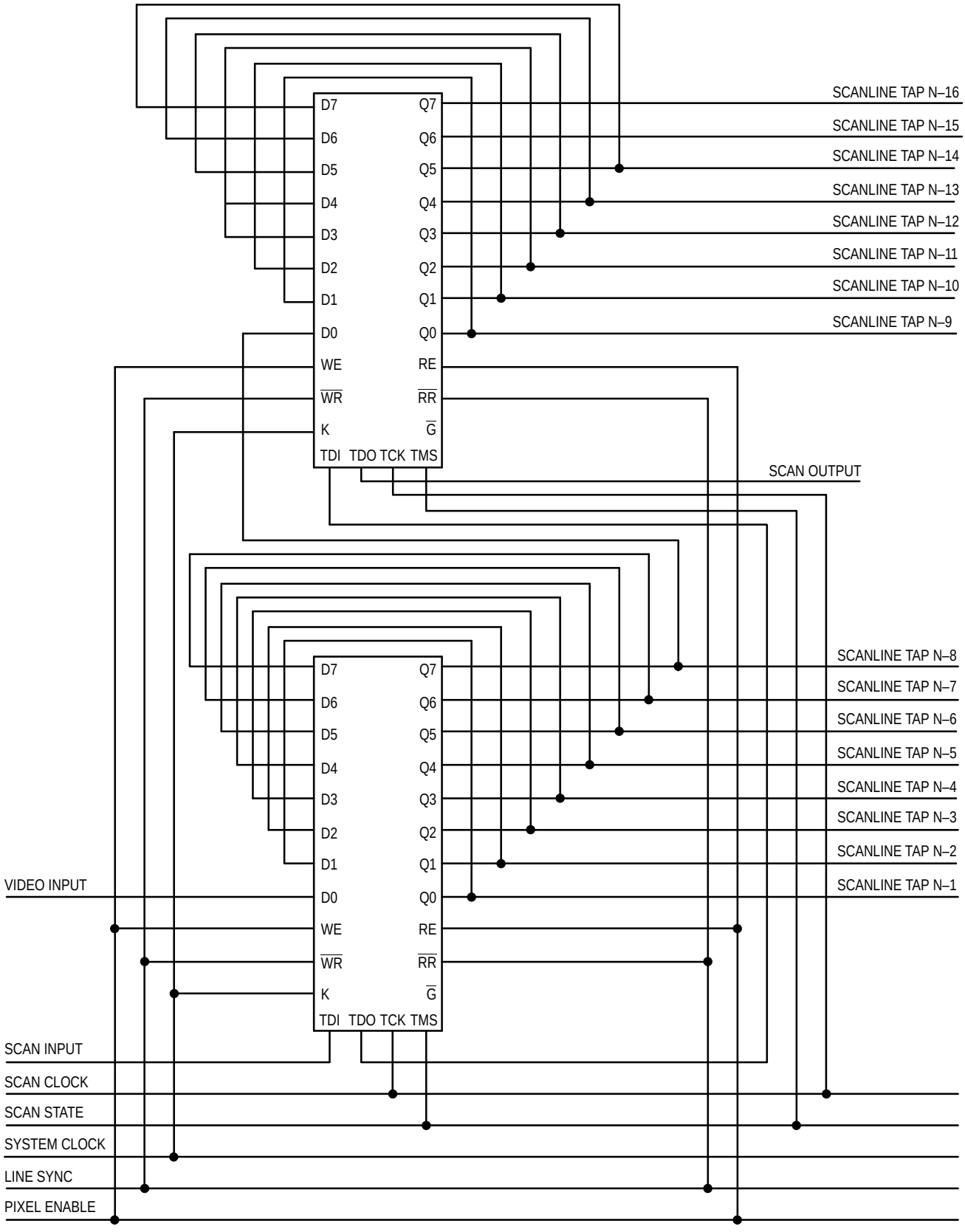


Figure 7. Multi–Stage 1–Bit Video Scanline Delay (8192 Pixels Maximum)

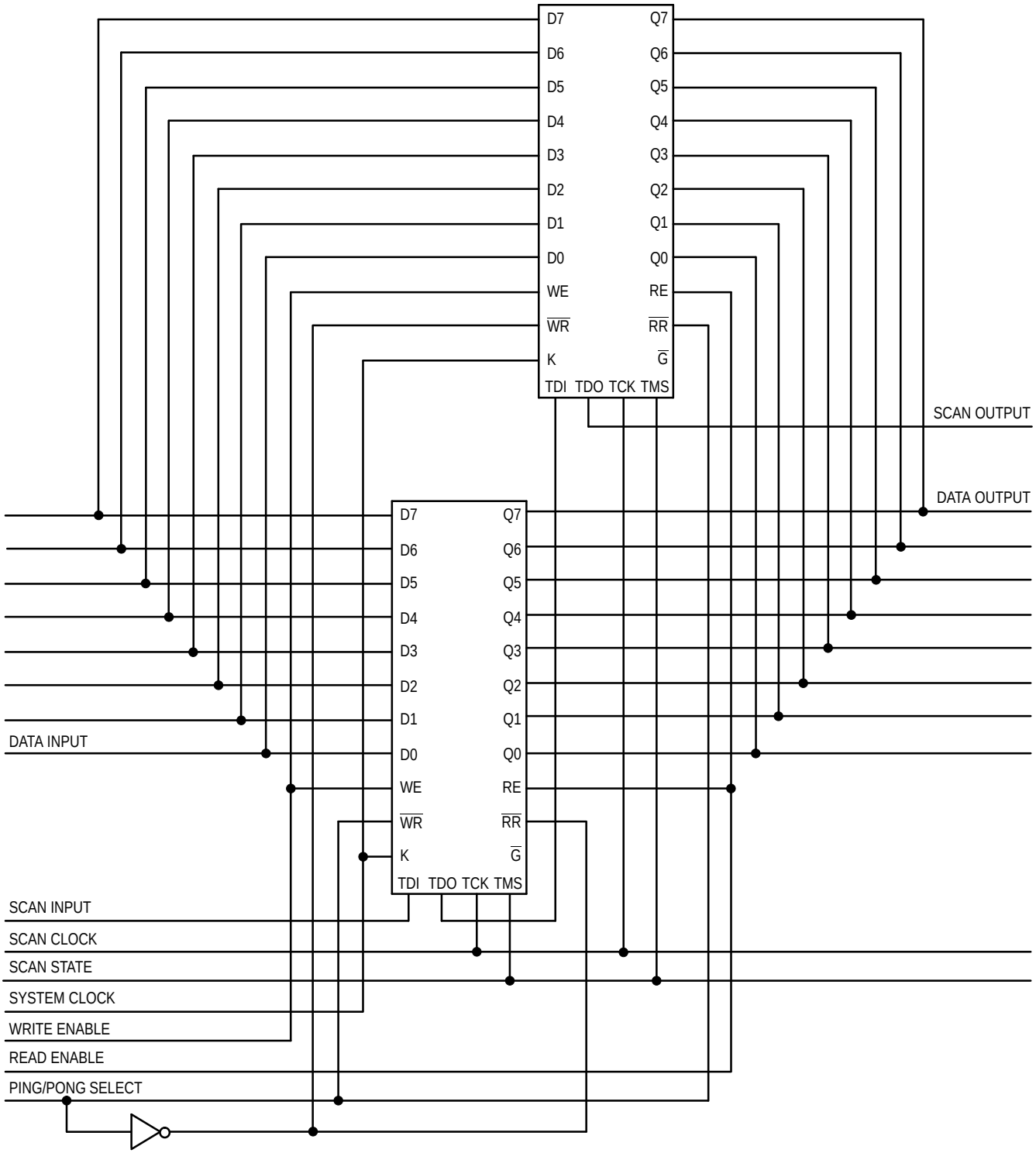


Figure 8. “Ping–Pong” Synchronizing Buffer (8192 Pixels Maximum)

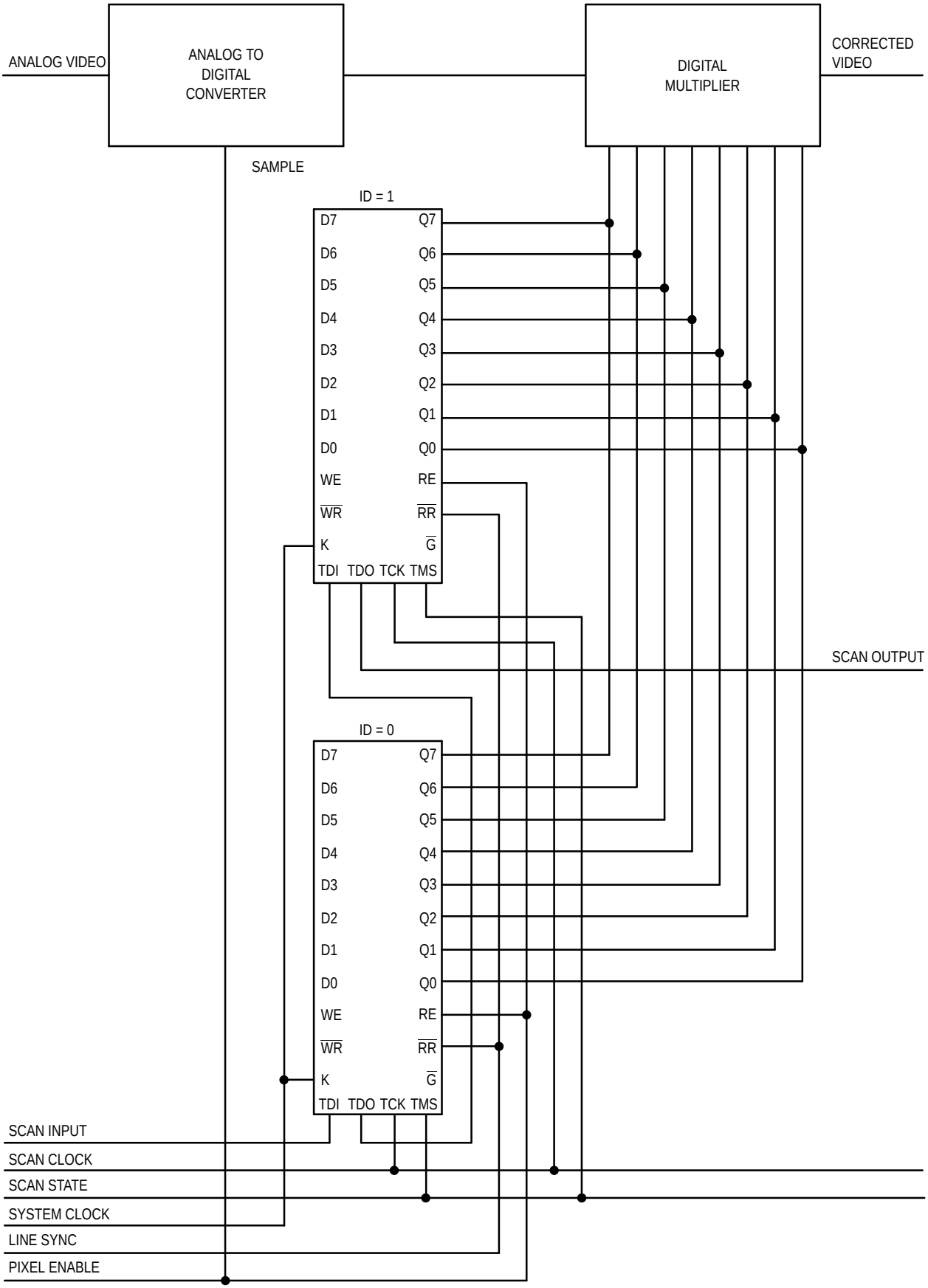


Figure 9. CCD Gain Correction, Buffer Written From Scan Input (16384 Pixels Maximum)

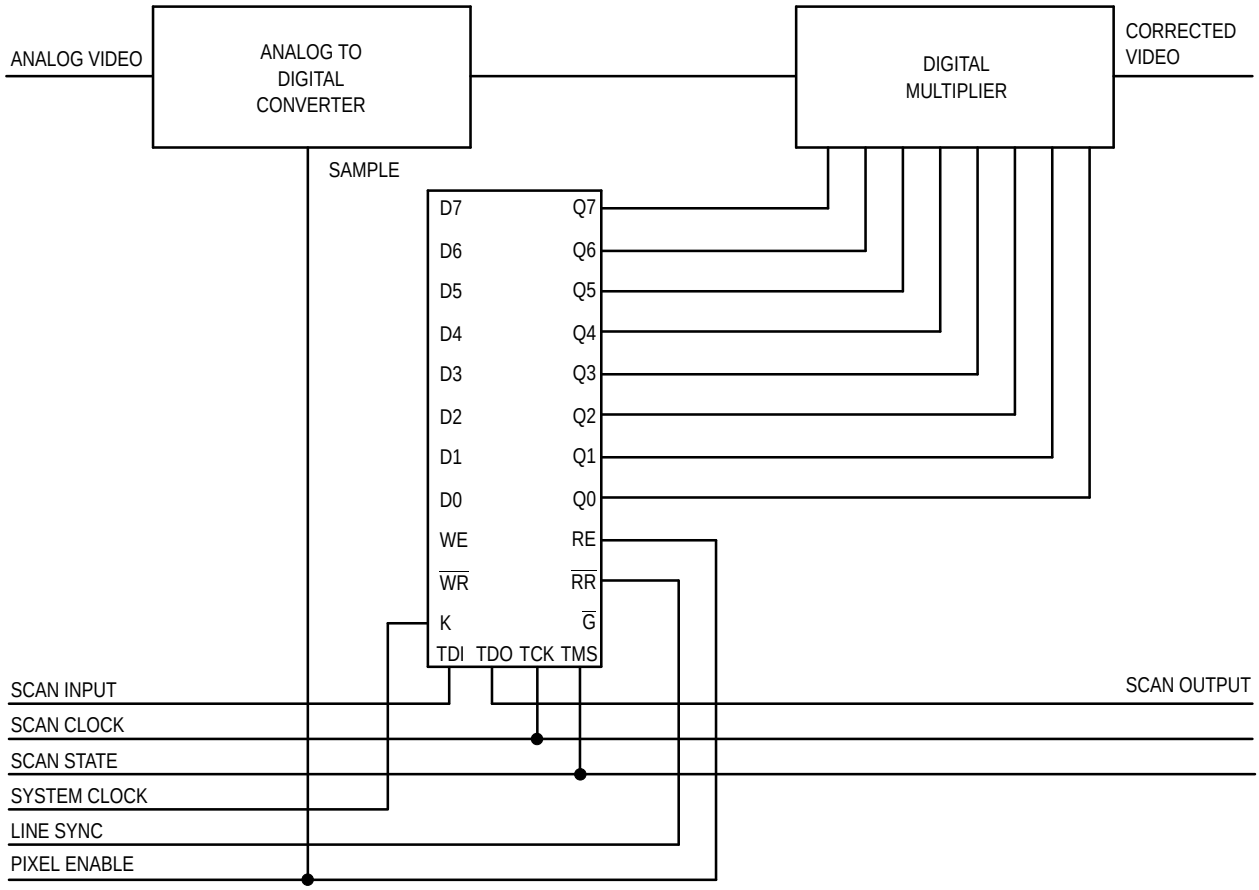


Figure 10. CCD Gain Correction, Buffer Written From Scan Input (8192 Pixels Maximum)

ORDERING INFORMATION

(Order by Full Part Number)

MCM 62X308 J XX

Motorola Memory Prefix

Part Number

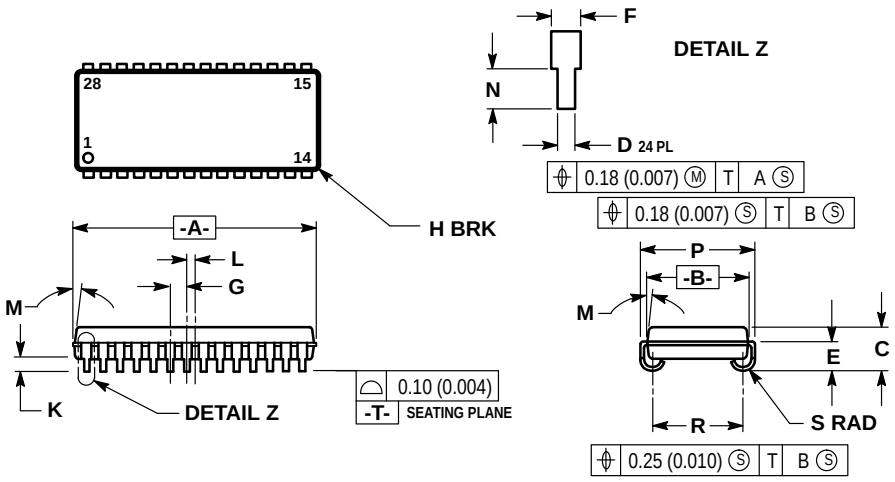
Speed (15–5 = 15 ns, 17 = 17 ns)

Package (J = SOJ)

Full Part Numbers — MCM62X308J15–5 MCM62X308J17

PACKAGE DIMENSIONS

J PACKAGE
300 MIL SOJ
CASE 810B–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM –T–.
5. 810B–01 AND –02 OBSOLETE, NEW STANDARD 810B–03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

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