MCM62995A

16K x 16 Bit Asynchronous/ Latched Address Fast Static RAM

The MCM62995A is a 262,144 bit latched address static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Address, data in, and chip enable latches are provided. When latch enable (LE for address and chip enables and DL for data in) is high, the address, data in, and chip enable latches are in the transparent state. If latch enable (LE, DL) is tied high, the device can be used as an asynchronous SRAM. When latch enable (LE, DL) is low, the address, data in and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

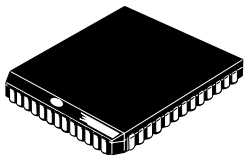
Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0 – DQ7 (the lower bits), while $\overline{BWH}$ controls DQ8 – DQ15 (the upper bits).

Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62995A is available in a 52 pin plastic leaded chip carrier (PLCC).

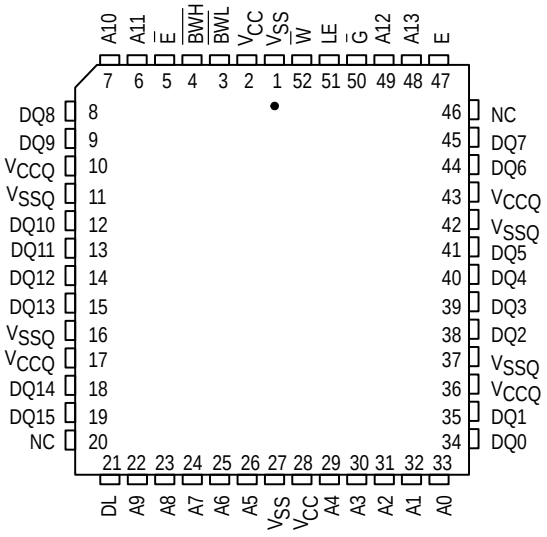
This device is ideally suited for systems which require wide data bus widths, cache memory and tag RAMs. See Figure 2 for applications information.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENT

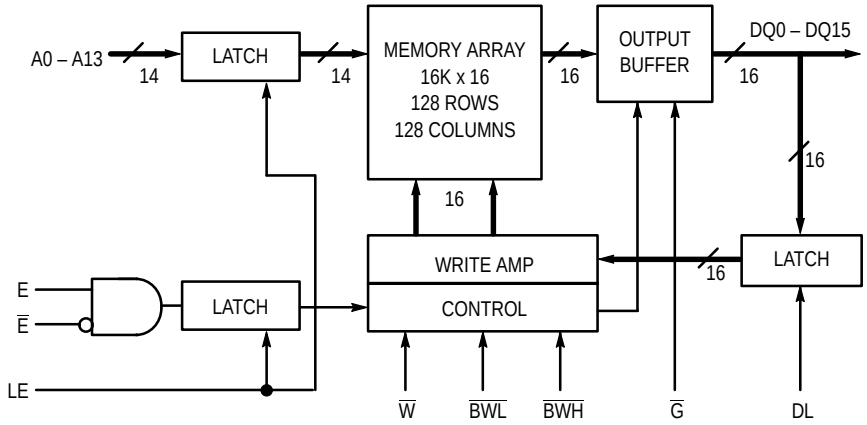


PIN NAMES	
A0 – A13	Address Inputs
LE	Latch Enable
DL	Data Latch Enable
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

REV 2
5/95

BLOCK DIAGRAM



TRUTH TABLE

Es	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	LE	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	H	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	H	X	L	Read Cycle	I_{CC}	Data Out
T	H	X	X	L	X	L	Latched Read Cycle	I_{CC}	Data Out
T	L	L	L	H	H	X	Write Cycle All Bits	I_{CC}	High–Z
T	L	H	H	X	X	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	H	H	X	Write Cycle Lower 8 Bits	I_{CC}	High–Z
T	L	H	L	H	L	X	Write Cycle Upper 8 Bits Latched Data–In	I_{CC}	High–Z
T	L	L	L	L	L	X	Latched Write Cycle Latched Data–In	I_{CC}	High–Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and Addresses satisfy the specified setup and hold times for the falling edge of LE. Data–in satisfies the specified setup and hold times for falling edge of DL.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = V_{SSQ} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current (E = V_{IL}, $\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC TEST LOADS

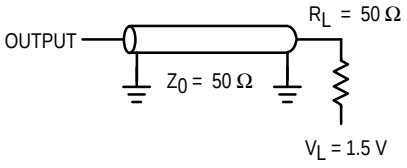


Figure 1A

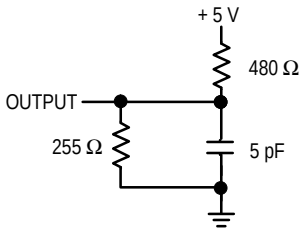


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, V_{CCQ} = 3.3 V or 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

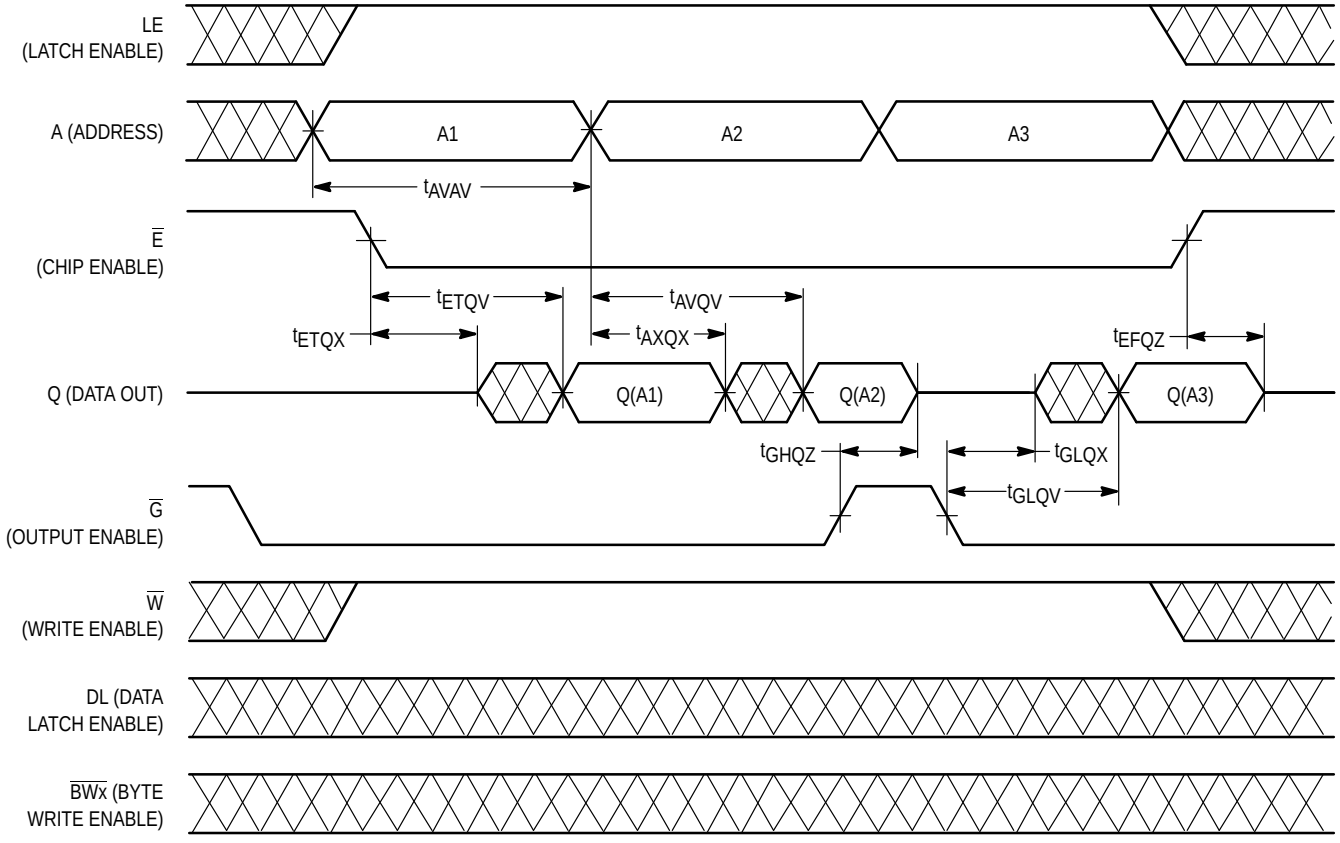
Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	6
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	2	9	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	8	2	10		
Power Up Time	t_{ETICCA}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. Write Enable is equal to V_{IH} for all read cycles.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All read cycle timing is referenced from the last valid address to the first transitioning address.
6. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

ASYNCHRONOUS READ CYCLES



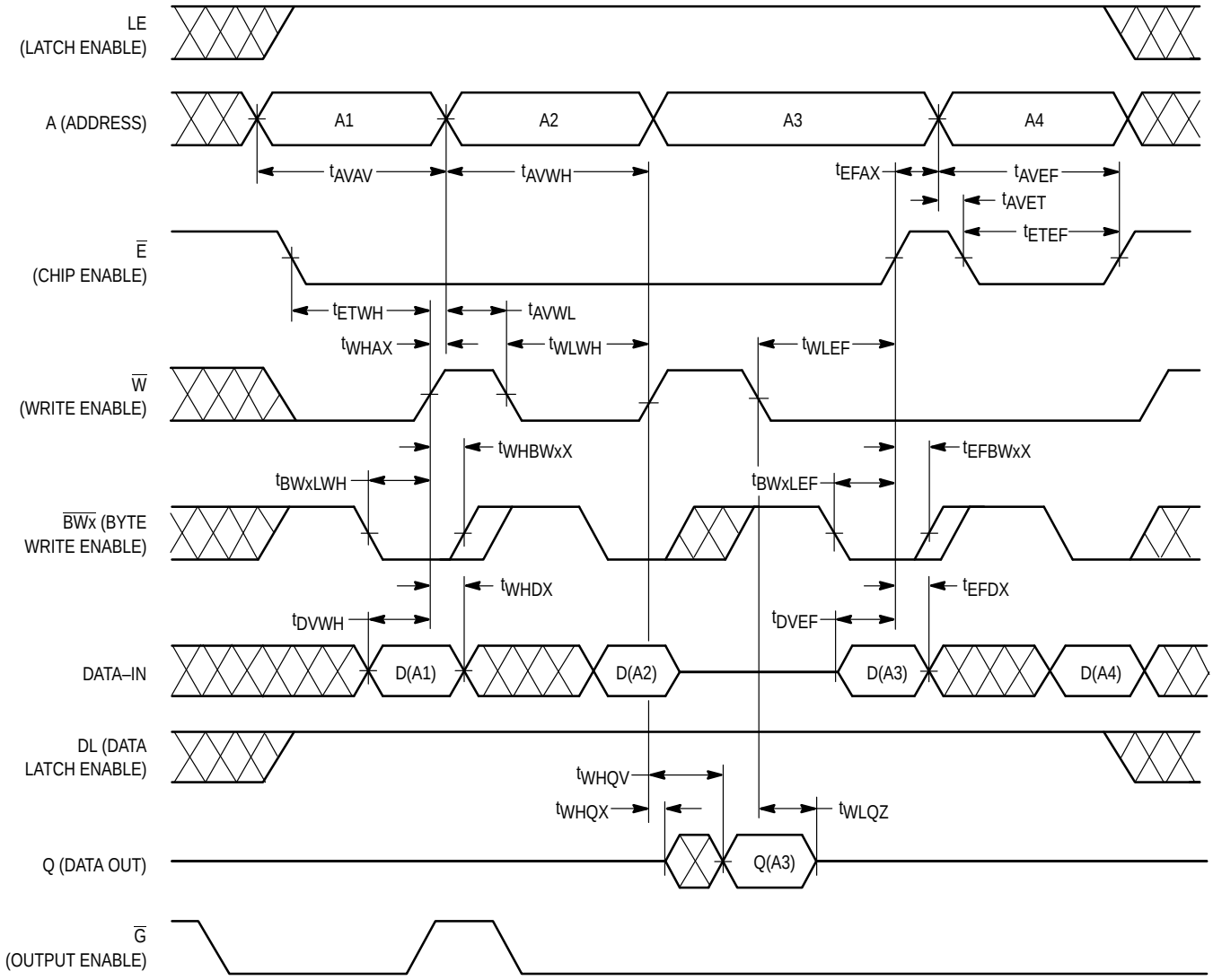
ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	6
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to E, $\overline{E}$ “False”	t_{AVEF}	10	—	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ “True”	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ “False”	t_{DVEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		2
Byte Write Low to E, $\overline{E}$ “False”	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Hold Times:										ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ “False” to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ “False” to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ “False” to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
Write Pulse Width:										ns	
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	18	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ High to Output High–Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:

1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low.
3. Write must be equal to V_{IH} for all address transitions.
4. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
5. EF is defined by $\overline{E}$ going high or E going low.
6. All write cycle timing is referenced from the last valid address to the first transitioning address.
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

ASYNCHRONOUS WRITE CYCLE

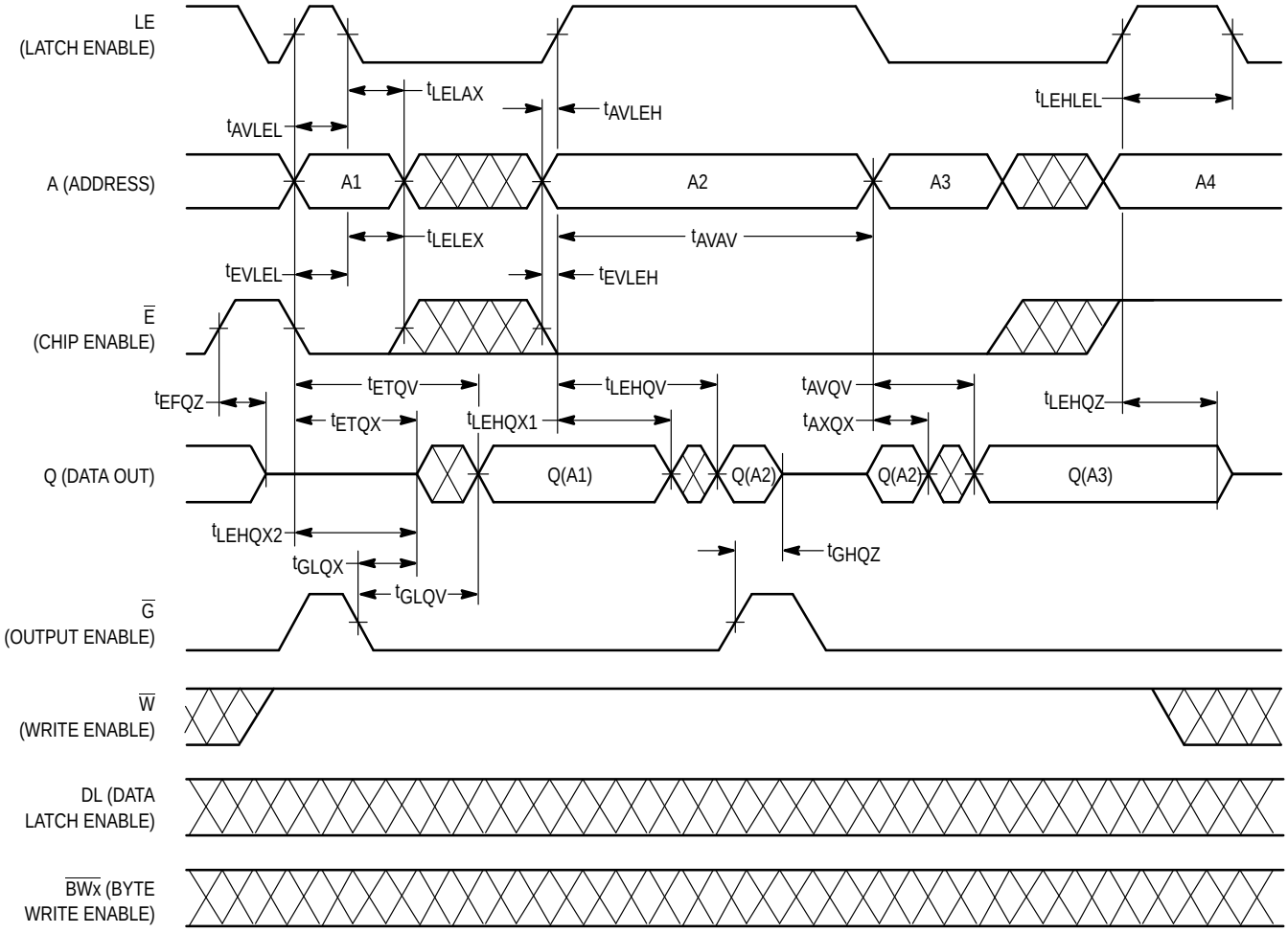


LATCHED READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		5
LE High to Output Valid	t_{LEHQV}	—	12	—	15	—	20	—	25		6
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Setup Times:										ns	
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		6
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		6
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Hold Times:										ns	6
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—	3	—		
Output Hold:										ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—	4	—		
LE High to Output Invalid	t_{LEHQX1}	4	—	4	—	4	—	4	—		
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
LE High to Output Active	t_{LEHQX2}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	2	10	2	10		
LE High to Output High–Z	t_{LEHQZ}	2	9	2	9	2	10	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	8	2	10		

NOTES:
1. Write Enable is equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. Addresses valid prior to or coincident with $\overline{E}$ going low and E going high
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



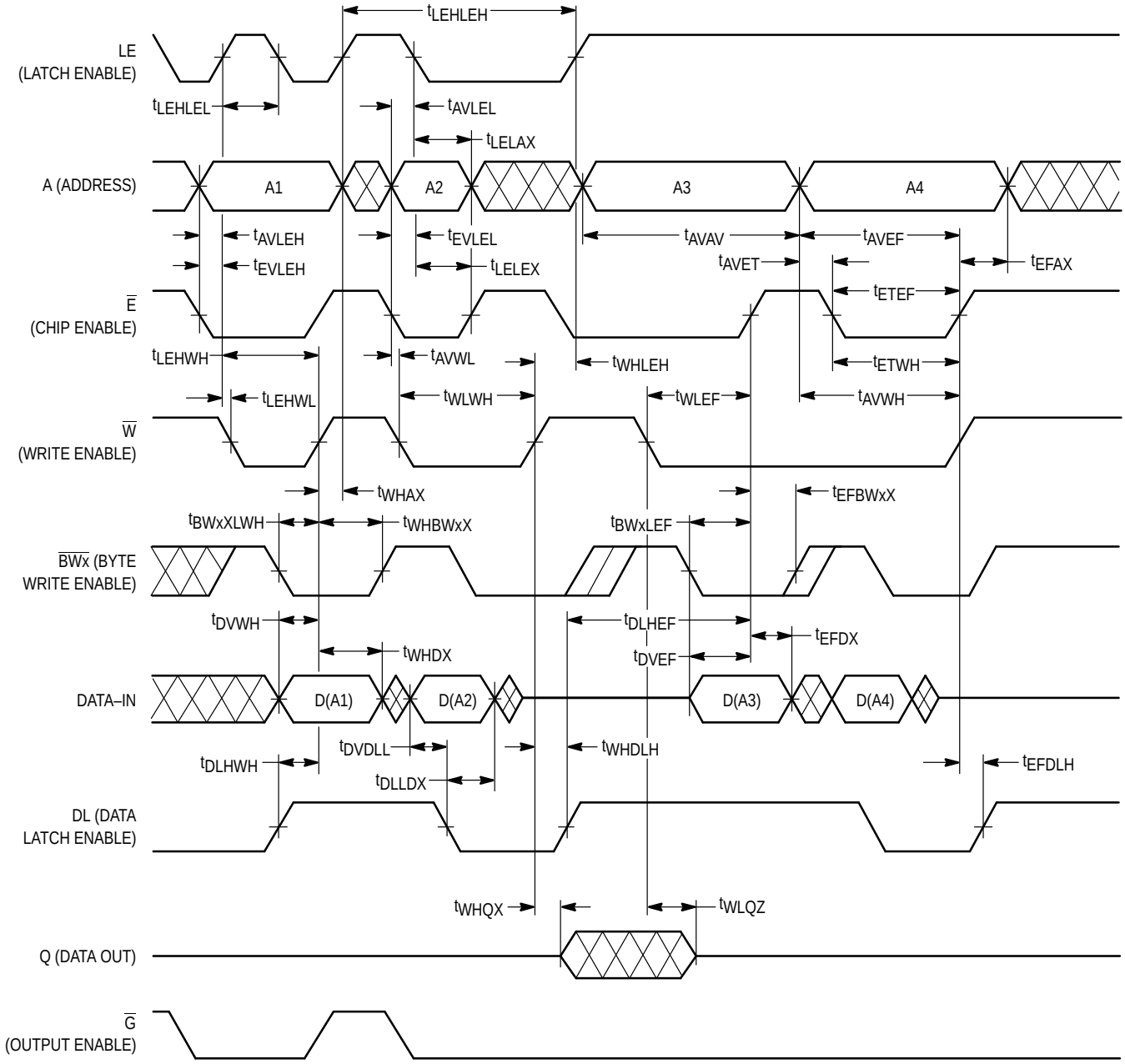
LATCHED WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times:										ns	5
Address Valid to Address Valid	t_{AVAV}	15	—	15	—	20	—	25	—		
LE High to LE High	t_{LEHLEH}	15	—	15	—	20	—	25	—		
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to End of Write	t_{AVEF}	10	—	13	—	15	—	20	—		
E, $\overline{E}$ “Valid” to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ “Valid” to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
LE High to $\overline{W}$ Low	t_{LEHWL}	0	—	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ “True”	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ “False”	t_{DVEF}	5	—	6	—	8	—	10	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	8	—	10	—		
DL High to E, $\overline{E}$ “False”	t_{DLHEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write Low to E, $\overline{E}$ “False”	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		
Hold Times:										ns	
LE Low to E, $\overline{E}$ “Invalid”	t_{LELEX}	3	—	3	—	3	—	3	—		5
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		5
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ “False” to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ “False” to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ “False” to DL High	t_{EFDLH}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ “False” to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to LE High	t_{WHLEH}	0	—	0	—	0	—	0	—		
Write Pulse Width:										ns	
LE High to $\overline{W}$ High	t_{LEHWH}	12	—	13	—	15	—	20	—		6
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:

1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remians at V_{IH} while $\overline{W}$ is low.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

LATCHED WRITE CYCLES



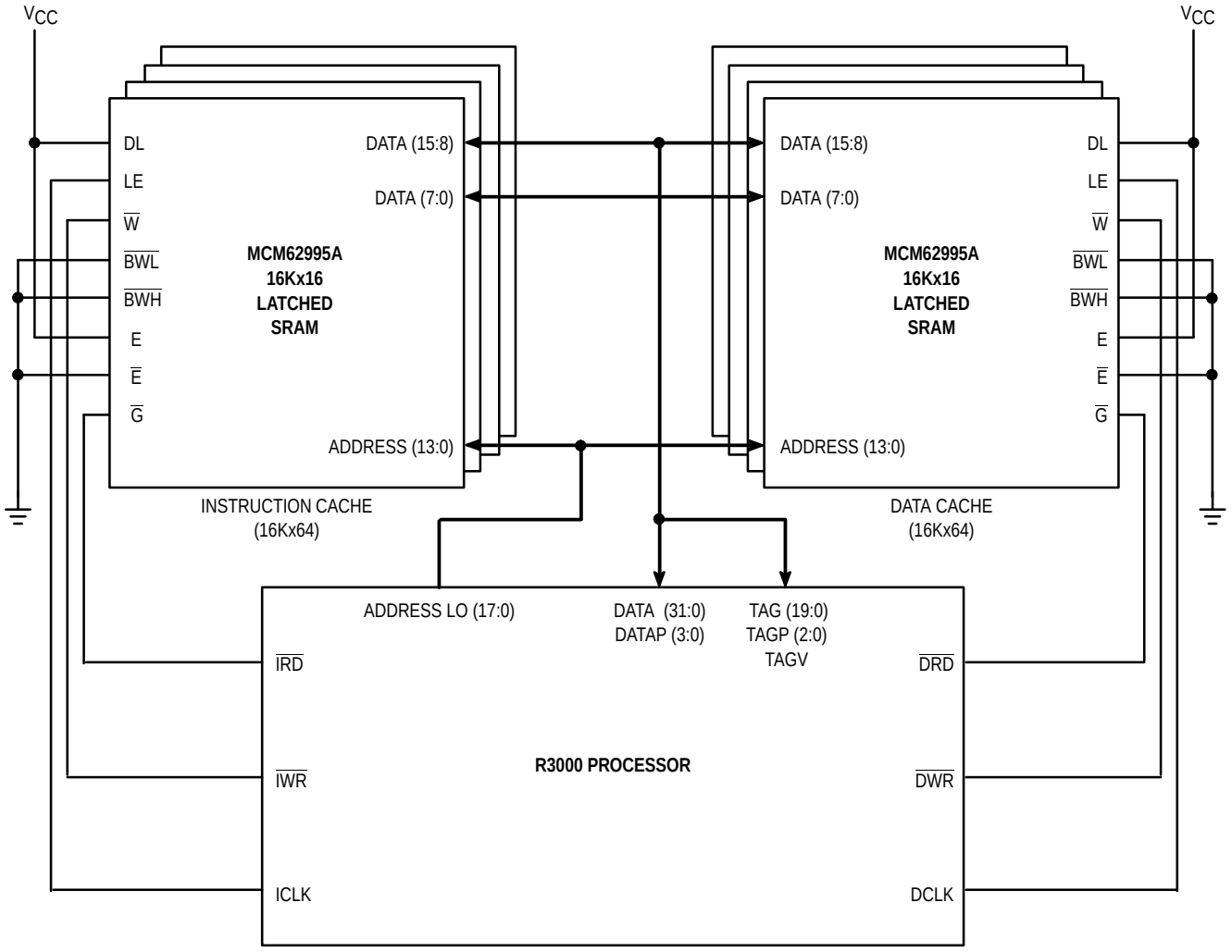


Figure 2. R3000 Application Example with 128K Byte Segregated Instruction/Data Cache Using Eight Motorola MCM62995A Latched SRAMs

ORDERING INFORMATION
(Order by Full Part Number)

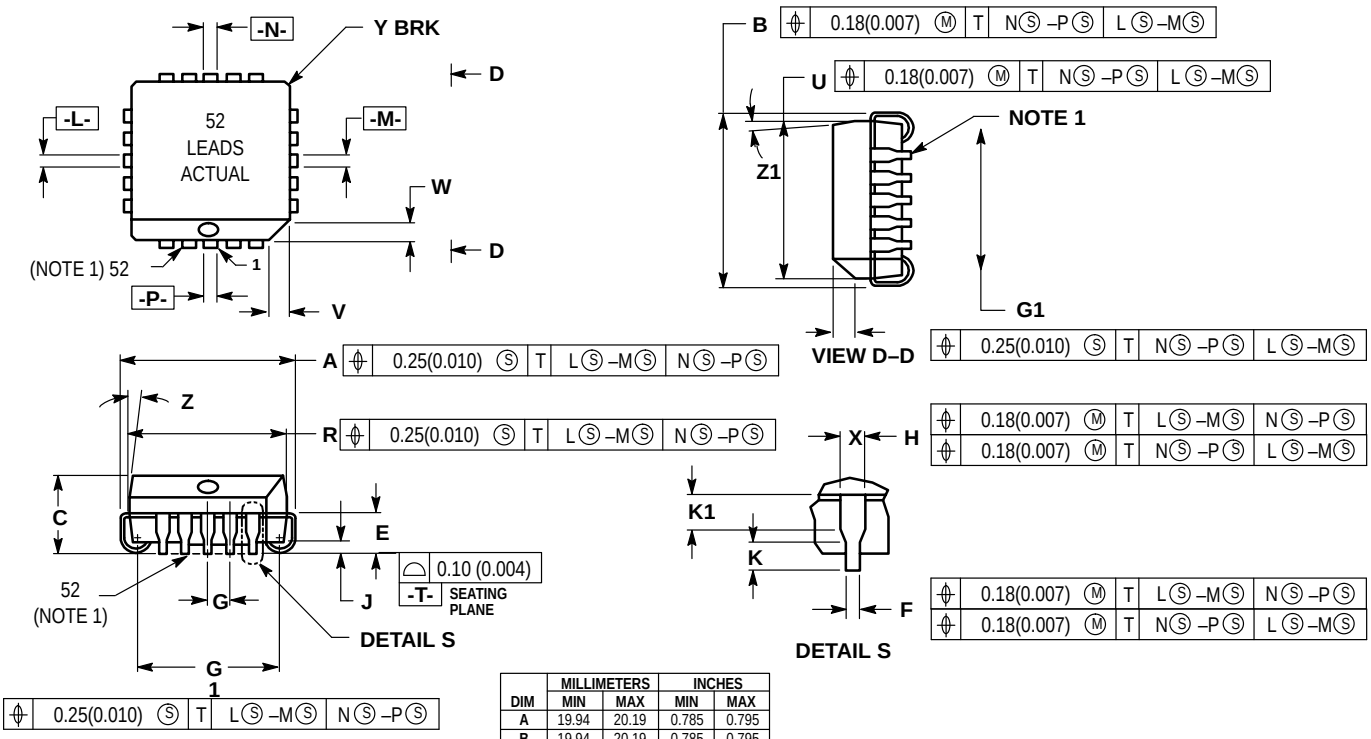
MCM 62995A FN XX

- MCM — Motorola Memory Prefix
- 62995A — Part Number
- FN — Package (FN = PLCC)
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns 25 = 25 ns)

Full Part Numbers — MCM62995AFN12 MCM62995AFN15 MCM62995AFN20 MCM62995AFN25

PACKAGE DIMENSIONS

FN PACKAGE
52–LEAD PLCC
CASE 778–02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	18.04	18.54	0.710	0.730
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4–32–1, Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.