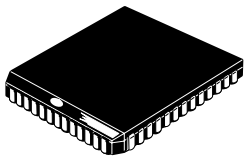
MCM62990A

16K x 16 Bit Synchronous Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM62990A is a 262,144 bit synchronous static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry. Inputs to the device fall into two categories: synchronous and asynchronous. All synchronous inputs pass through positive–edge–triggered registers controlled by a single clock input (K). The synchronous inputs include all addresses, the two chip enables (SE and $\overline{SE}$), and the synchronous write enable ($\overline{SW}$).

Asynchronous inputs include the asynchronous byte write strobes ($\overline{AWL}$ and $\overline{AWH}$), output enable ($\overline{G}$), data input (DQ0 – DQ15), and the data latch enable (DL). Input data can be asynchronously latched by DL to provide simplified data–in timings during write cycles.

Address and write control are registered on–chip which greatly simplifies write cycles. Dual write strobes ($\overline{AWL}$ and $\overline{AWH}$) are provided to allow individually writeable bytes. $\overline{AWL}$ controls DQ0 – DQ7, the lower bits while $\overline{AWH}$ controls DQ8 – DQ15, the upper bits. In addition, the AWs allow late write cycles to be aborted if they are "false" during the low period of the clock. Dual chip enables (SE and $\overline{SE}$) are provided, allowing address decoding to be accomplished on–chip when the device is used in a dual bank mode.

An input data latch is provided. When data latch enable (DL) is high, the data latch is in the transparent state. When DL is low, the data latch is in the latched state. This data input latch simplifies write cycles by guaranteeing data hold time in a simple fashion.

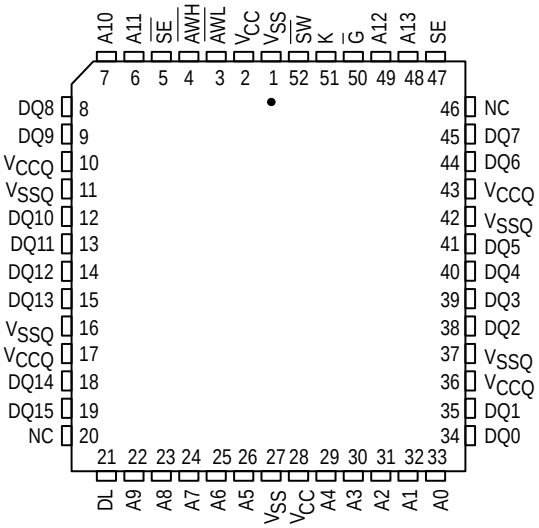
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, one set of power pins is electrically isolated from the other two and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62990A will be available in a 52 pin plastic leaded chip carrier (PLCC).

Typical applications for this device are cache memory and tag RAMs, memory in systems which are pipelined and systems which require wide data bus widths and reduced parts count.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Clock Controlled Registered Address, Write Control, and Dual Chip Enables
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

PIN ASSIGNMENT



PIN NAMES

A0 – A13	Address Inputs
K	Clock Input
DL	Data Latch Enable
$\overline{SW}$	Synchronous Write Enable
$\overline{AWL}$	Lower Byte Async Write Strobe
$\overline{AWH}$	Upper Byte Async Write Strobe
SE	Synchronous Chip Enable
$\overline{SE}$	Synchronous Chip Enable
$\overline{G}$	Asynchronous Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

REV 1
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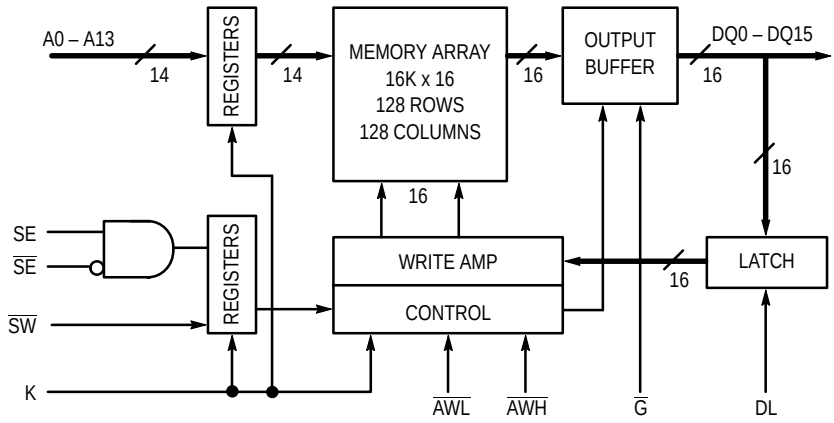
BLOCK DIAGRAM



TRUTH TABLE (See Notes)

SEs	$\overline{SW}$	$\overline{AWL}$	$\overline{AWH}$	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	H	X	Write Cycle All Bits Transparent Data In	I_{CC}	High–Z
T	L	H	H	X	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	H	X	Write Cycle Lower 8 Bits Transparent Data In	I_{CC}	High–Z
T	L	H	L	L	X	Write Cycle Upper 8 Bits Latched Data In	I_{CC}	High–Z

NOTES:
1. True (T) is SE = 1 and $\overline{SE}$ = 0.
2. Registered inputs (Addresses, $\overline{SW}$, SE, and $\overline{SE}$) satisfy the specified setup and hold times about the rising edge of clock (K). Data–in satisfies the specified setup and hold times for DL.
3. A transparent write cycle is defined by DL high during the write cycle.
4. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified setup and hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, $T_A = 0$ to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}**	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible) (V_{CCQ} must be ≤ V_{CC} at all times, including power up.)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)
** V_{CC} must be ≥ V_{CCQ} at all times, including power up.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G} = V_{IH}$)	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G} = V_{IH}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current ($\overline{E} = V_{IH}$, $E = V_{IL}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 3.3 V or 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Notes 2 and 3)

Parameter	Symbol	62990A–12		62990A–15		62990A–20		62990A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Times Clock High to Clock High	t_{KHKH}	15	—	15	—	20	—	25	—	ns	
Access Times										ns	4
Clock High to Output Valid	t_{KHQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Aborted Write Cycles										ns	
Clock Low to Asynchronous Write Strobes ($\overline{AWL}$, $\overline{AWH}$) High	t_{KLAWxH}	—	0	—	0	—	0	—	0		
Clock High to $\overline{AWx}$ Invalid	t_{KHAWxL}	2	—	2	—	2	—	2	—		
Output Buffer Control										ns	
Asynchronous Output Enable ($\overline{G}$) High to Output High Z	t_{GHQZ}	2	5	2	5	2	5	2	5		1
$\overline{G}$ Low to Output Low Z	t_{GLQX}	2	—	2	—	2	—	2	—		1
Reads:											
Clock (K) High to Output Low Z After Deselect or Write	t_{KHQX1}	8	—	8	—	8	—	8	—		1
Data Out Hold After Clock High	t_{KHQX2}	5	—	5	—	5	—	5	—		5
Writes:											
K High to Output High Z After Read	t_{KHQZ}	3	10	3	10	3	10	3	10		1
Clock										ns	
Clock High Time	t_{KHKL}	4	—	4	—	4	—	4	—		
Clock Low Time	t_{KLKH}	7	—	8	—	10	—	10	—		
Setup Times										ns	
Address Valid to Clock High	t_{AVKH}	3	—	3	—	3	—	3	—		5
Synchronous Write ($\overline{SW}$) Valid to Clock High	t_{SWVKH}	3	—	3	—	3	—	3	—		5
Synchronous Enables (SE, $\overline{SE}$) Valid to Clock High	t_{SEVKH}	3	—	3	—	3	—	3	—		5
Writes:											
Data–In Valid to Clock High	t_{DVKH}	5	—	6	—	6	—	7	—		2, 5
$\overline{AWL}$, $\overline{AWH}$ Low to Clock High	t_{AWxLKH}	6	—	6	—	6	—	7	—		5
Data Latch:											
Data–In Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		3, 5
Hold Times										ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—	2	—	2	—		5
Clock High to $\overline{SW}$ Invalid	t_{KHSWX}	3	—	3	—	3	—	3	—		5
Clock High to SE, $\overline{SE}$ Invalid	t_{KHSEX}	3	—	3	—	3	—	3	—		5
Writes:											
Clock High to Data–In Invalid	t_{KHDX}	2	—	2	—	2	—	2	—		2, 5
Clock High to $\overline{AWL}$, $\overline{AWH}$ High	t_{KHAWxH}	2	—	2	—	2	—	2	—		5
Clock High to DL High	t_{KHDLH}	2	—	2	—	2	—	2	—		3, 5
Data Latch:											
DL Low to Data–In Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		3, 5
DL High to Clock High	t_{DLHKH}	5	—	6	—	6	—	7	—		3, 5

NOTES:
1. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} and t_{GHQZ} is less than t_{GLQX} for a given device.
2. A transparent write cycle is defined by DL high during the write cycle.
3. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified hold time for the rising edge of clock (K).
4. Into rated load of 85 pF equivalent resistive load (see Figure 1A).
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for all rising edges of clock (K) or falling edges of data latch enable (DL).

AC TEST LOADS

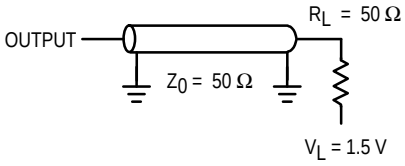


Figure 1A

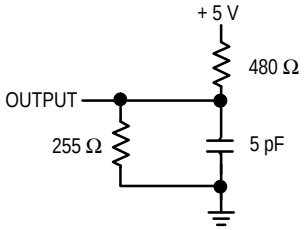
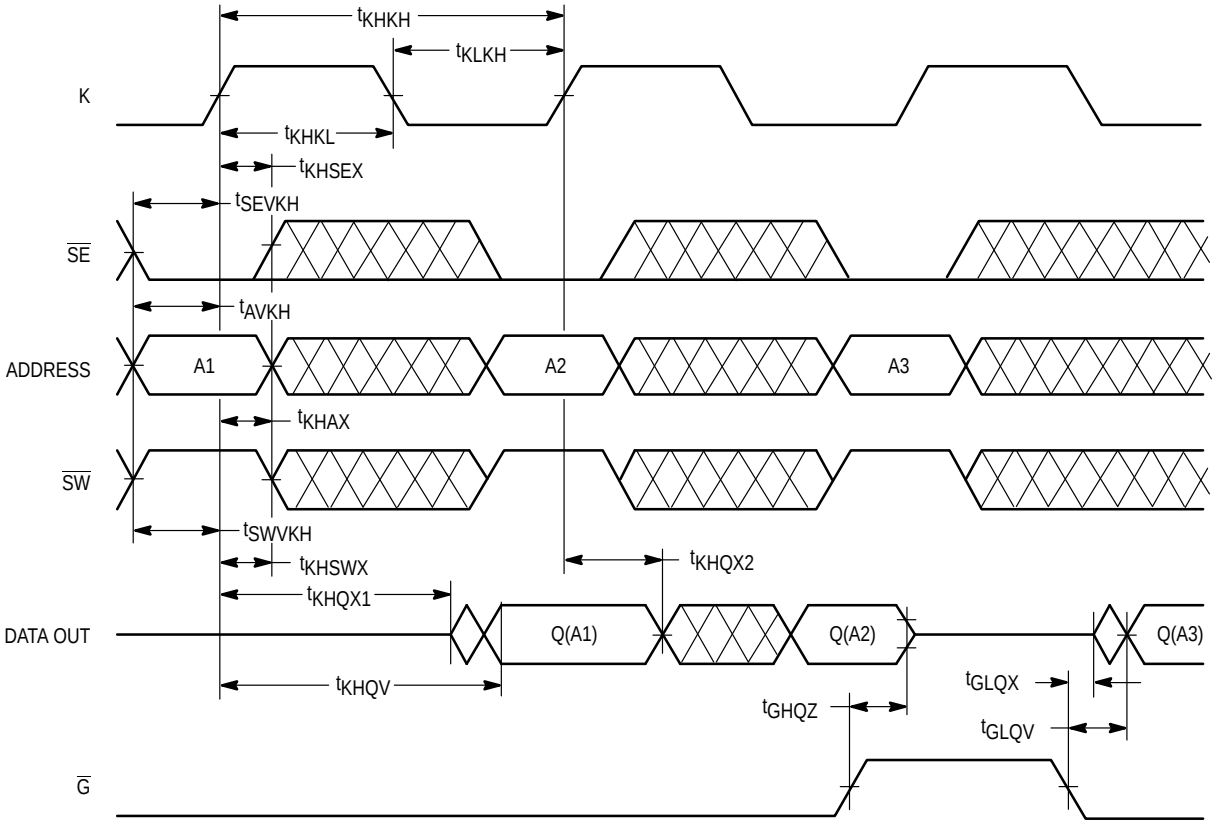
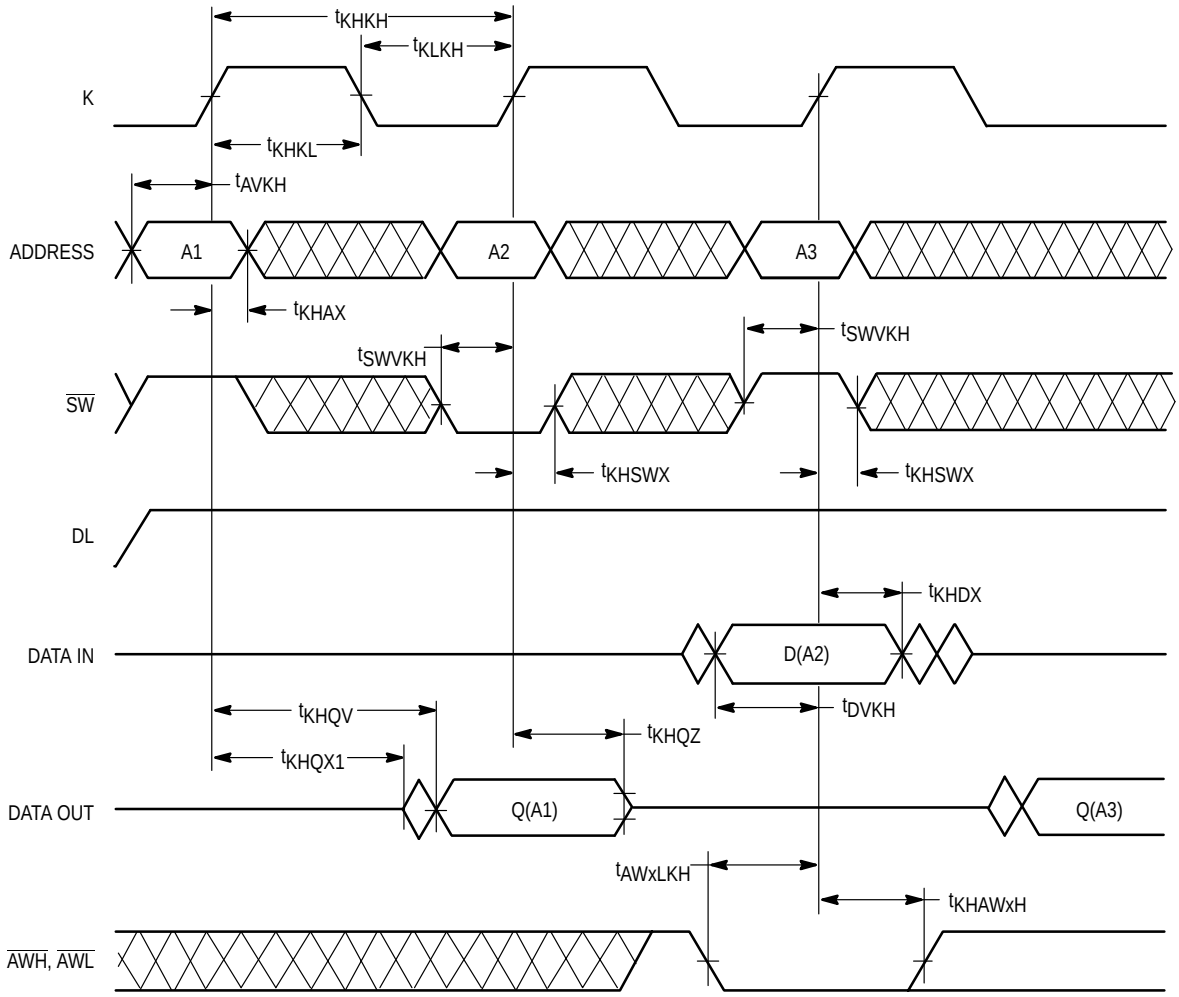


Figure 1B

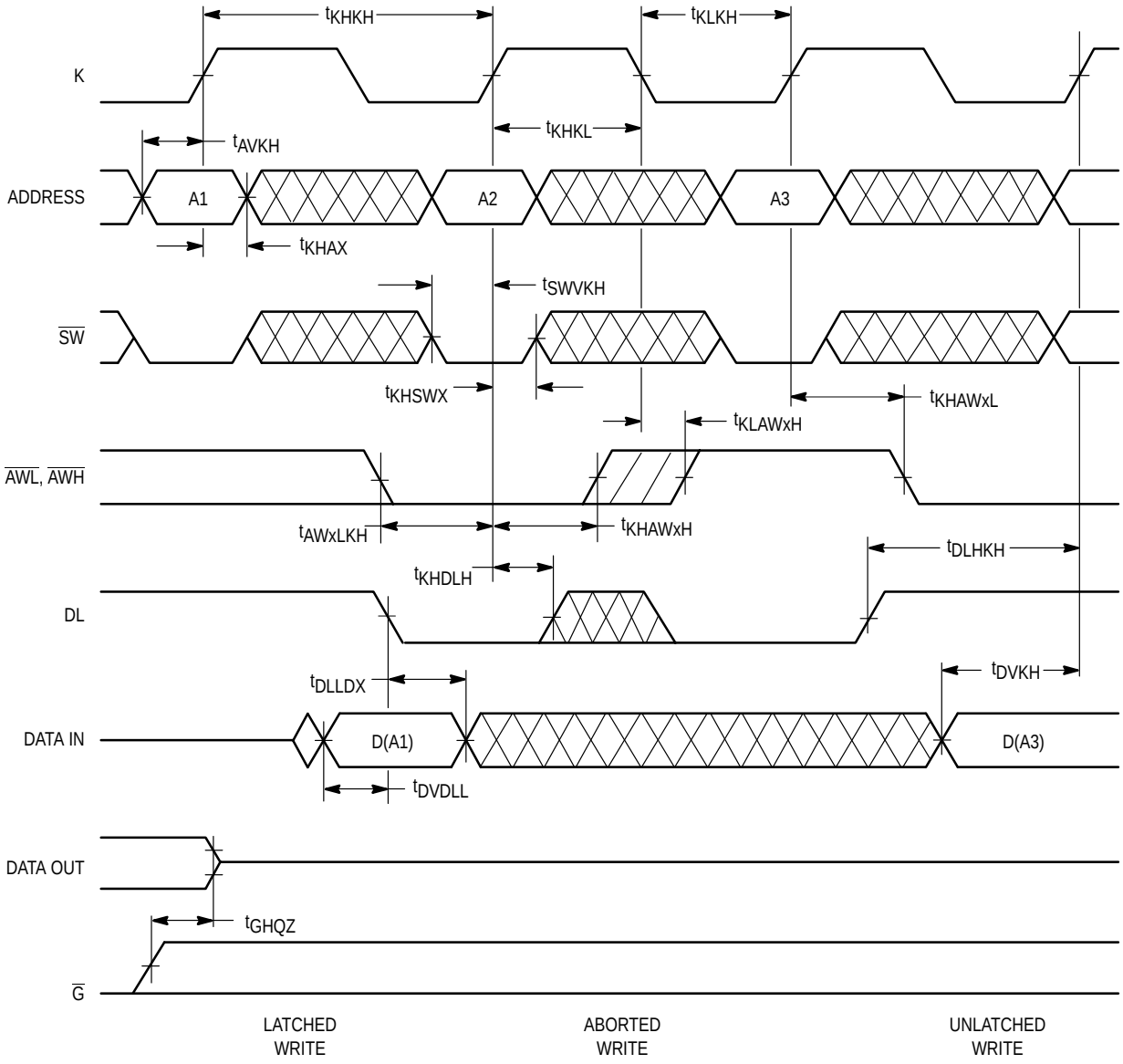
READ CYCLES



READ–UNLATCHED WRITE–READ CYCLES



WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

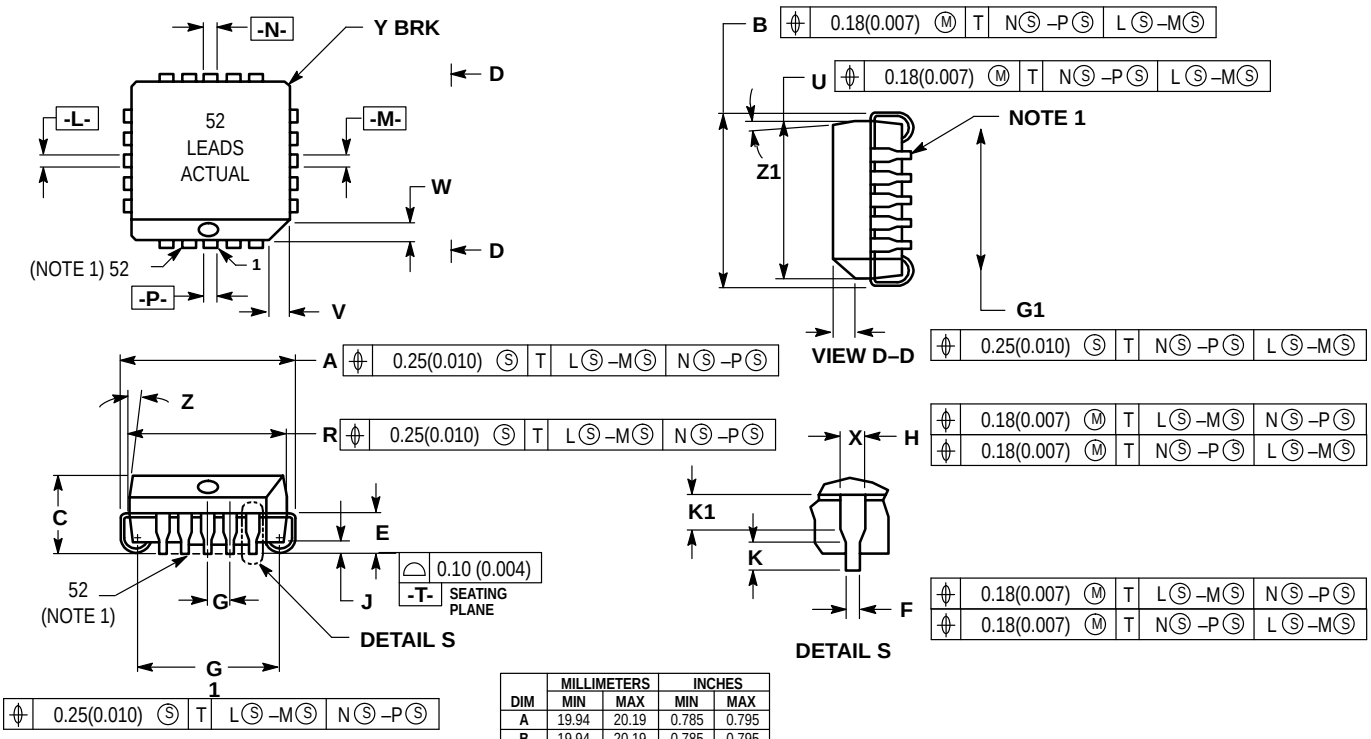
MCM 62990A FN XX

- MCM — Motorola Memory Prefix
- 62990A — Part Number
- FN — Package (FN = PLCC)
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)

Full Part Numbers — MCM62990AFN12 MCM62990AFN15 MCM62990AFN20 MCM62990AFN25

PACKAGE DIMENSIONS

FN PACKAGE
52–LEAD PLCC
CASE 778–02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	18.04	18.54	0.710	0.730
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

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