

# 1M x 4 Bit Static Random Access Memory

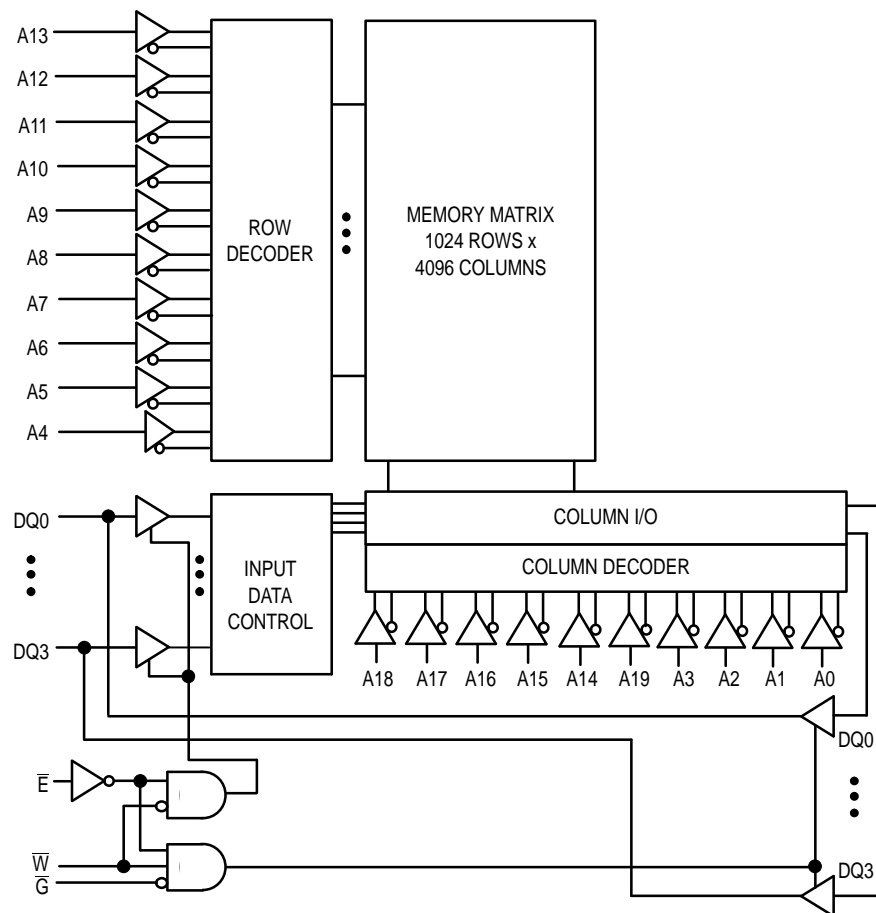
The MCM6249 is a 4,194,304 bit static random access memory organized as 1,048,576 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6249 is equipped with chip enable ( $\bar{E}$ ) and output enable ( $\bar{G}$ ) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

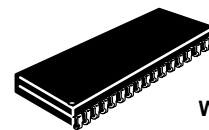
The MCM6249 is available in a 400 mil, 32-lead surface-mount SOJ package.

- Single 5 V  $\pm$  10% Power Supply
- Fast Access Time: 20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Power Operation: 190/175/160 mA Maximum, Active AC

**BLOCK DIAGRAM**



## MCM6249



**WJ PACKAGE**  
400 MIL SOJ  
CASE 857A-02

**PIN ASSIGNMENT**

A7	1	32	A1
A8	2	31	A0
A9	3	30	A5
A17	4	29	A4
A6	5	28	A19
$\bar{E}$	6	27	$\bar{G}$
DQ0	7	26	DQ3
VCC	8	25	VSS
VSS	9	24	VCC
DQ1	10	23	DQ2
$\bar{W}$	11	22	A2
A13	12	21	A16
A18	13	20	A15
A10	14	19	A14
A11	15	18	A3
A12	16	17	NC

**PIN NAMES**

A0 – A19	Address Inputs
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
$\bar{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
NC	No Connection
VCC	+ 5 V Power Supply
VSS	Ground

**TRUTH TABLE** (X = Don't Care)

$\bar{E}$	$\bar{G}$	$\bar{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	$I_{SB1}, I_{SB2}$
L	H	H	Output Disabled	High-Z	—	$I_{CCA}$
L	L	H	Read	D <sub>out</sub>	Read	$I_{CCA}$
L	X	L	Write	High-Z	Write	$I_{CCA}$

**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to $V_{SS}$	$V_{CC}$	- 0.5 to + 7.0	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$	$V_{in}, V_{out}$	- 0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	$I_{out}$	± 20	mA
Power Dissipation	$P_D$	1.0	W
Temperature Under Bias	$T_{bias}$	- 10 to + 85	°C
Operating Temperature	$T_A$	0 to + 70	°C
Storage Temperature — Plastic	$T_{stg}$	- 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	- 0.5*	—	0.8	V

\*  $V_{IL} \text{ (min)} = -0.5 \text{ V dc}$ ;  $V_{IL} \text{ (min)} = -2.0 \text{ V ac}$  (pulse width  $\leq 2.0 \text{ ns}$ ).

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0 \text{ to } V_{CC}$ )	$I_{kg}(I)$	—	± 1.0	μA
Output Leakage Current ( $\bar{E} = V_{IH}$ , $V_{out} = 0 \text{ to } V_{CC}$ )	$I_{kg}(O)$	—	± 1.0	μA
Output Low Voltage ( $I_{OL} = +8.0 \text{ mA}$ )	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = -4.0 \text{ mA}$ )	$V_{OH}$	2.4	—	V

**POWER SUPPLY CURRENTS**

Parameter	Symbol	Min	Typ	Max	Unit
AC Active Supply Current ( $I_{out} = 0 \text{ mA}$ , $V_{CC} = \text{max}$ )	$I_{CC}$	—	175	190	mA
		—	160	175	
		—	145	160	
AC Standby Current ( $V_{CC} = \text{max}$ , $\bar{E} = V_{IH}$ , No other restrictions on other inputs)	$I_{SB1}$	—	50	60	mA
		—	40	50	
		—	35	40	
CMOS Standby Current ( $\bar{E} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$ ) ( $V_{CC} = \text{max}$ , $f = 0 \text{ MHz}$ )	$I_{SB2}$	—	10	15	mA

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, T<sub>A</sub> = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs			
	$\bar{E}$ , $\bar{G}$ , $\bar{W}$	C <sub>in</sub>	4	6
Input/Output Capacitance		C <sub>ck</sub>	5	8
	DQ	C <sub>I/O</sub>	5	8

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V  
 Input Rise/Fall Time ..... 2 ns  
 Input Timing Measurement Reference Level ..... 1.5 V

Output Timing Measurement Reference Level ..... 1.5 V  
 Output Load ..... See Figure 1A

### READ CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t <sub>AVAV</sub>	20	—	25	—	35	—	ns	2, 3
Address Access Time	t <sub>AVQV</sub>	—	20	—	25	—	35	ns	
Enable Access Time	t <sub>ELQV</sub>	—	20	—	25	—	35	ns	4
Output Enable Access Time	t <sub>GLQV</sub>	—	6	—	8	—	10	ns	
Output Hold from Address Change	t <sub>AXQX</sub>	5	—	5	—	5	—	ns	
Enable Low to Output Active	t <sub>ELQX</sub>	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t <sub>GLQX</sub>	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t <sub>EHQZ</sub>	0	9	0	10	0	12	ns	5, 6, 7
Output Enable High to Output High–Z	t <sub>GHQZ</sub>	0	9	0	10	0	12	ns	5, 6, 7
Power Up Time	t <sub>ELICCH</sub>	0	—	0	—	0	—	ns	
Power Down Time	t <sub>EHICCL</sub>	—	20	—	25	—	35	ns	

#### NOTES:

1.  $\bar{W}$  is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with  $\bar{E}$  going low/ $\bar{E}$  going high.
5. At any given voltage and temperature, t<sub>EHQZ</sub> max < t<sub>ELQX</sub> min, and t<sub>GHQZ</sub> max < t<sub>GLQX</sub> min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ( $\bar{E} \leq V_{IL}$ ,  $\bar{G} \leq V_{IL}$ ).

### AC TEST LOADS

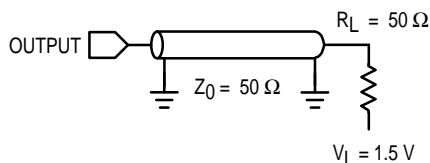


Figure 1A

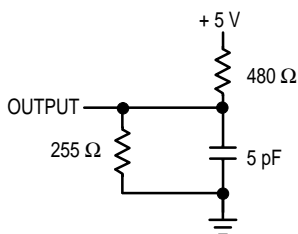
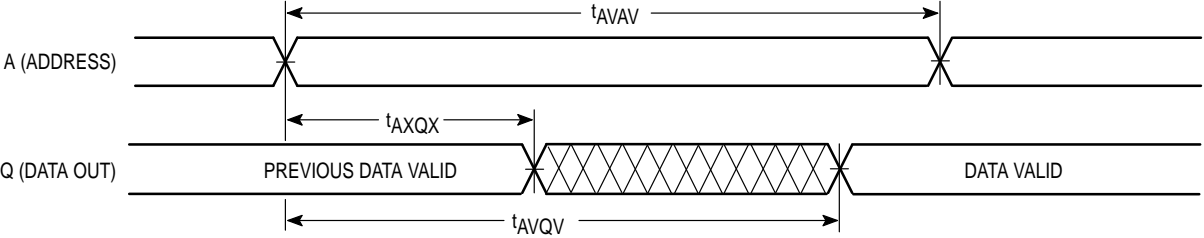


Figure 1B

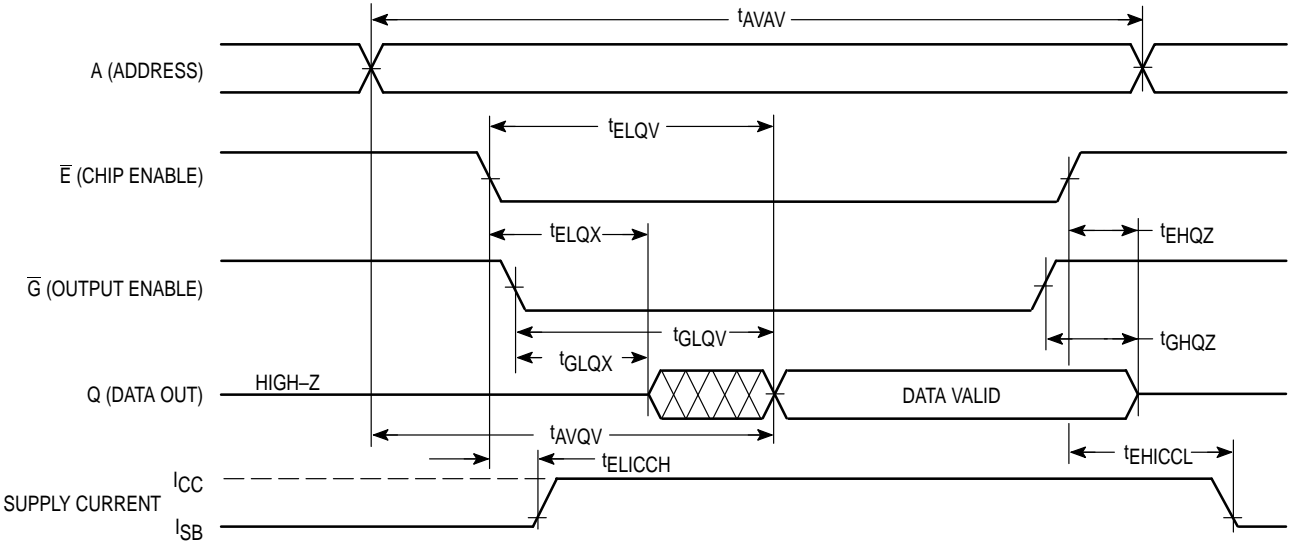
### TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

## READ CYCLE 1 (See Note 8)



### READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with  $\overline{E}$  going low/ $\overline{E}$  going high

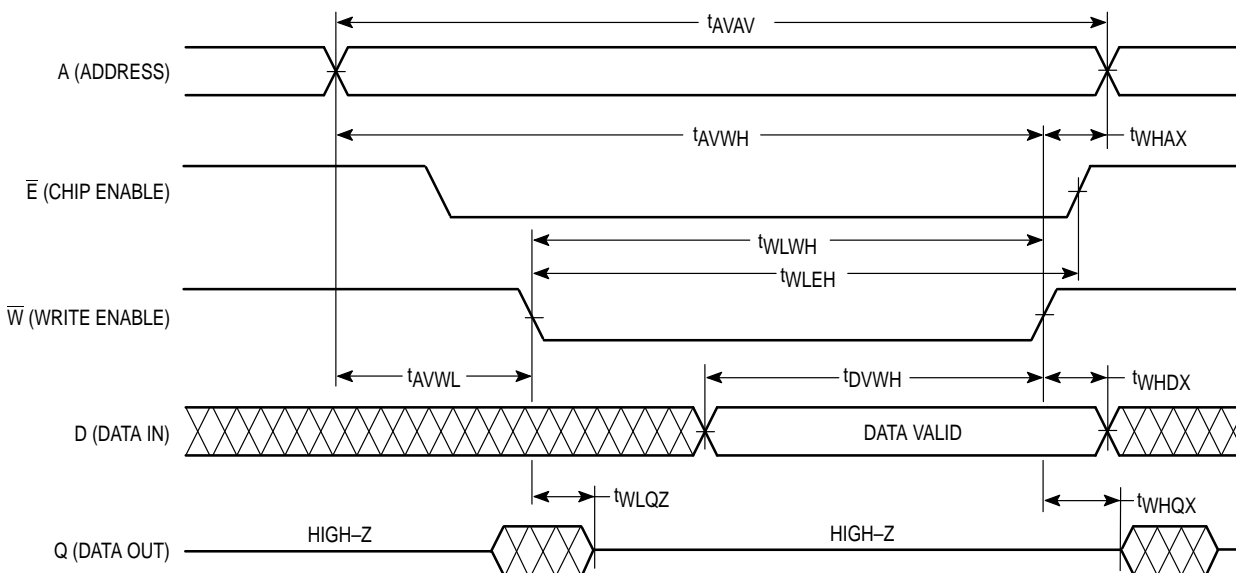
# **WRITE CYCLE 1** ( $\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	20	—	25	—	35	—	ns	4
Address Setup Time	$t_{AVWL}$	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	15	—	17	—	20	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	15	—	17	—	20	—	ns	
Data Valid to End of Write	$t_{DVWH}$	10	—	10	—	15	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	0	—	ns	
Write Low to Data High–Z	$t_{WLQZ}$	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	$t_{WHQX}$	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	$t_{WHAX}$	0	—	0	—	0	—	ns	

## NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured  $\pm 500$  mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature,  $t_{WLQZ}$  max <  $t_{WHQX}$  min both for a given device and from device to device.

## **WRITE CYCLE 1** ( $\overline{W}$ Controlled, See Notes 1, 2, and 3)



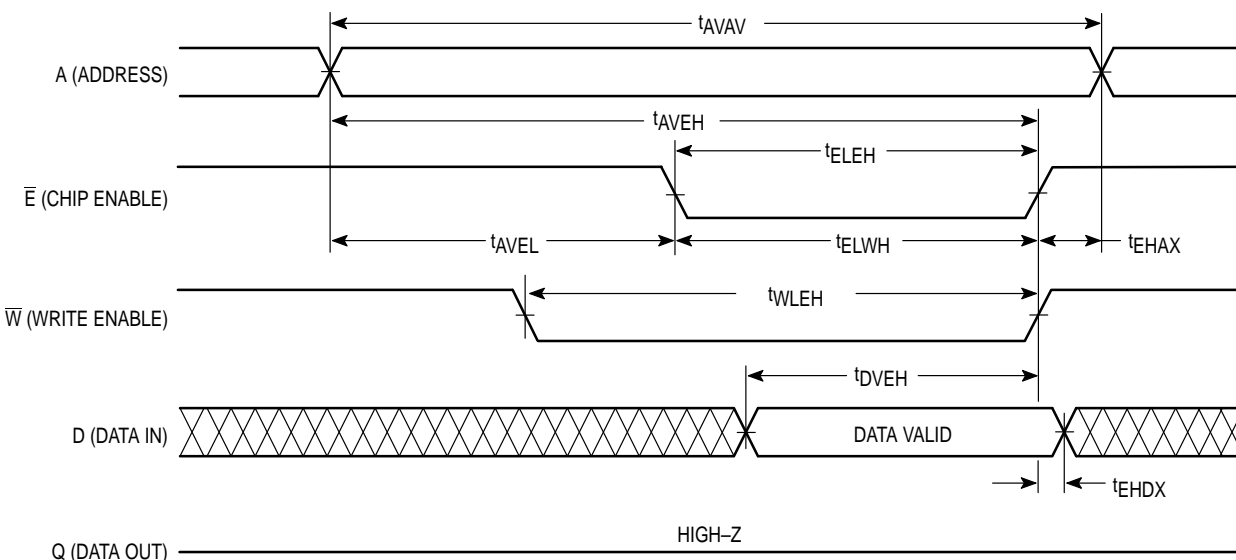
# **WRITE CYCLE 2** ( $\bar{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	20	—	25	—	35	—	ns	4
Address Setup Time	$t_{AVEL}$	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	15	—	17	—	20	—	ns	
Enable Pulse Width	$t_{ELEH}$ , $t_{ELWH}$	15	—	17	—	20	—	ns	5,6
Write Pulse Width	$t_{WLEH}$	15	—	17	—	20	—	ns	
Data Valid to End of Write	$t_{DVEH}$	10	—	10	—	15	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	0	—	ns	

## **NOTES:**

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\bar{G}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high impedance condition.
6. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high impedance condition.

## **WRITE CYCLE 2** ( $\bar{E}$ Controlled, See Notes 1, 2, and 3)



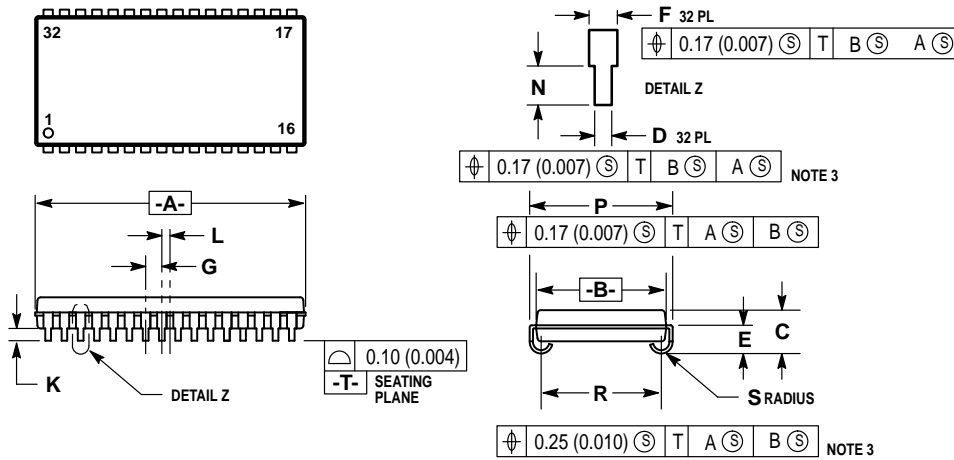
## **ORDERING INFORMATION** (Order by Full Part Number)

**MCM** **6249** **XX** **XX** **XX**  
 Motorola Memory Prefix \_\_\_\_\_  
 Part Number \_\_\_\_\_  
 Shipping Method (R2 = Tape and Reel, Blank = Rails)  
 Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)  
 Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6249WJ20 MCM6249WJ20R2  
 MCM6249WJ25 MCM6249WJ25R2  
 MCM6249WJ35 MCM6249WJ35R2

## PACKAGE DIMENSIONS


### WJ PACKAGE 400 MIL SOJ CASE 857A-02



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
6. 857A-01 IS OBSOLETE, NEW STANDARD 857A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.83	21.08	0.820	0.830
B	10.03	10.29	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.27	9.52	0.365	0.375
S	0.77	1.01	0.030	0.040

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**MCM6249/D**

