

512K x 8 Bit Static Random Access Memory

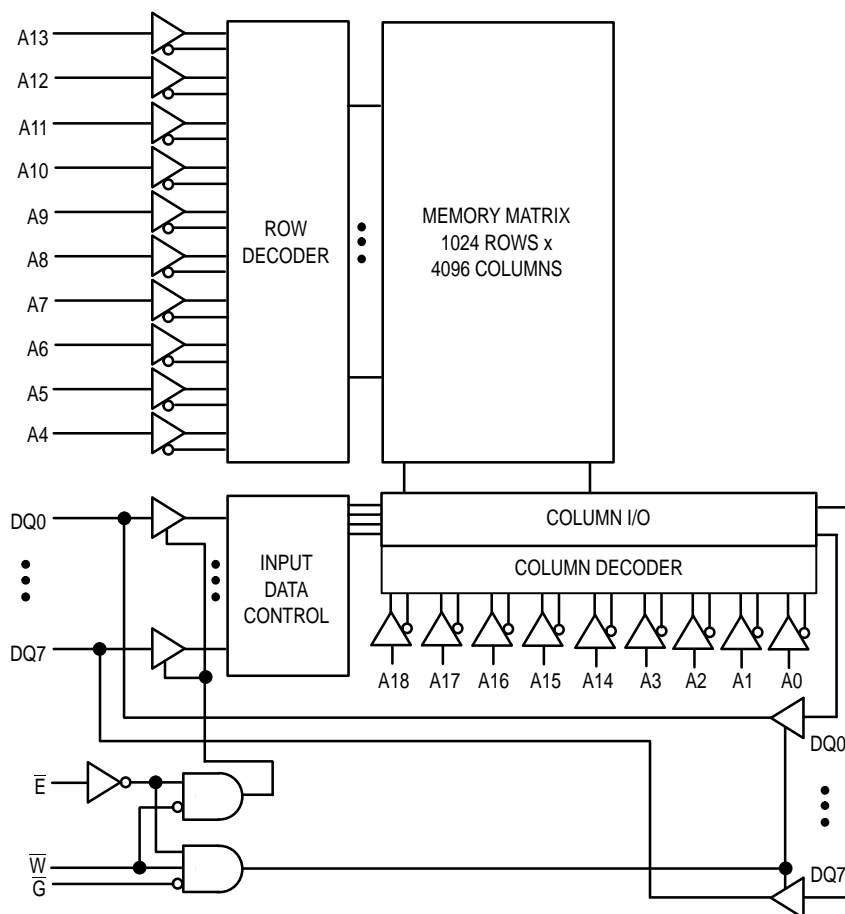
The MCM6246 is a 4,194,304 bit static random access memory organized as 524,288 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6246 is equipped with chip enable (\bar{E}) and output enable (\bar{G}) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

The MCM6246 is available in a 400 mil, 36-lead surface-mount SOJ package.

- Single 5 V \pm 10% Power Supply
- Fast Access Time: 20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Power Operation: 200/185/170 mA Maximum, Active AC

BLOCK DIAGRAM



MCM6246



WJ PACKAGE
400 MIL SOJ
CASE 893-01

PIN ASSIGNMENT

A6	1	36	NC
A7	2	35	A1
A8	3	34	A0
A9	4	33	A5
A17	5	32	A4
\bar{E}	6	31	\bar{G}
DQ0	7	30	DQ7
DQ1	8	29	DQ6
VCC	9	28	VSS
VSS	10	27	VCC
DQ2	11	26	DQ5
DQ3	12	25	DQ4
\bar{W}	13	24	A16
A18	14	23	A15
A10	15	22	A14
A11	16	21	A3
A12	17	20	A2
A13	18	19	NC

PIN NAMES

A0 – A18	Address Inputs
\bar{W}	Write Enable
\bar{G}	Output Enable
\bar{E}	Chip Enable
DQ0 – DQ7	Data Input/Output
NC	No Connection
VCC	+ 5 V Power Supply
VSS	Ground

TRUTH TABLE (X = Don't Care)

\bar{E}	\bar{G}	\bar{W}	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	I_{SB1} , I_{SB2}
L	H	H	Output Disabled	High-Z	—	I_{CCA}
L	L	H	Read	D _{out}	Read	I_{CCA}
L	X	L	Write	High-Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	- 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in} , V_{out}	- 0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	- 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	- 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	V_{IL}	- 0.5*	—	0.8	V

* V_{IL} (min) = - 0.5 V dc; V_{IL} (min) = - 2.0 V ac (pulse width ≤ 2.0 ns).

** V_{IH} (max) = $V_{CC} + 0.3 \text{ V}$ dc; V_{IH} (max) = $V_{CC} + 2.0 \text{ V}$ ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0 \text{ to } V_{CC}$)	$I_{lkg(I)}$	—	± 1.0	μA
Output Leakage Current ($\bar{E} = V_{IH}$, $V_{out} = 0 \text{ to } V_{CC}$)	$I_{lkg(O)}$	—	± 1.0	μA
Output Low Voltage ($I_{OL} = + 8.0 \text{ mA}$)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH} = - 4.0 \text{ mA}$)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
AC Active Supply Current ($I_{out} = 0 \text{ mA}$, $V_{CC} = \text{max}$)	I_{CC}	—	185	200	mA
		—	170	185	
		—	155	170	
AC Standby Current ($V_{CC} = \text{max}$, $\bar{E} = V_{IH}$, No other restrictions on other inputs)	I_{SB1}	—	55	60	mA
		—	45	50	
		—	35	40	
CMOS Standby Current ($\bar{E} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$) ($V_{CC} = \text{max}$, $f = 0 \text{ MHz}$)	I_{SB2}	—	10	15	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	
Input Capacitance	All Inputs Except Clocks and DQs	C _{in}	4	6	pF
	E, G, W	C _{ck}	5	8	
Input/Output Capacitance	DQ	C _{I/O}	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels	0 to 3.0 V	Output Timing Measurement Reference Level	1.5 V
Input Rise/Fall Time	2 ns	Output Load	See Figure 1A
Input Timing Measurement Reference Level	1.5 V		

READ CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t _{AVAV}	20	—	25	—	35	—	ns	2, 3
Address Access Time	t _{AVQV}	—	20	—	25	—	35	ns	
Enable Access Time	t _{ELQV}	—	20	—	25	—	35	ns	4
Output Enable Access Time	t _{GLQV}	—	6	—	8	—	10	ns	
Output Hold from Address Change	t _{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t _{ELQX}	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t _{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t _{EHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Output Enable High to Output High–Z	t _{GHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Power Up Time	t _{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t _{EHICCL}	—	20	—	25	—	35	ns	

NOTES:

1. W is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with E going low/E going high.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$).

AC TEST LOADS

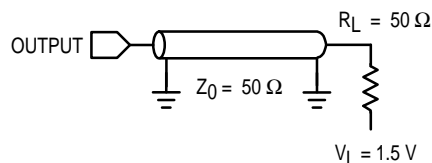


Figure 1A

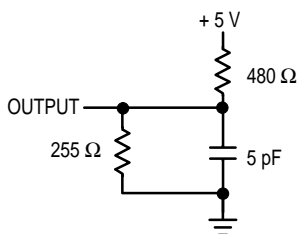
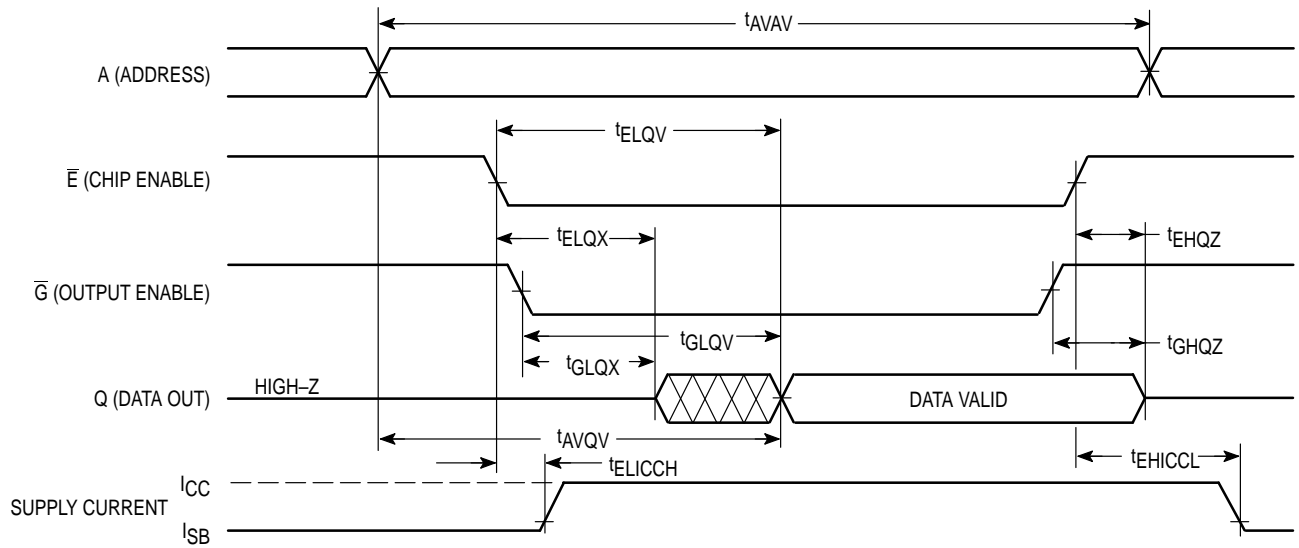


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 2 (See Note)



MOTOROLA FAST SRAM

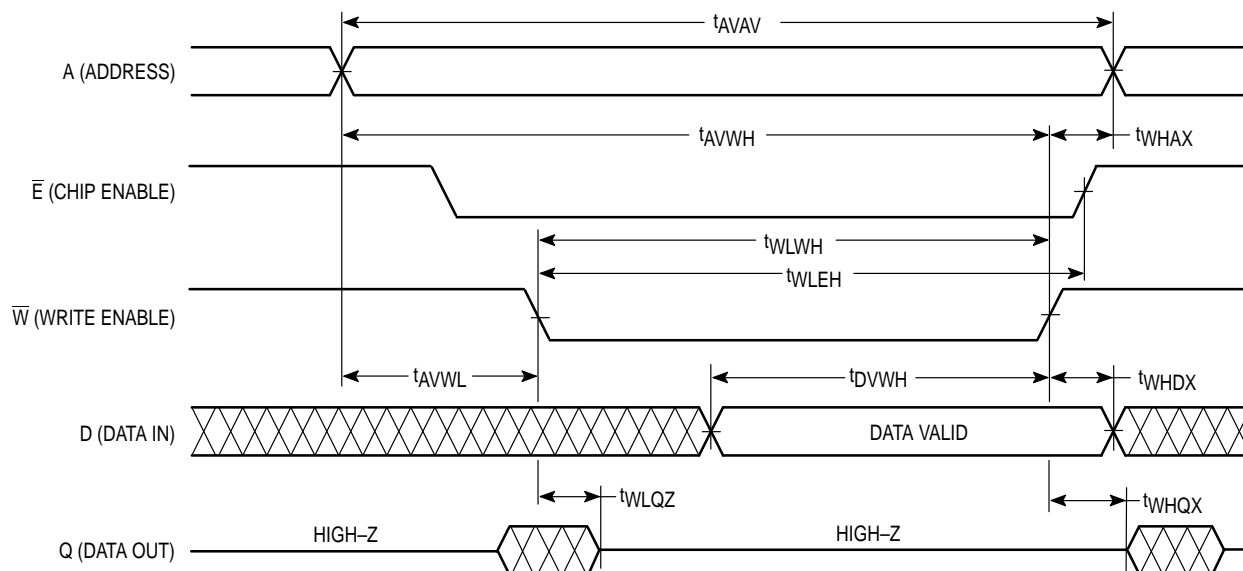
WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If \overline{G} goes low coincident with or after \overline{W} goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1, 2, and 3)



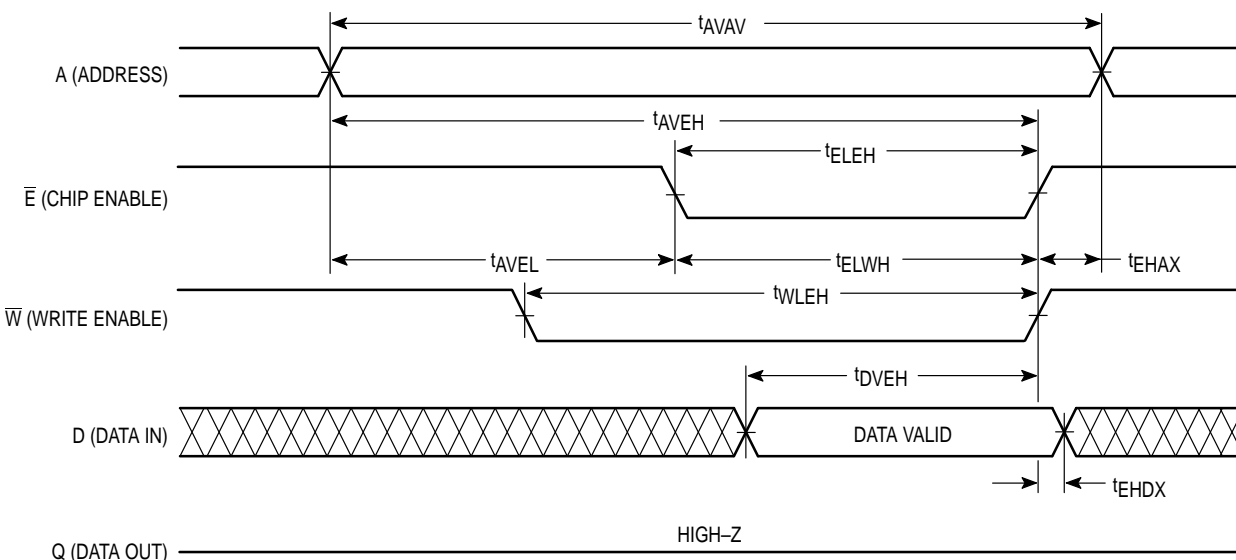
WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	ns	
Enable Pulse Width	t_{ELEH} , t_{ELWH}	15	—	17	—	20	—	ns	5,6
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If \bar{G} goes low coincident with or after \bar{W} goes low, the output will remain in a high-impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance condition.
6. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1, 2, and 3)



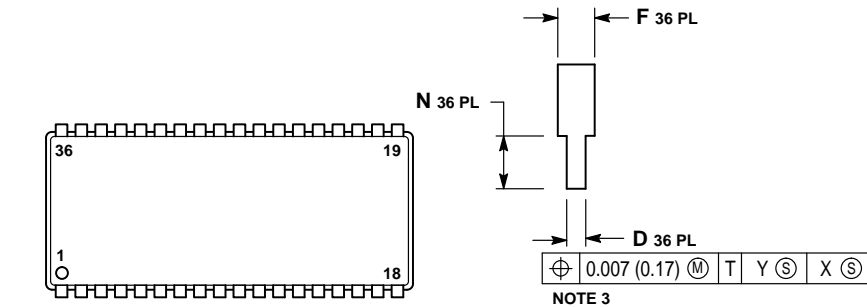
ORDERING INFORMATION (Order by Full Part Number)

MCM **6246** **XX** **XX** **XX**
 Motorola Memory Prefix _____
 Part Number _____
 Shipping Method (R2 = Tape and Reel, Blank = Rails)
 Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
 Package (WJ = 400 mil SOJ)

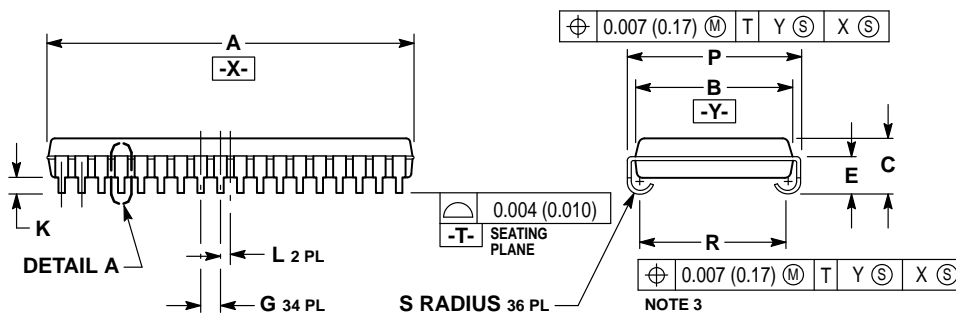
Full Part Numbers — MCM6246WJ20 MCM6246WJ20R2
 MCM6246WJ25 MCM6246WJ25R2
 MCM6246WJ35 MCM6246WJ35R2

PACKAGE DIMENSIONS


400 MIL SOJ
CASE 893-01



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. TO BE DETERMINED AT PLANE -T-.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
 5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.920	0.930	23.37	23.62
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.035	0.045	0.89	1.14
L	0.025 BASIC		0.64 BASIC	
N	0.030	0.045	0.77	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.28	9.52
S	0.030	0.040	0.77	1.01

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MOTOROLA

◇ CODELINE TO BE PLACED HERE

MCM6246/D

