MCM6226A

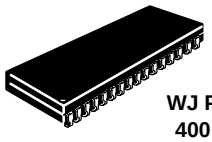
128K x 8 Bit Static Random Access Memory

The MCM6226A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226A is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

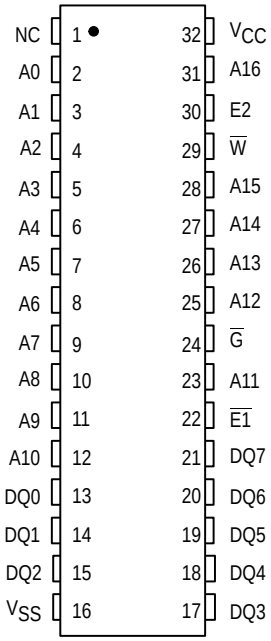
The MCM6226A is available in 400 mil, 32 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 180/160/150/140 mA Maximum, Active AC

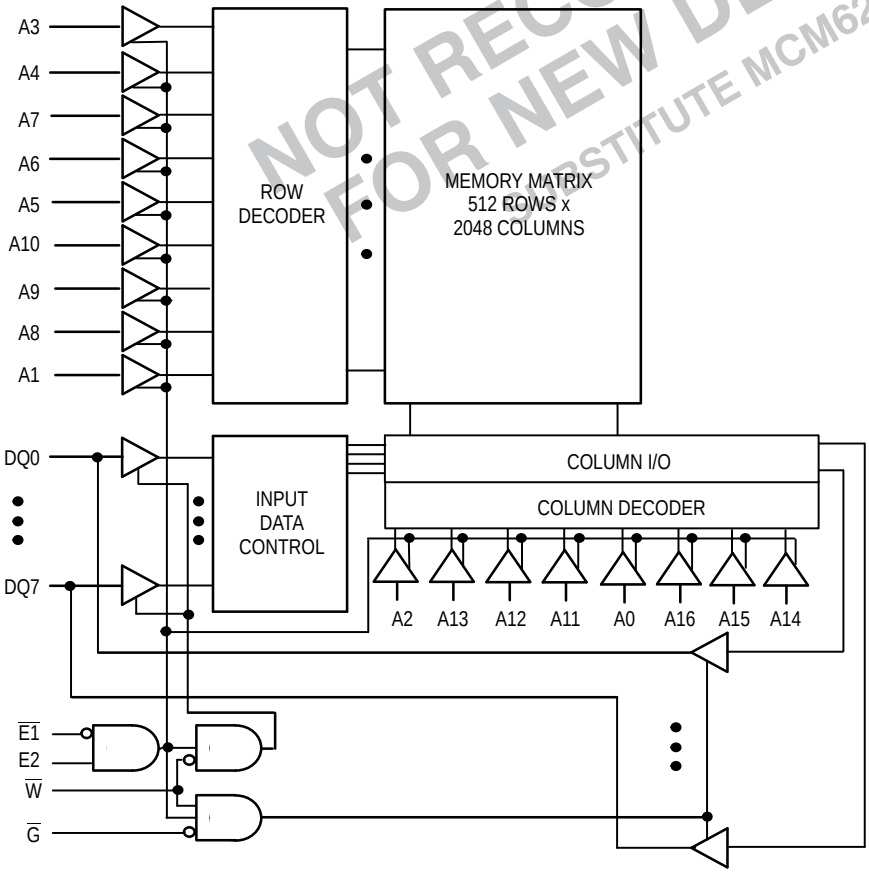


WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

REV 4
5/95

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High–Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} to 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ**	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
MCM6226A–20: t_{AVAV} = 20 ns		—	150	180	
MCM6226A–25: t_{AVAV} = 25 ns		—	135	160	
MCM6226A–35: t_{AVAV} = 35 ns		—	125	150	
MCM6226A–45: t_{AVAV} = 45 ns		—	120	140	
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f = f_{max})	I_{SB1}	—	7	20	mA
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	4	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
**Typical values are measured at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQ $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2 ns
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	6226A–20		6226A–25		6226A–35		6226A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	4
Address Access Time	t_{AVQV}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	—	35	—	45	ns	5
Output Enable Access Time	t_{GLQV}	—	8	—	10	—	15	—	15	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	0	12	0	15	ns	6, 7, 8
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	0	12	0	15	ns	6, 7, 8
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

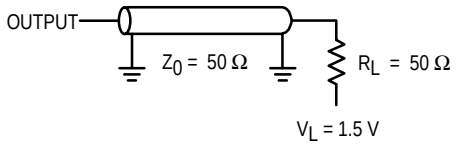


Figure 1A

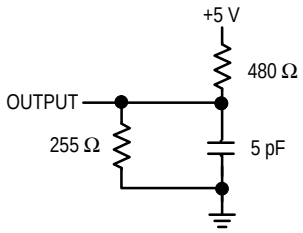
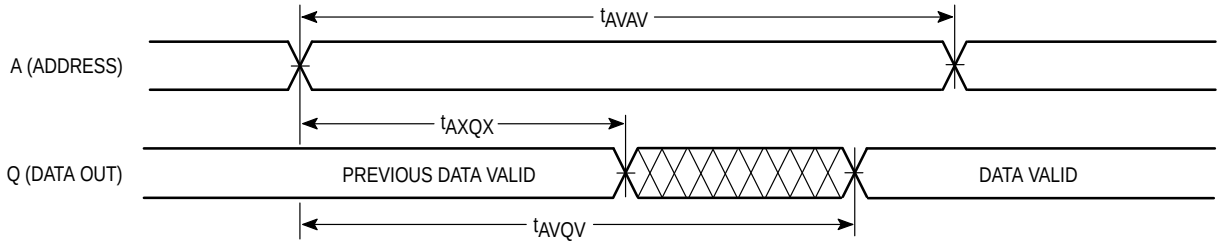


Figure 1B

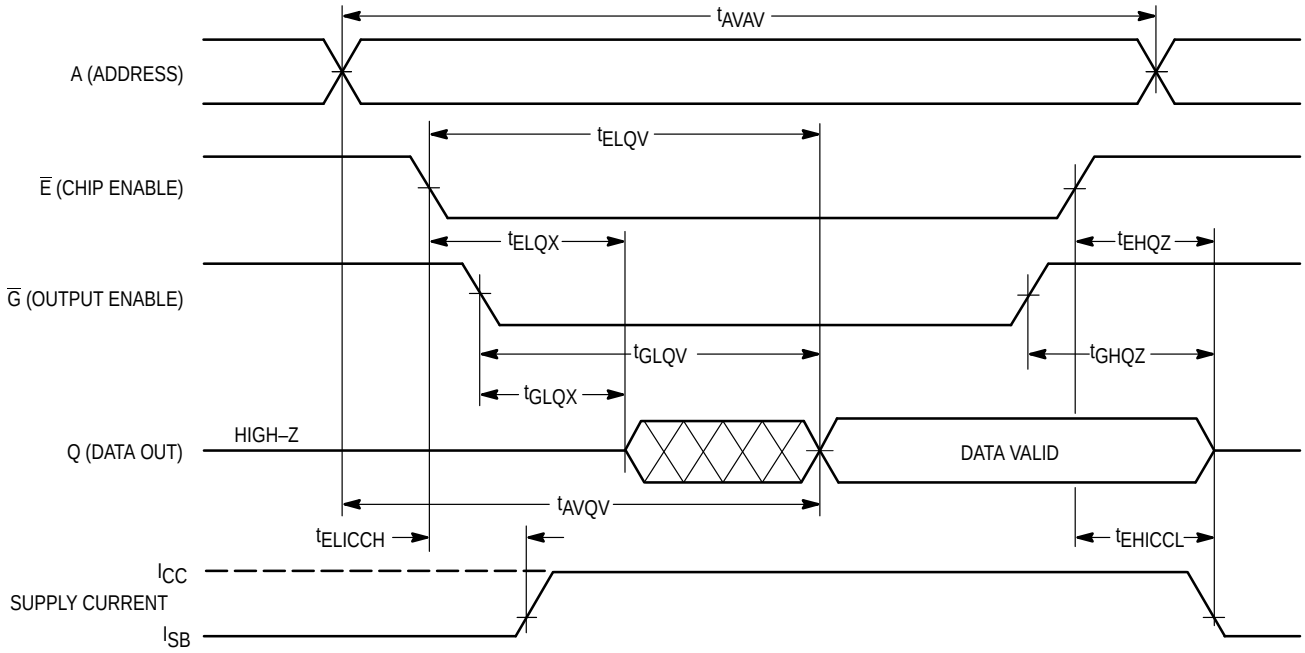
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

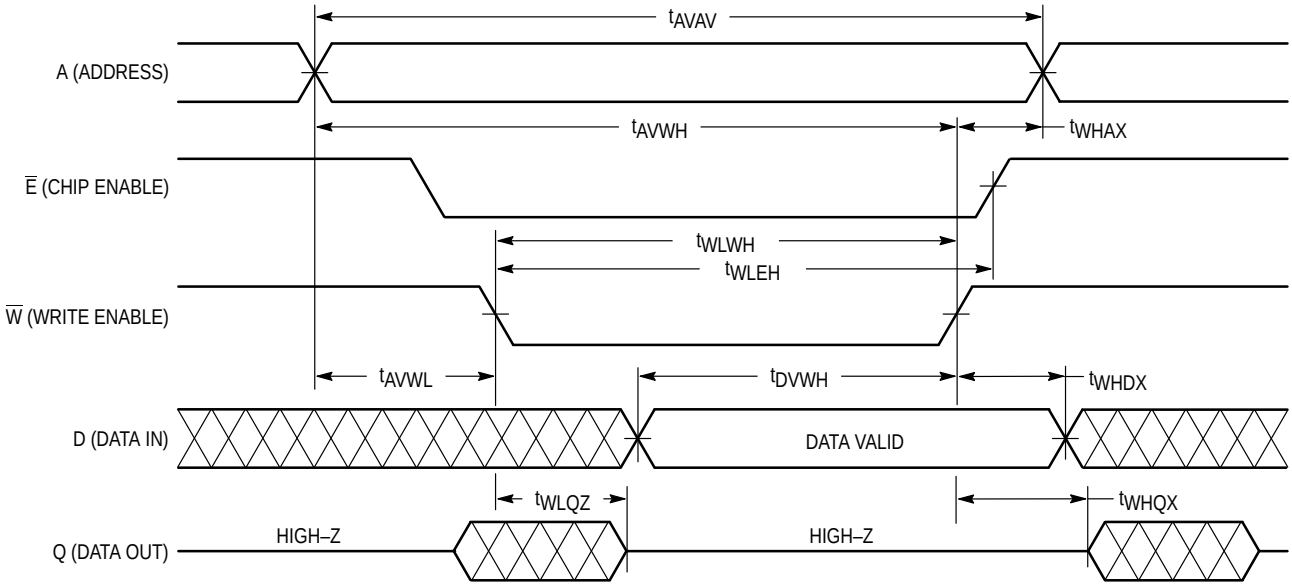


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226A–20		6226A–25		6226A–35		6226A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	5
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	20	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	0	20	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

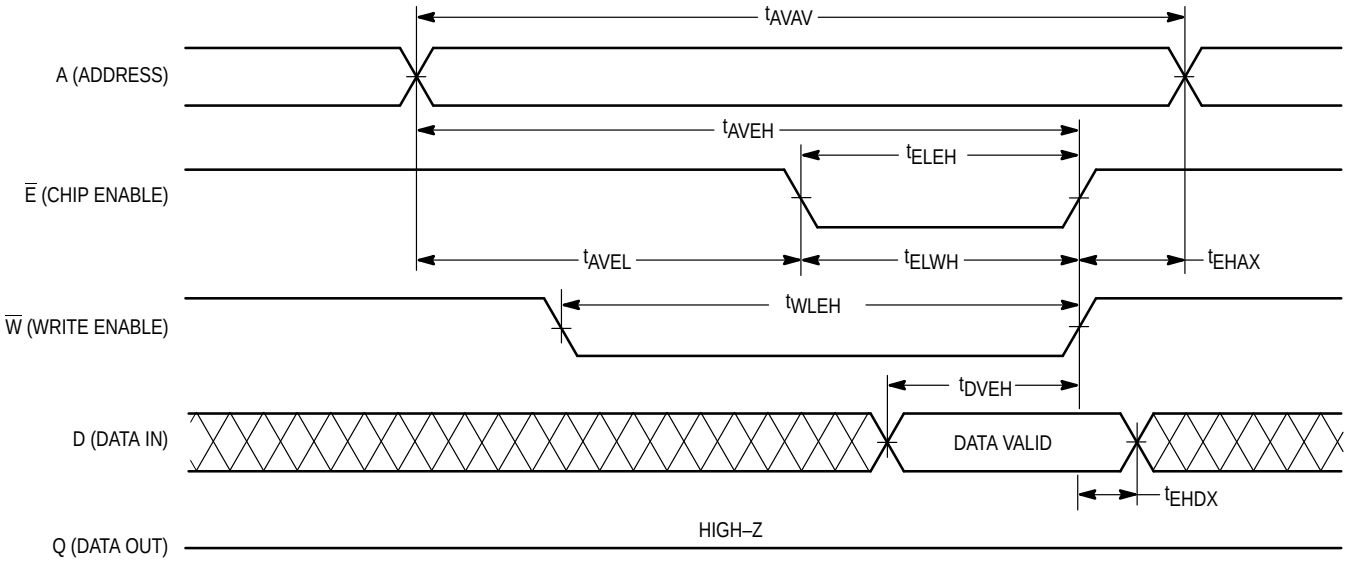


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226A–20		6226A–25		6226A–35		6226A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	5
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	15	—	17	—	20	—	25	—	ns	6, 7
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

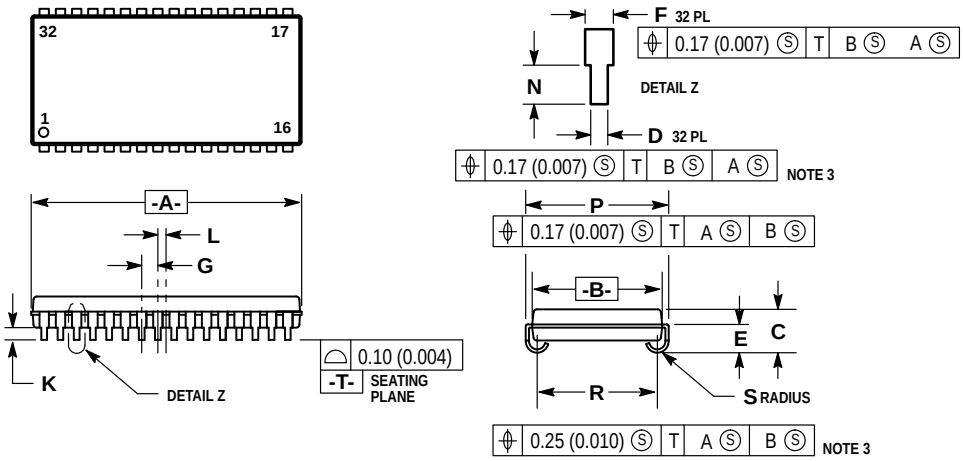
MCM 6226A WJ XX XX

- MCM — Motorola Memory Prefix
- 6226A — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6226AWJ20, MCM6226AWJ20R2, MCM6226AWJ25, MCM6226AWJ25R2, MCM6226AWJ35, MCM6226AWJ35R2, MCM6226AWJ45, MCM6226AWJ45R2

PACKAGE DIMENSIONS

32 LEAD
400 MIL SOJ
CASE 857A–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.83	21.08	0.820	0.830
B	10.03	10.29	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.27	9.52	0.365	0.375
S	0.77	1.01	0.030	0.040

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4–32–1, Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.