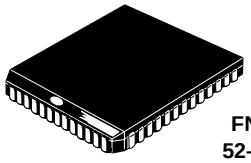
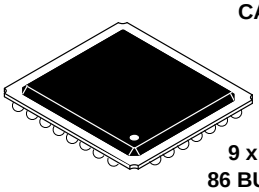
MCM56824A

DSPRAM™
8K x 24 Bit Fast Static RAM



FN PACKAGE
52–LEAD PLCC
CASE 778–02



9 x 10 GRID
86 BUMP PBGA
CASE 896A–01

The MCM56824A is a 196,608 bit static random access memory organized as 8,192 words of 24 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to the Motorola DSP56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic.

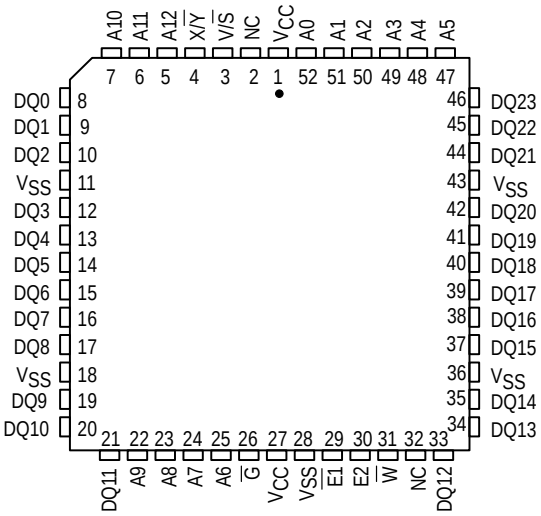
The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, useful in low–power applications. A single on–chip multiplexer selects A12 or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands by dynamically re–partitioning the RAM array. Typical applications will logically map vector operands into upper memory with scalar operands being stored in lower memory. By connecting DSP56001 address A15 to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource irrespective of operand type. See application diagrams at the end of this document for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise.

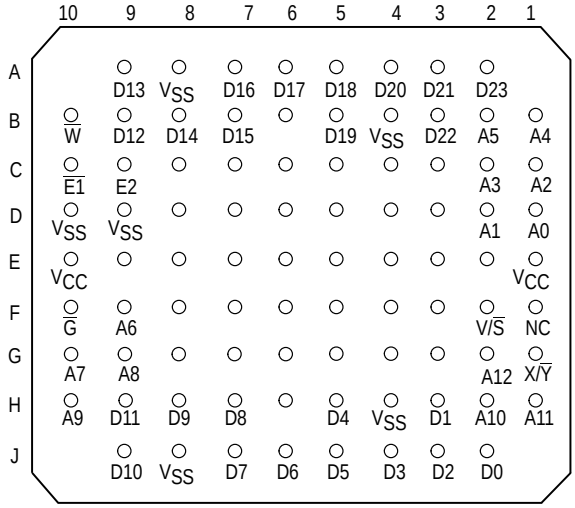
The MCM56824A is available in a 52 pin plastic leaded chip–carrier (PLCC) and a 9 x 10 grid, 86 bump surface mount PBGA.

- Single 5 V ± 10% Power Supply
- Fast Access and Cycle Times: 20/25/35 ns Max
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- Single Bit On–Chip Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three State Outputs
- High Board Density PLCC Package
- Low Power Standby Mode
- Fully TTL Compatible

PIN ASSIGNMENTS
PLCC



VIEW OF PBGA PACKAGE BOTTOM



Not to Scale

PIN NAMES

A0 – A11	Address Inputs
A12, X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexer Control
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ23	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of the device, all V_{SS} pins must be connected to ground.

DSPRAM is a trademark of Motorola, Inc.

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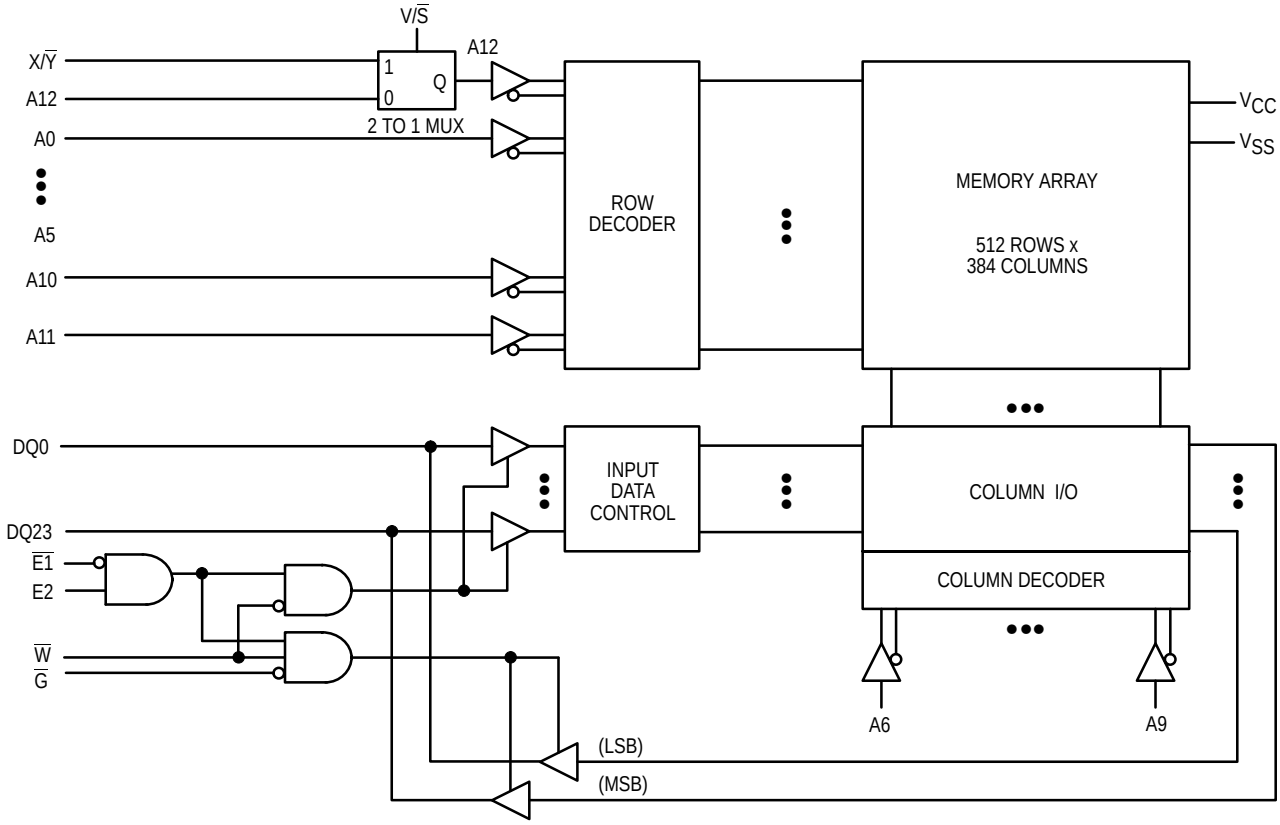
MOTOROLA

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	I_{SB}	High–Z
X	L	X	X	X	Not Selected	I_{SB}	High–Z
L	H	H	H	X	Output Disable	I_{CC}	High–Z
L	H	L	H	H	Read Using X/$\overline{Y}$	I_{CC}	Data Out
L	H	L	H	L	Read Using A12	I_{CC}	Data Out
L	H	X	L	H	Write Using X/$\overline{Y}$	I_{CC}	Data In
L	H	X	L	L	Write Using A12	I_{CC}	Data In

NOTE: X=don't care.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.75	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board with at least 300 LFPM of transverse air flow being maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(i)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0 mA, All Other Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V) MCM56824A–20 Cycle Time: ≥ 20 ns MCM56824A–25 Cycle Time: ≥ 25 ns MCM56824A–35 Cycle Time: ≥ 35 ns	I_{CCA}	 — — —	 260 220 180	mA
Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, All Inputs = V_{IL} or V_{IH})	I_{SB1}	—	15	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0 – DQ23	C_{in}	4	6	pF
Input/Output Capacitance	DQ0 – DQ23	C_{out}	6	8	pF

AC TEST LOADS

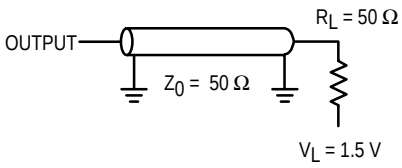


Figure 1A

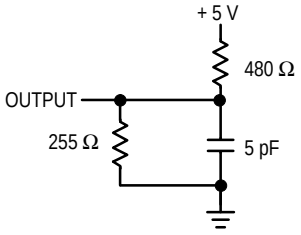


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

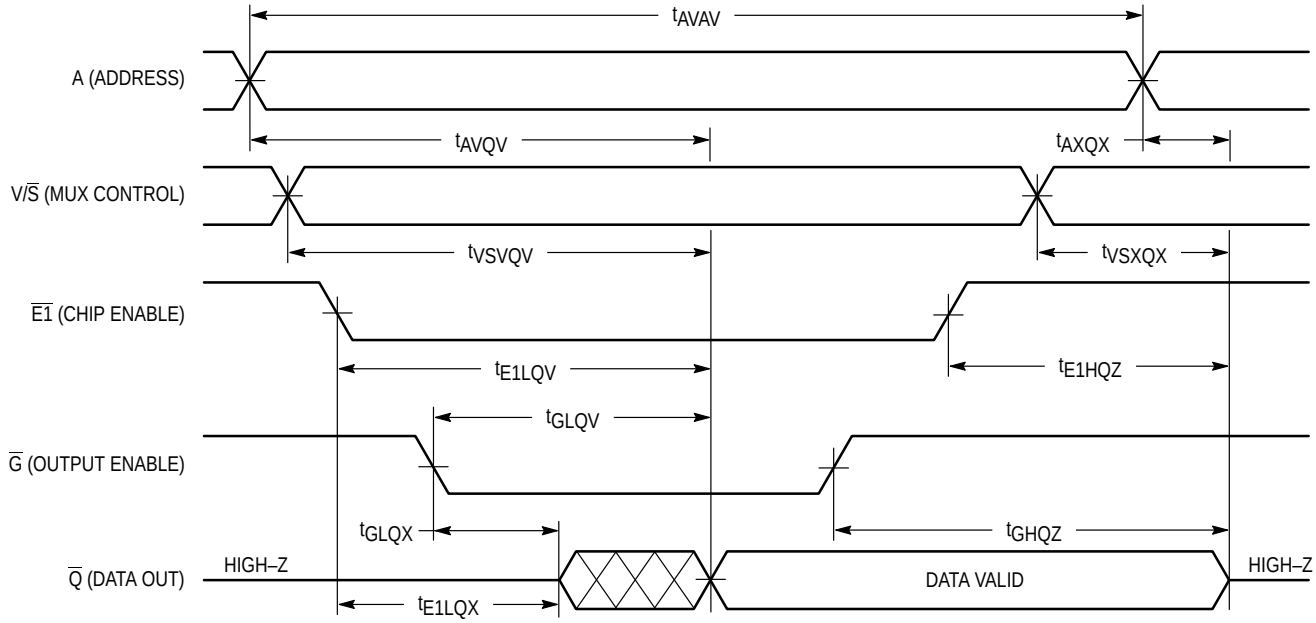
Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Access Time	t_{AVQV}	—	20	—	25	—	35	ns	
MUX Control Valid to Output Valid	t_{VSVQV}	—	20	—	25	—	35	ns	
Chip Enable to Output Valid	t_{E1LQV} t_{E2HQV}	—	20	—	25	—	35	ns	4
Output Enable to Output Valid	t_{GLQV}	—	8	—	10	—	15	ns	
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	2	—	2	—	0	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	0	—	0	—	0	—	ns	5
Output Hold from Address Change	t_{AXQX}	4	—	5	—	5	—	ns	
Output Hold from MUX Control Change	t_{VSXQX}	4	—	5	—	5	—	ns	
Chip Enable to Output High–Z	t_{E1HQZ} t_{E2LQZ}	0	10	0	15	0	15	ns	4, 5
Output Enable High to Output High–Z	t_{GHQZ}	0	8	0	15	0	15	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address or vector/scalar transition to the first address or vector/scalar transition.
3. Addresses valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

READ CYCLE

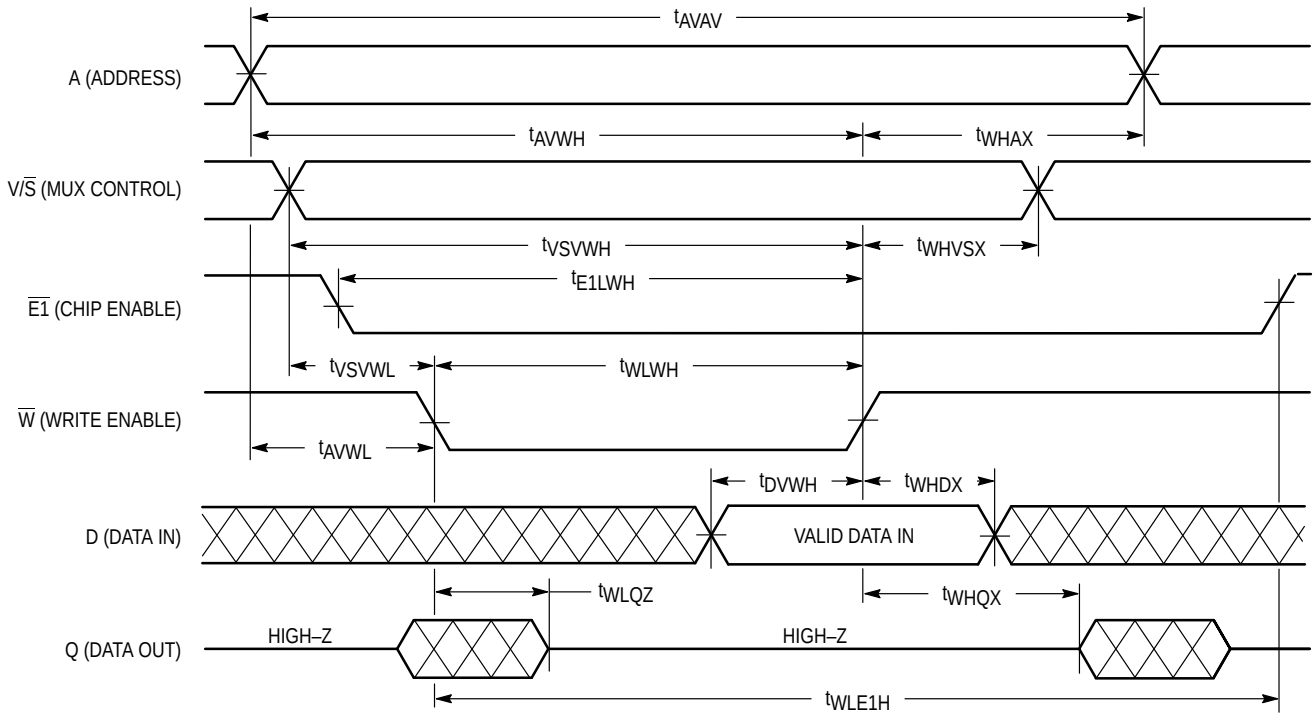


WRITE CYCLE TIMING (Write Enable Initiated, See Note 1)

Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	20	—	30	—	ns	
MUX Control Valid to End of Write	t_{VSVWH}	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	15	—	15	—	20	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	15	—	15	—	20	—	ns	3, 4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	15	—	15	—	20	—	ns	3, 4
Data Valid to End of Write	t_{DVWH}	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	5
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{WHVSX}	0	—	0	—	0	—	ns	
Write High to Output Low–Z	t_{WHQX}	4	—	5	—	5	—	ns	6
Write Low to Output High–Z	t_{WLQZ}	0	15	0	15	0	15	ns	6

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. Write must be high for all address transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high–impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

$\overline{WE}$ INITATED WRITE CYCLE

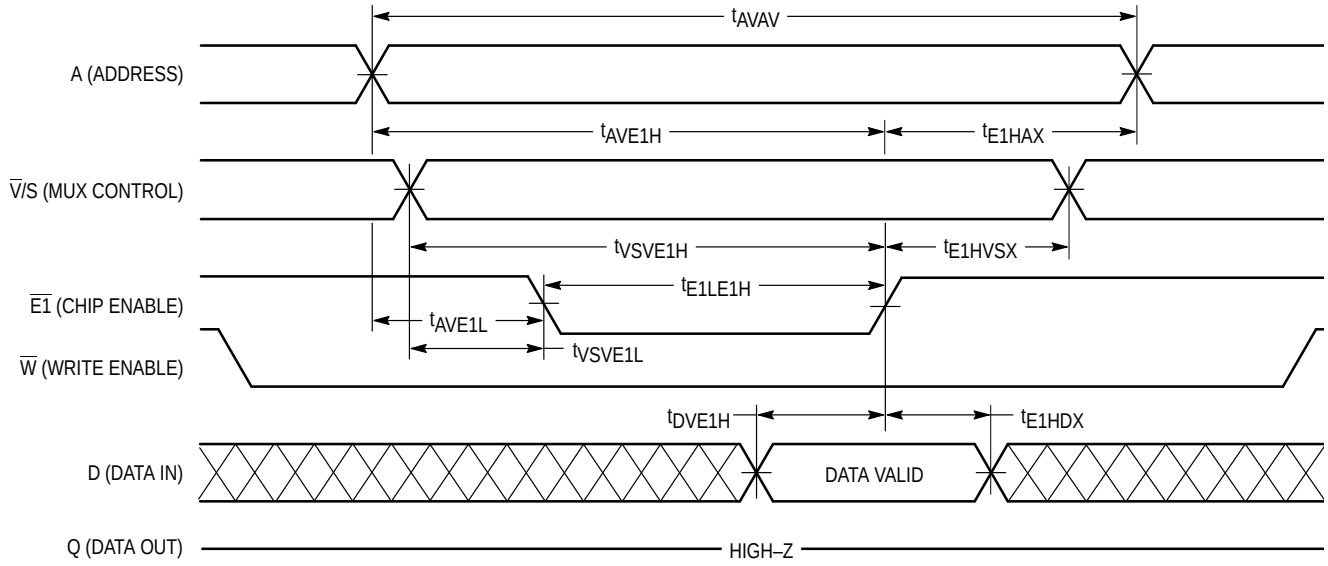


WRITE CYCLE TIMING (Chip Enable Initiated, See Note 1)

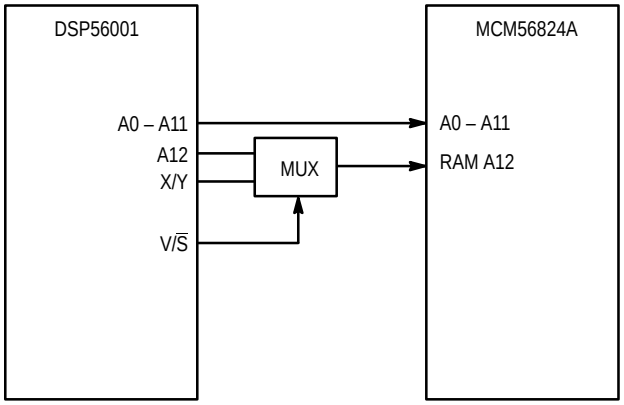
Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVE1L} t_{AVE2H}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVE1L} t_{VSVE2H}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	15	—	20	—	30	—	ns	2
MUX Control Valid to End of Write	t_{VSVE1H} t_{VSVE2L}	15	—	20	—	30	—	ns	2
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	12	—	15	—	20	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	8	—	10	—	15	—	ns	2
Data Hold Time	t_{E1HDX} t_{E2LDX}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{E1HVSX} t_{E2LVSX}	0	—	0	—	0	—	ns	2

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high–impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.

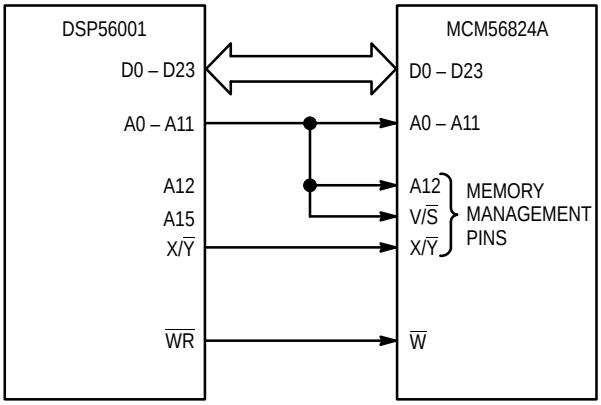
$\overline{E1}$ OR E2 INITIATED WRITE CYCLE

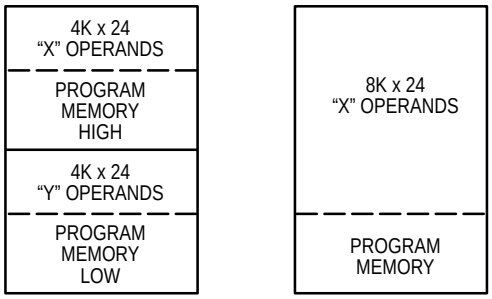


DSPRAM Multiplexed Vector/Scalar Address Maps

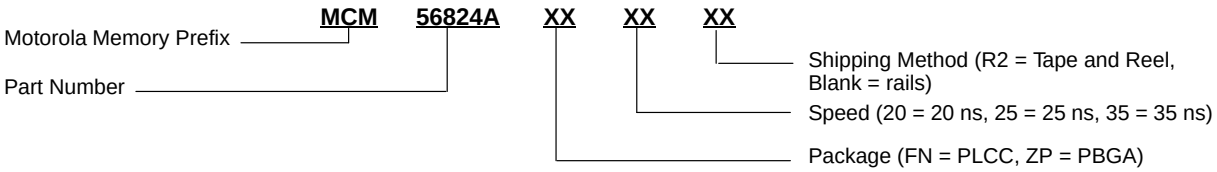


8K x 24 DSPRAM Used in Typical Application





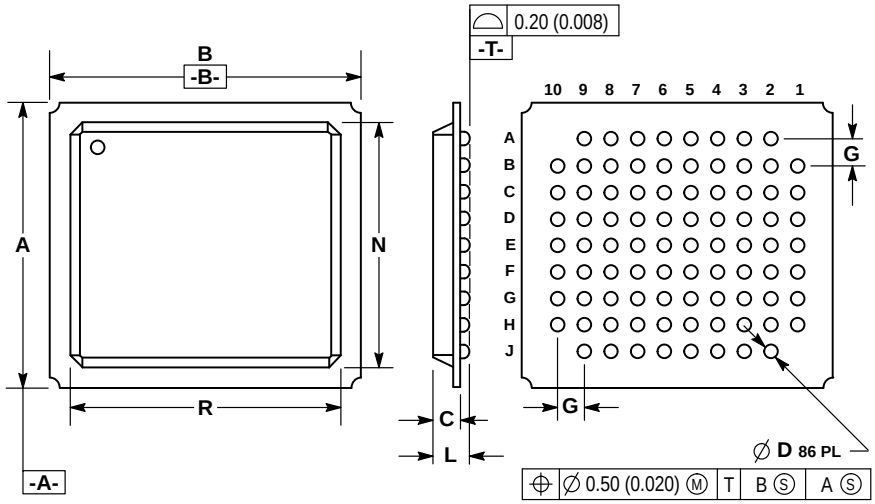
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM56824AFN20 MCM56824AFN25 MCM56824AFN35
MCM56824AZP20 MCM56824AZP25 MCM56824AZP35
MCM56824AZP20R2 MCM56824AZP25R2 MCM56824AZP35R2

PACKAGE DIMENSIONS

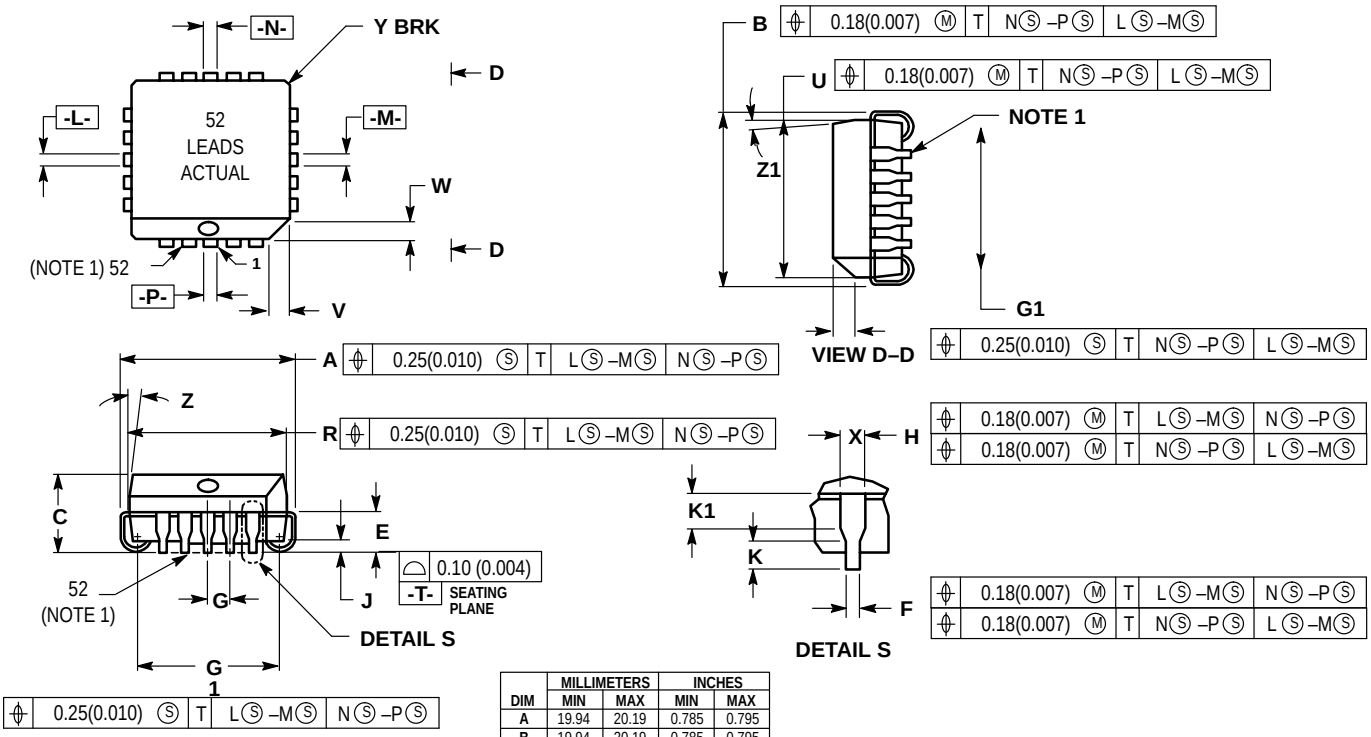
ZP PACKAGE
9 x 10 PBGA
CASE 896A–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.16	16.36	0.637	0.644
B	17.68	17.88	0.697	0.703
C	1.33	1.73	0.053	0.068
D	0.69	0.81	0.028	0.031
G	1.524 BSC		0.060 BSC	
L	1.84	2.44	0.073	0.096
N	13.80	14.20	0.544	0.559
R	15.29	15.69	0.602	0.617

FN PACKAGE
52–LEAD PLCC
CASE 778–02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	18.04	18.54	0.710	0.730
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

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USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
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