MCM32A32
MCM32A64

128KB and 256KB Secondary Cache Fast Static RAM Modules

With Tag for 486 Processor Based Systems

The MCM32A32 and MCM32A64 are two products in Motorola's asynchronous secondary cache module family for the 486 processor. The modules are configured with 32–bit data, 8–bit tag, and an altered bit for writeback caches. The family supports all cache sizes of the 486 processor. They are offered in 33 and 50 MHz versions.

The 32A32 is a 128KB single bank cache of 32K x 32. The tag is 8K x 8, and the altered bit is 8K x 1.

The 32A64 is a 256KB double bank cache of 64K x 32. The tag is 16K x 8 and the altered bit is 16K x 1. The cache family is designed to interface with popular 486 chipsets with on–board cache controllers.

Cache upgrades are seamless, eliminating the need for motherboard jumpers.

PD0, 1, 2 are reserved for density identification:

MCM32A32: PD0 = gnd, PD1 = gnd, PD2 = open
MCM32A64: PD0 = open, PD1 = open, PD2 = gnd

- 64 Position Dual Readout SIMM for Circuit Density
- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times/Cycle Times: 15 ns/50 MHz, 20 ns/33 MHz
- Cache Byte Write, Byte Chip Enable, Bank Output Enable
- Tag Write Enable, Altered Write Enable, Tag/Altered Chip Enable
- Decoupling Capacitors Are Used For Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes

REV 1
5/95

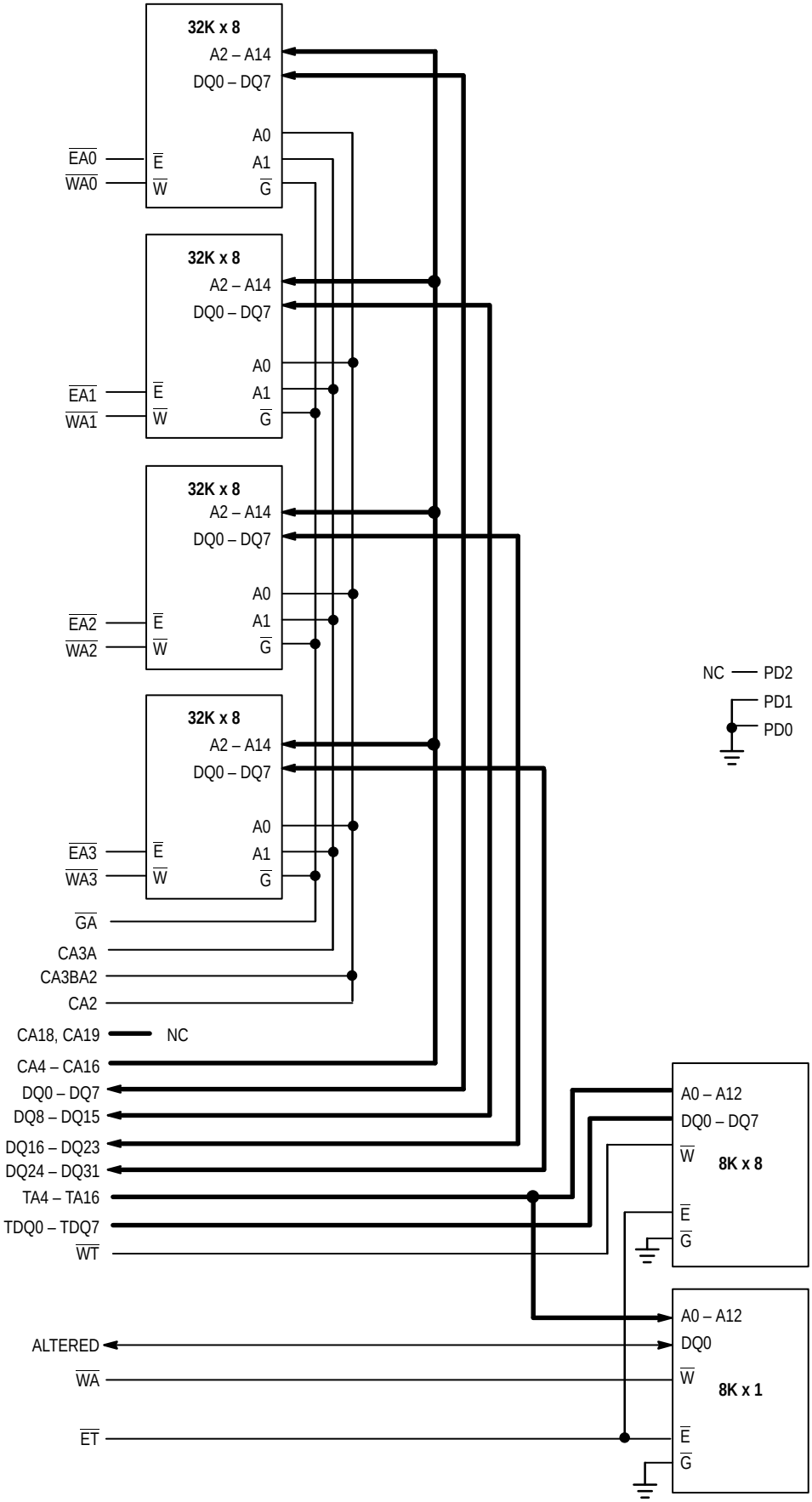
PIN ASSIGNMENT
64 POSITION DUAL READOUT
128 PIN SIMM
TOP VIEW

PD0	1	65	PD1
PD2	2	66	V_{SS}
DQ0	3	67	DQ1
DQ2	4	68	DQ3
DQ4	5	69	V_{CC}
DQ6	6	70	DQ5
DQ8	7	71	DQ7
V_{SS}	8	72	DQ9
DQ10	9	73	DQ11
DQ12	10	74	DQ13
DQ14	11	75	DQ15
DQ16	12	76	DQ17
DQ18	13	77	DQ19
DQ20	14	78	DQ21
V_{SS}	15	79	V_{SS}
DQ22	16	80	DQ23
DQ24	17	81	DQ25
V_{CC}	18	82	V_{CC}
DQ26	19	83	DQ27
DQ28	20	84	DQ29
DQ30	21	85	DQ31
NC	22	86	NC
NC	23	87	NC
V_{SS}	24	88	V_{SS}
$\overline{EA0}$	25	89	$\overline{EB0}$
$\overline{EA1}$	26	90	$\overline{EB1}$
$\overline{EA2}$	27	91	V_{CC}
$\overline{EA3}$	28	92	$\overline{EB2}$
V_{SS}	29	93	$\overline{EB3}$
$\overline{GA}$	30	94	$\overline{GB}$
$\overline{WA0}$	31	95	$\overline{WB0}$
WA1	32	96	WB1
$\overline{WA2}$	33	97	$\overline{WB2}$
$\overline{WA3}$	34	98	$\overline{WB3}$
$\overline{WT}$	35	99	WA
$\overline{ET}$	36	100	V_{CC}
NC	37	101	NC
NC	38	102	NC
CA3A	39	103	CA3BA2
CA2	40	104	CA3B
V_{SS}	41	105	V_{SS}
CA4	42	106	CA5
CA6	43	107	CA7
CA8	44	108	CA9
CA10	45	109	CA11
CA12	46	110	CA13
CA14	47	111	CA15
CA16	48	112	CA17
CA18	49	113	CA19
V_{SS}	50	114	V_{SS}
TA4	51	115	TA5
TA6	52	116	TA7
TA8	53	117	TA9
TA10	54	118	TA11
TA12	55	119	TA13
TA14	56	120	TA15
TA16	57	121	TA17
TA18	58	122	TA19
V_{SS}	59	123	V_{SS}
TDQ0	60	124	TDQ1
TDQ2	61	125	TDQ3
TDQ4	62	126	TDQ5
TDQ6	63	127	TDQ7
ALT	64	128	V_{CC}

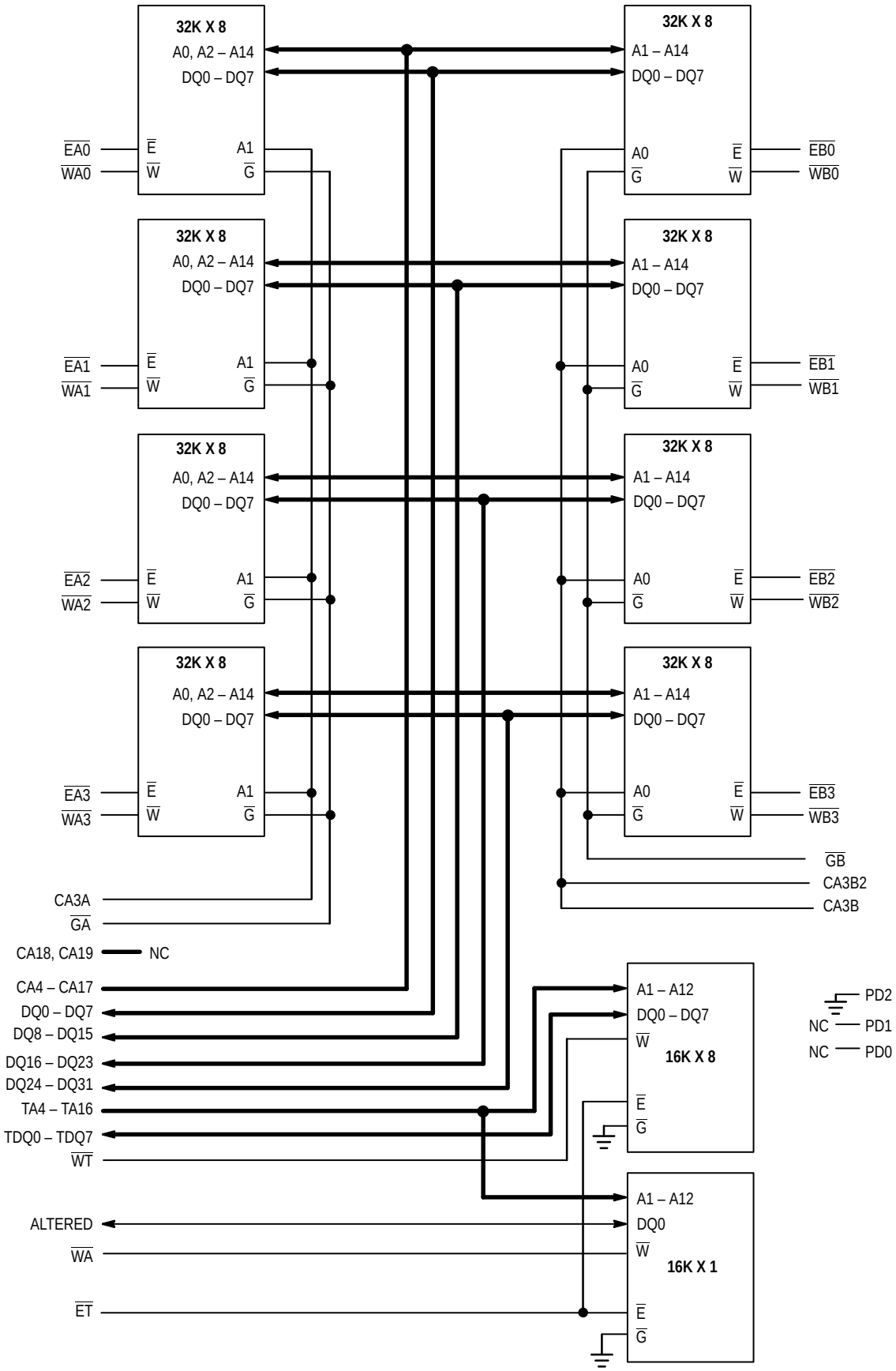
PIN NAMES

CA2 – CA19	Cache Address Inputs
$\overline{WA0}$ – $\overline{WA3}$; $\overline{WB0}$ – $\overline{WB3}$	Byte Write Enable
$\overline{EA0}$ – $\overline{EA3}$; $\overline{EB0}$ – $\overline{EB3}$	Cache Chip Enable
$\overline{GA}$, $\overline{GB}$	Bank Output Enable
DQ0 – DQ31	Cache Data Input/Output
TA4 – TA19	Tag Address Inputs
$\overline{WT}$	Tag Write Enable
$\overline{WA}$	Altered Write Enable
$\overline{ET}$	Tag/Altered Chip Enable
TDQ0 – TDQ7	Tag Data Input/Output
ALT	Altered Input/Output
PD0 – PD2	Presence Detect
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

128KB BLOCK DIAGRAM



256KB BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

NOTE: $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	11.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 10	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 10	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	32A32 33 MHz	32A32 50 MHz	32A64 33 MHz	32A64 50 MHz	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	840	920	1530	1680	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	250	280	465	520	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	110	110	190	190	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Cache Address Input Capacitance	C_{in}	48	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF
Tag Address Input Capacitance	C_{in}	18	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	33 MHz		50 MHz		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	20	ns	
Tag Access Time	t_{AVTV}	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	ns	4
Output Enable Access Time	t_{GLQV}	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	ns	5,6,7
Enable Low to Output Active	t_{ELQX}	4	—	4	—	ns	5,6,7
Enable High to Output High–Z	t_{EHQZ}	0	8	0	9	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	5,6,7
Output Enable High to Output High–Z	t_{GHQZ}	0	7	0	8	ns	5,6,7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E}$ = $\overline{E}$xx, $\overline{ET}$; $\overline{W}$ = $\overline{W}$xx, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

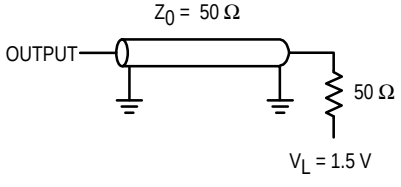


Figure 1A

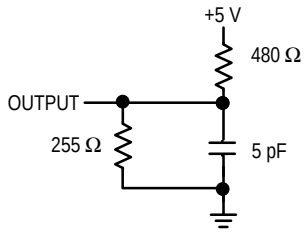
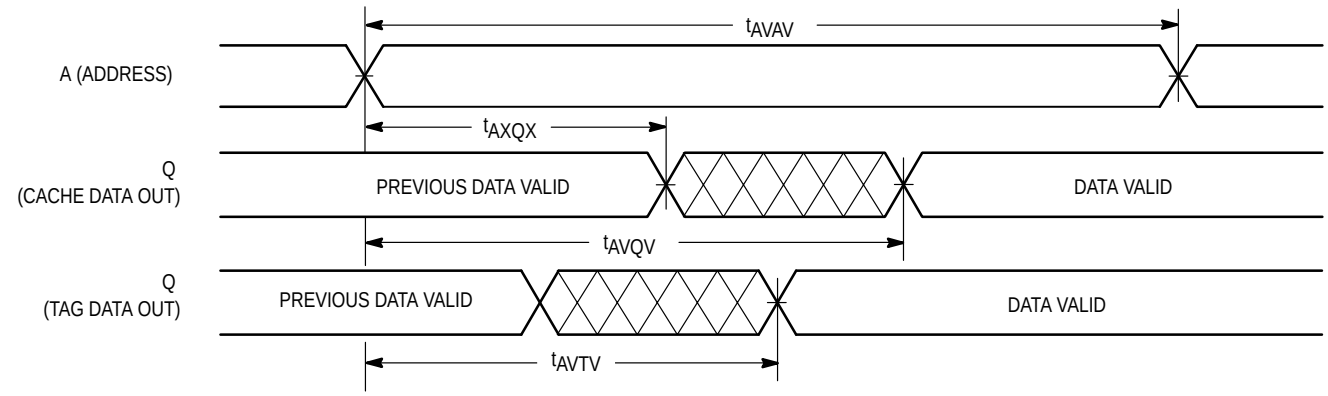


Figure 1B

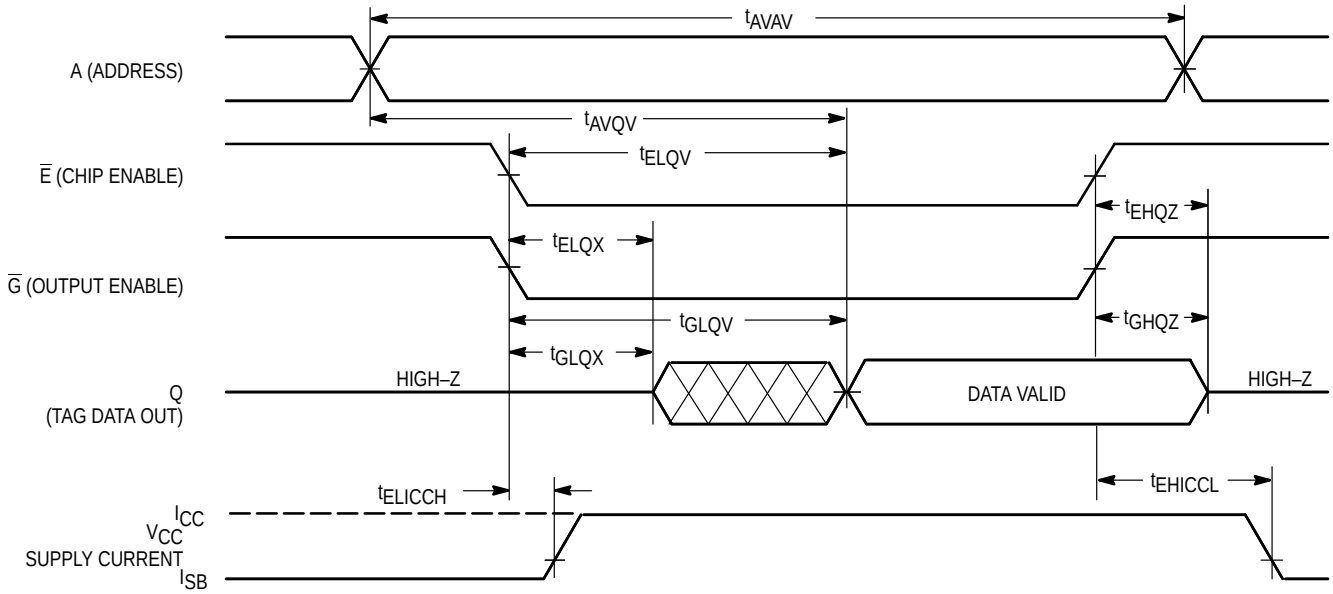
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)

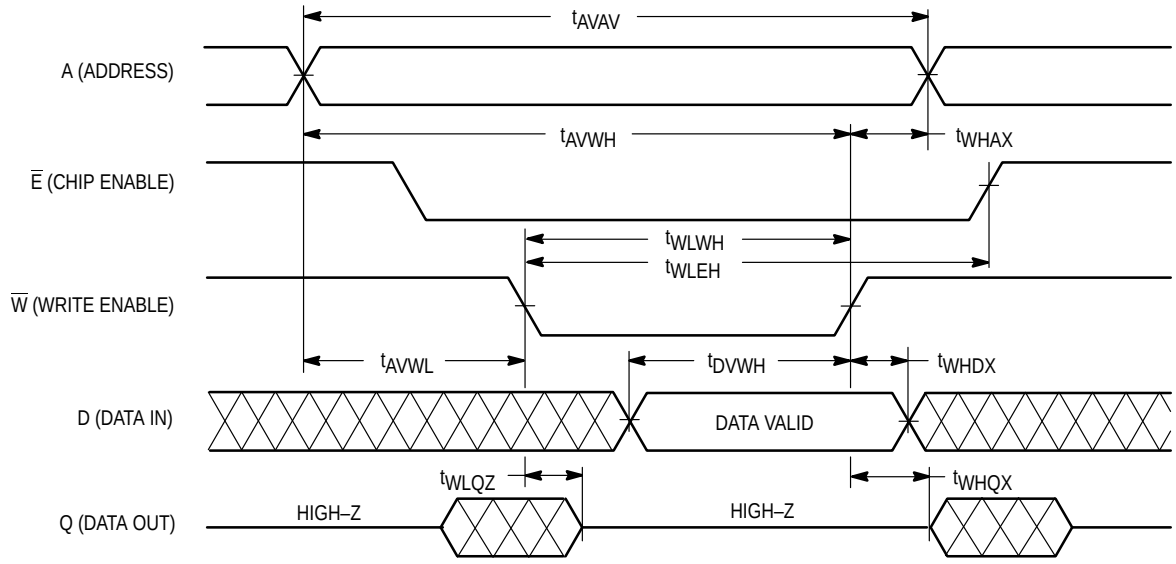


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	50 MHz		33 MHz		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	15	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	0	8	ns	6,7,8
Write High to Output Active	t_{WHQX}	0	—	0	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

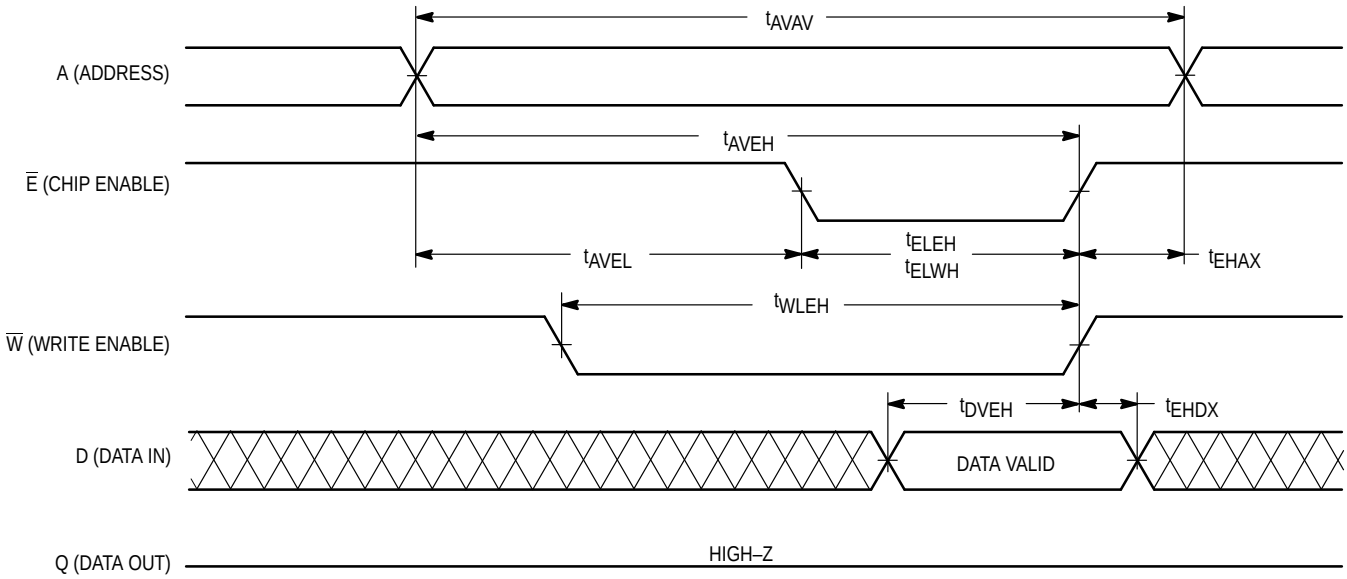


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

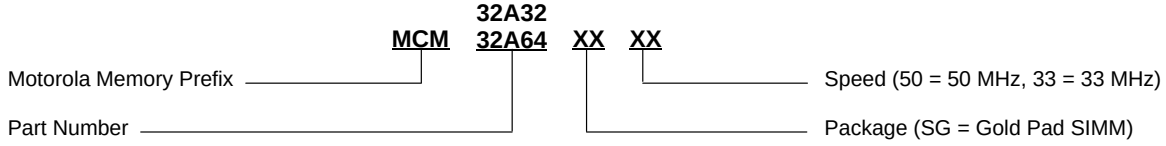
Parameter	Symbol	50 MHz		33 MHz		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	ns	
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	12	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32A32SG50 MCM32A32SG33
MCM32A64SG50 MCM32A64SG33

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