MCM32128A

128K x 32 Bit
Fast Static RAM Module

The MCM32128A is a 4M bit static random access memory module organized as 131,072 words of 32 bits. The module is offered in a 64–lead single in–line memory module (SIMM). Four MCM6226 fast static RAMs, packaged in 32–lead SOJ packages are mounted on a printed circuit board along with four decoupling capacitors.

The MCM6226 is a high–performance CMOS fast static RAM organized as 131,072 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM32128A is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 520/480/460 mA Maximum, Active AC
- High Board Density ZIP or SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte
- High Quality Four–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

**PIN ASSIGNMENT
TOP VIEW
64-LEAD SIMM – CASE TBD**

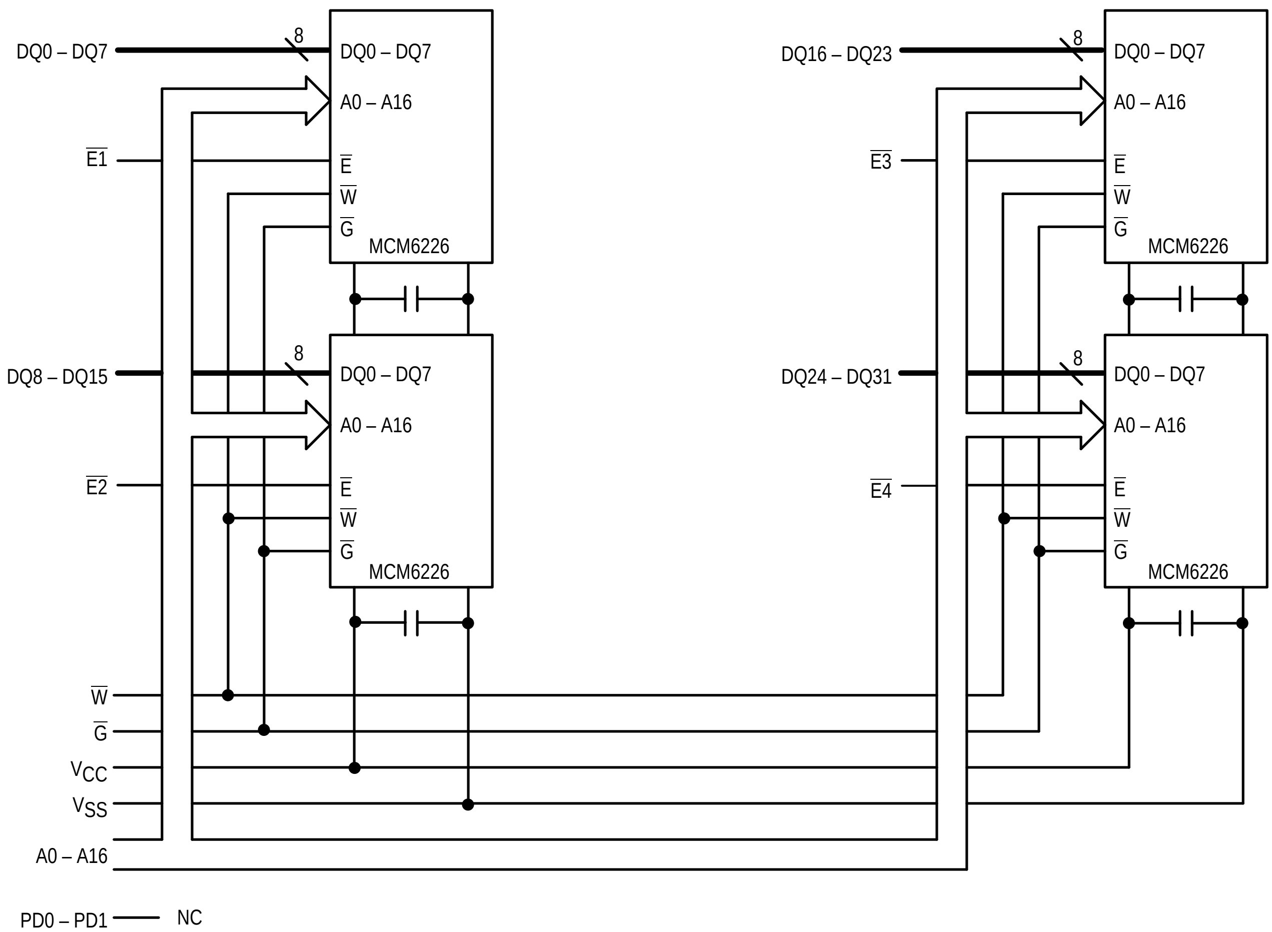
PD0	2	1	V_{SS}
DQ0	4	3	PD1
DQ1	6	5	DQ8
DQ2	8	7	DQ9
DQ3	10	9	DQ10
V_{CC}	12	11	DQ11
A1	14	13	A0
A3	16	15	A2
A5	18	17	A4
DQ4	20	19	DQ12
DQ5	22	21	DQ13
DQ6	24	23	DQ14
DQ7	26	25	DQ15
$\overline{W}$	28	27	V_{SS}
A7	30	29	A6
$\overline{E1}$	32	31	$\overline{E2}$
$\overline{E3}$	34	33	$\overline{E4}$
A8	36	35	NC
V_{SS}	38	37	$\overline{G}$
DQ16	40	39	DQ24
DQ17	42	41	DQ25
DQ18	44	43	DQ26
DQ19	46	45	DQ27
A10	48	47	A9
A12	50	49	A11
A14	52	51	A13
A15	54	53	V_{CC}
DQ20	56	55	A16
DQ21	58	57	DQ28
DQ22	60	59	DQ29
DQ23	62	61	DQ30
V_{SS}	64	63	DQ31

PIN NAMES	
A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD1	Package Density

For proper operation of the device, V_{SS} must be connected to ground.

FUNCTIONAL BLOCK DIAGRAM

128K x 32 MEMORY MODULE



TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	4.4	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 4	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 4	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min)	MCM32128A–15: t_{AVAV} = 15 ns MCM32128A–20: t_{AVAV} = 20 ns MCM32128A–25: t_{AVAV} = 25 ns	I_{CCA}	— — —	520 480 460	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)		I_{SB1}	—	160	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31 and $\overline{E1}$ – $\overline{E4}$) ($\overline{E1}$ – $\overline{E4}$)	C_{in} C_{in}	24 14	pF pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . 1.5 V
Output Timing Reference Level . . . . 1.5 V
Input Pulse Levels . . . . 0 to 3.0 V

Output Load . . . . See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time . . . . 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM32128A–15		MCM32128A–20		MCM32128A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	8	—	9	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	8	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

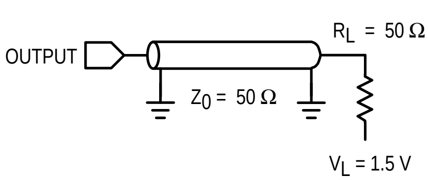


Figure 1A

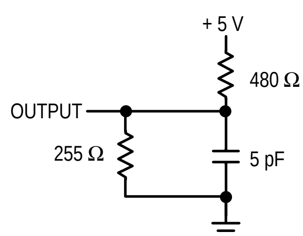
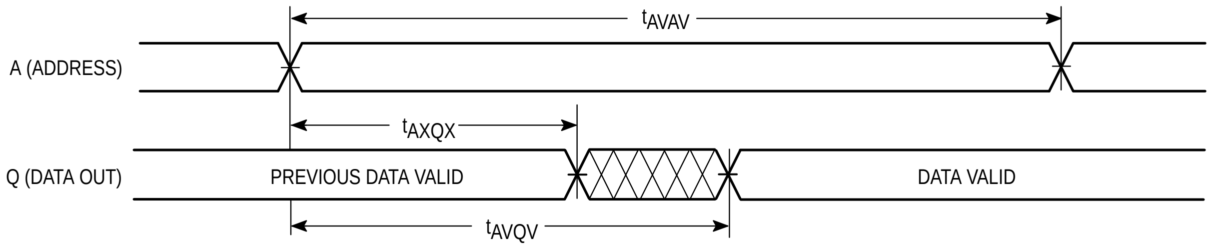


Figure 1B

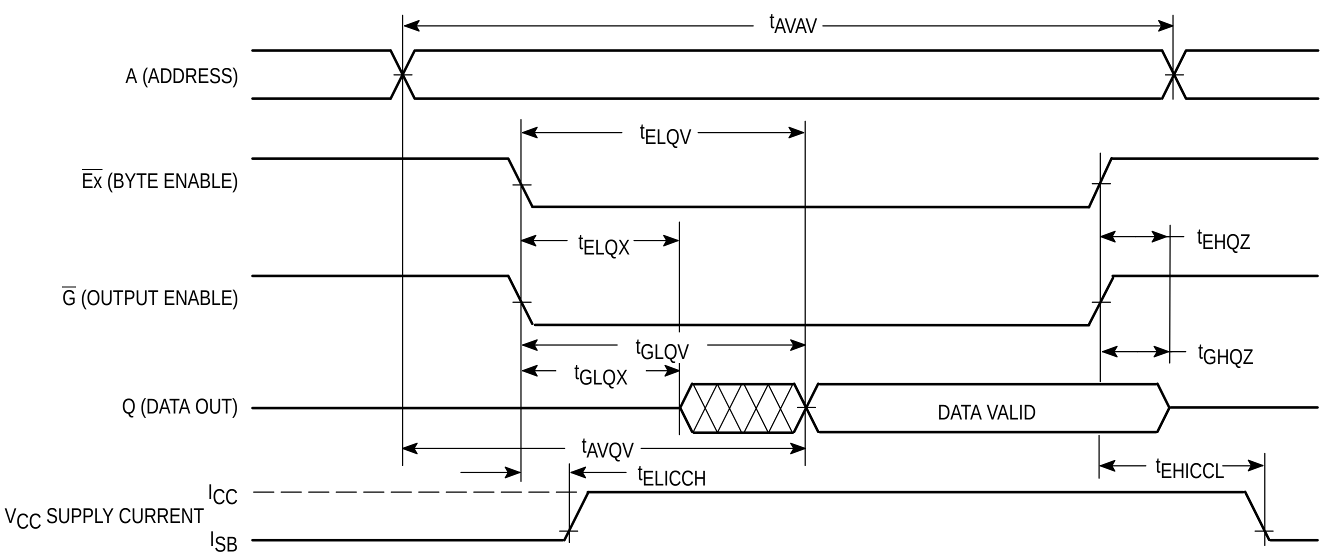
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



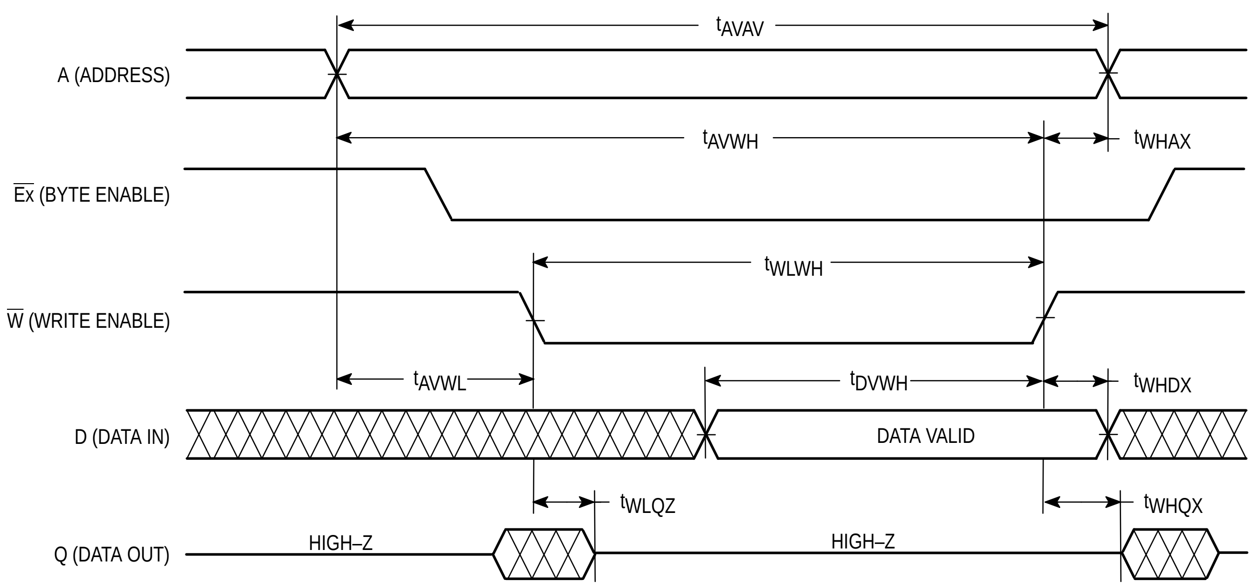
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32128A–15		MCM32128A–20		MCM32128A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	8	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

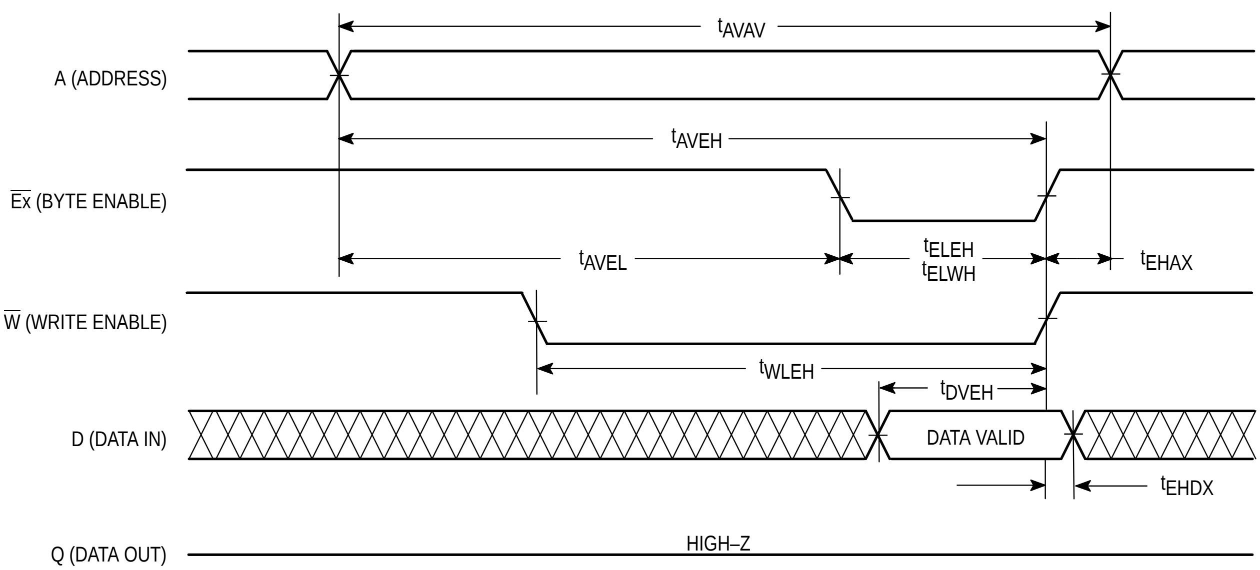


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32128A–15		MCM32128A–20		MCM32128A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	10	—	12	—	15	—	ns	4,5
Enable to End of Write	t_{ELWH}	10	—	12	—	15	—	ns	
Write Pulse Width	t_{WLEH}	10	—	12	—	15	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 32128A XX XX

Motorola Memory Prefix — MCM

Part Number — 32128A

Package (Z = ZIP Module, SG = Gold Pad SIMM)

Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns)

Full Part Numbers — MCM32128AZ15 MCM32128AZ20 MCM32128AZ25
MCM32128ASG15 MCM32128ASG20 MCM32128ASG25

Literature Distribution Centers:
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