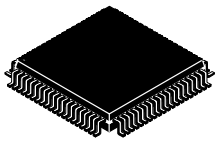
MCD221

Technical Summary

CD–Interface and Audio Processor (CIAP)



FU SUFFIX
QFP PACKAGE
CASE 841B–01

ORDERING INFORMATION

MCD221FU	QFP

This technical summary provides a brief description of the MCD221 CD–Interface and Audio Processor. A complete data sheet for the MCD221 is available and can be ordered from your local Motorola sales office. The order number is MCD221/D.

The MCD221 has two main functions. The first is to form an interface between a CD drive unit and a CD–i or Photo–CD player. The connection to the drive is designed for both applications and can be either a Digital Out (EBU standard) interface, or an I^2S plus subcode interface. The host interface can be either a 68000 interface for CD–i players, or a serial (SPI) interface for Photo–CD.

The second function of the MCD221 is to decode ADPCM (CD–i base case) audio, to perform audio mixing functions as specified in the Green Book, and to be able to add external audio to the base case audio. The MCD221 can also be used for handling the ADPCM decoding for Photo–CD.

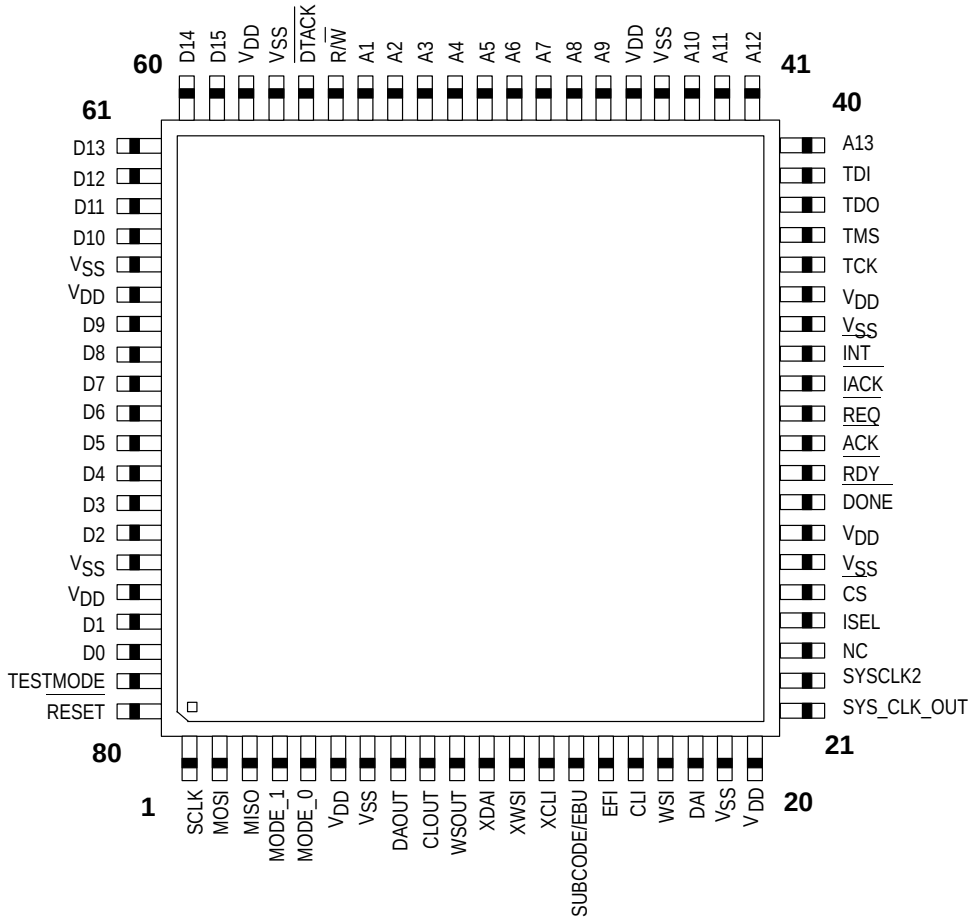
The main features of the MCD221 are as follows:

- Accepts Audio Inputs in I^2S Format (MPEG1) for Mixing with CIAP Internal Audio
- Output Can Be Either I^2S or SONY Format
- Data Input Rate Can Be Up to 2 Times Normal Speed
- Can Connect to a Host via Either a 68K or Serial Interface
- 80–Pin Quad Flat Pack (QFP)

NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

PIN ASSIGNMENT



SIGNAL DESCRIPTIONS

Host Interface

Mnemonic	Type	Name and Function
A[13 … 1]	O	System Address Bus. The address must be stable before $\overline{CS}$ is asserted. Active HIGH.
D[15 … 0]	B	System Data Bus. The data lines must be stable when $\overline{CS}$ is active during a write and before DTACK is asserted during a read. Tri–state.
$\overline{CS}$	I	Chip Select. Used to access the CIAP internal registers and buffers. Active LOW.
R/$\overline{W}$	I	Read/$\overline{Write}$. Indicates the direction of the data transfer. When LOW, the transfer is to the CIAP.
$\overline{DTACK}$	B	Data Transfer Acknowledge. Active LOW. During normal host access, DTACK is an output indicating that data has been put on (read cycles) or read from (write cycles) the data bus. (Active pullup.) During DMA, DTACK is an input indicating that the memory has put data on the data bus.
$\overline{INT}$	O	Interrupt. Released when the interrupt status register is read. Active LOW.
$\overline{IACK}$	I	Interrupt Acknowledge. Active LOW.
$\overline{REQ}$	O	DMA Request. Active LOW.
$\overline{ACK}$	I	Acknowledge. DMA handshake signal indicating that the bus is available for data transfer. Active LOW.
$\overline{RDY}$	O	Ready. DMA handshake signal indicating that the CIAP has completed the data transfer. Tri–state. Active LOW. When released by the CIAP, the output is forced high for a few nanoseconds before it is made tri–state.
$\overline{DONE}$	I	Done. Indicates the last transfer of a DMA burst. Active LOW.

Serial Interface

Mnemonic	Type	Name and Function
SCLK	I	Serial Clock.
MOSI	I	Serial Data. Master out, slave in.
MISO	O	Serial Data. Master in, slave out.
MODE_0, MODE_1	I	Serial Interface MODE bits. 00 = Write selected register 01 = Read selected register 10 = Write address 11 = No action

Data Input

Mnemonic	Type	Name and Function
CLI	I	Serial Bit Clock Input.
WSI	I	Word Clock Input.
DAI	I	Serial Data Input.
EFI	I	Error Flag Input.
SUBCODE/EBU	I	Subcode (P … W) serial data input or EBU input for both main channel and subchannel.

External Audio Interface

Mnemonic	Type	Name and Function
XCLI	I	External Audio Serial Bit Clock Input. When not used, the pin must be connected to V_{CC} or V_{SS}.
XWSI	I	External Audio Word Clock Input. When not used, the pin must be connected to V_{CC} or V_{SS}.
XDAI	I	External Audio Data Input. When not used, the pin must be connected to V_{CC} or V_{SS}.

Audio Output Interface

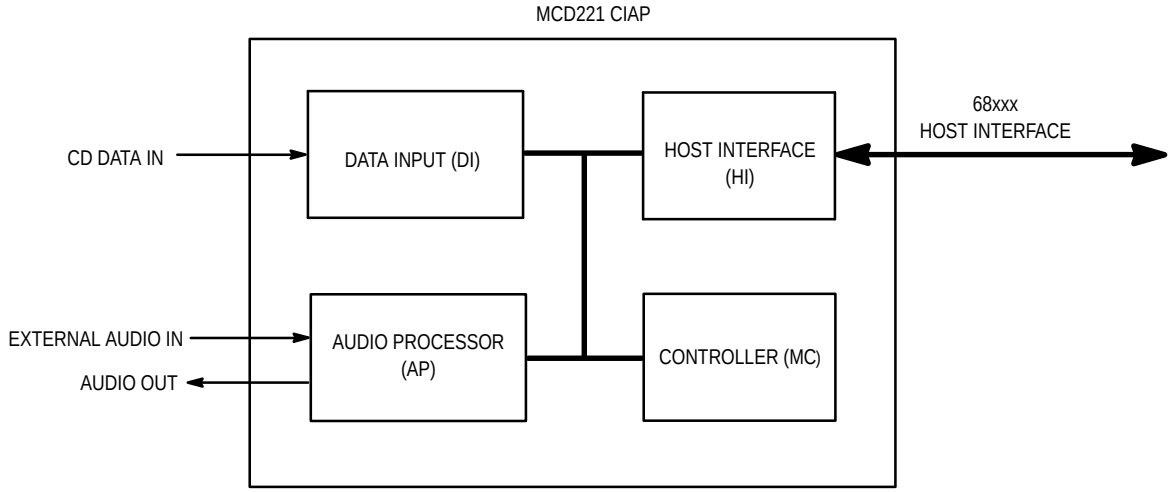
Mnemonic	Type	Name and Function
CLOUT	O	Audio Output Serial Clock.
WSOUT	O	Audio Output Word Clock.
DAOUT	O	Audio Output Serial Data.

General

Mnemonic	Type	Name and Function
SYS_CLK_OUT	O	16.9344 MHz System Clock Output.
SYSCLK2	I	Double System Clock Frequency Input. Input for an oscillator with a frequency of 33.8688 MHz.
$\overline{\text{RESET}}$	I	Reset. Global reset for the CIAP. Active LOW.
ISEL	I	Interface Select. 0 = Serial interface (no parallel access possible) 1 = 68000 interface (no serial access possible)
TDI	I	Test Data Input. (Boundary scan input pin.)
TDO	O	Test Data Output. (Boundary scan output pin.)
TCK	I	Test Clock. (Boundary scan input pin.)
TMS	I	Test Mode Select. (Boundary scan input pin.)
TESTMODE	O	When 0, the CIAP is operational. When 1, the CIAP is in test mode.

FUNCTIONAL DESCRIPTION

DATA FLOW DIAGRAM



The MCD221 Data Flow Diagram should be used in conjunction with the following notes which outline the function of the various blocks within the device:

- The **data input module** consists of two parts; a main channel decoder and a subchannel decoder. Both decoders can be active at the same time. The main channel decoder can be in different modes; CD–DA mode, CD–ROM mode, or CD–i mode.
- The **audio processor module** accepts an external audio input and, after processing, generates an audio output.
- The **microcode controller interface** takes care of accepting commands and passing data to the different parts of the audio processing unit.
- The **host interface** takes care of addressing the internal registers and buffers. The CIAP can interface with two possible hosts; a 68000 type host or a microcontroller that interfaces via a serial link.

REGISTER MEMORY MAP

Table 1. Registers and Buffers

Address (HEX)	Register	Description
0000	—	ADPCM buffer 0
08FE		
0900	—	ADPCM buffer 1
11FE		
1200	—	DATA buffer 0
1B22		
1B24	—	Q–buffer 0
1B2C		
1B2E	—	R … W buffer 0
1B8C		
1BC2	—	DATA buffer 1
24E4		
24E6	—	Q–buffer 1
24EE		
24F0	—	R … W buffer 1
254E		
2584	IER	Interrupt enable register
2586	ISR	Interrupt status register
2588	TACS	Temporal audio channel select register
258A	AACS	Actual audio channel select register
258C	TCM1	Temporal channel mask register
258E	ACM1	Actual channel mask register 1
2590	ACM2	Actual channel mask register 2
2592	FILE	File selection register
2594	BMAN	Buffer management register
2596	CCR	CIAP control register
259A	A_SHDW	ADPCM shadow register
25A0	AP_Left	Audio processor unit left register
25A2	AP_Right	Audio processor unit right register
25A4	AP_Vol	Audio processor unit volume register
25A6	APCR	Audio processor control register
25A8	ACONF	Audio configuration register
25AA	ASTAT	Audio processor status register
25C0	ICR	Interrupt control register
25C2	DMACTL	DMA control register
25FE	DLOAD	Download register

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) . . . . . 0°C to 70°C
Voltage, V_{DD} . . . . . 5 V ± 10%
Voltage, V_{SS} . . . . . 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	– 0.5	+ 7.0	V
V_I	Input Voltage	– 1.5	V_{DD} + 1.5	V
V_O	Output Voltage	– 0.5	V_{DD} + 0.5	V
I_O	Output Current	—	± 25	mA
P_d	Power Dissipation	—	1200	mW
T_{stg}	Storage Temperature	– 65	+ 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

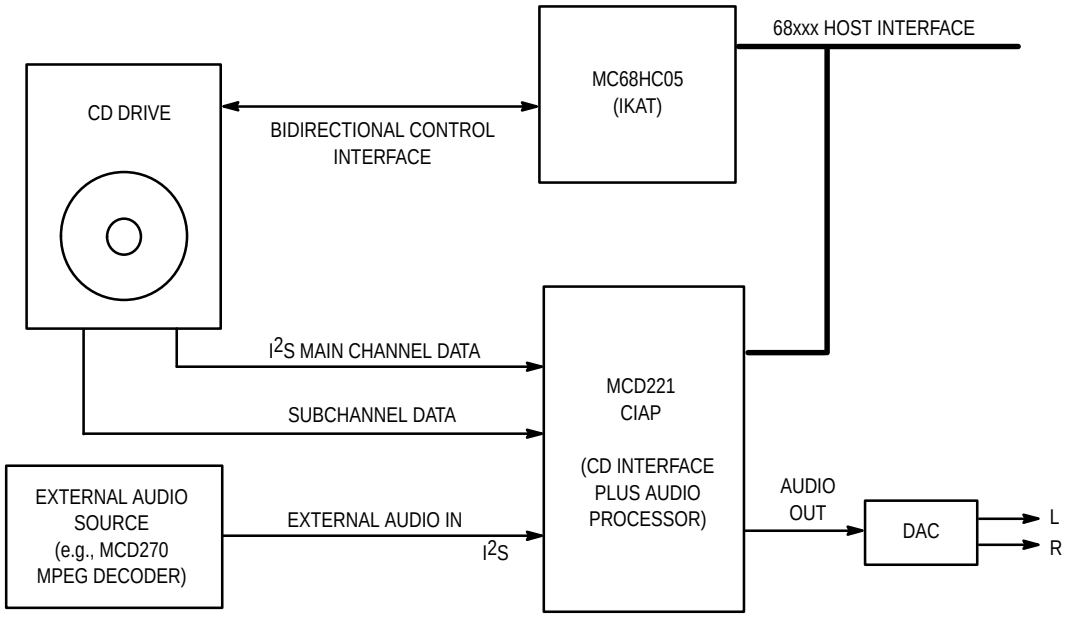
DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{DD}	33.8688 MHz	—	tba	mA
Input Voltage (TTL Input)	V_{IH} V_{IL}	— —	2.0 —	— 0.8	V
Output Voltage (8 mA)	V_{OH} V_{OL}	— —	3.5 —	— 0.4	V
Output Voltage (16 mA)	V_{OH} V_{OL}	— —	3.5 —	— 0.4	V
Power Dissipation		—	—	tba	mW

APPLICATION EXAMPLES

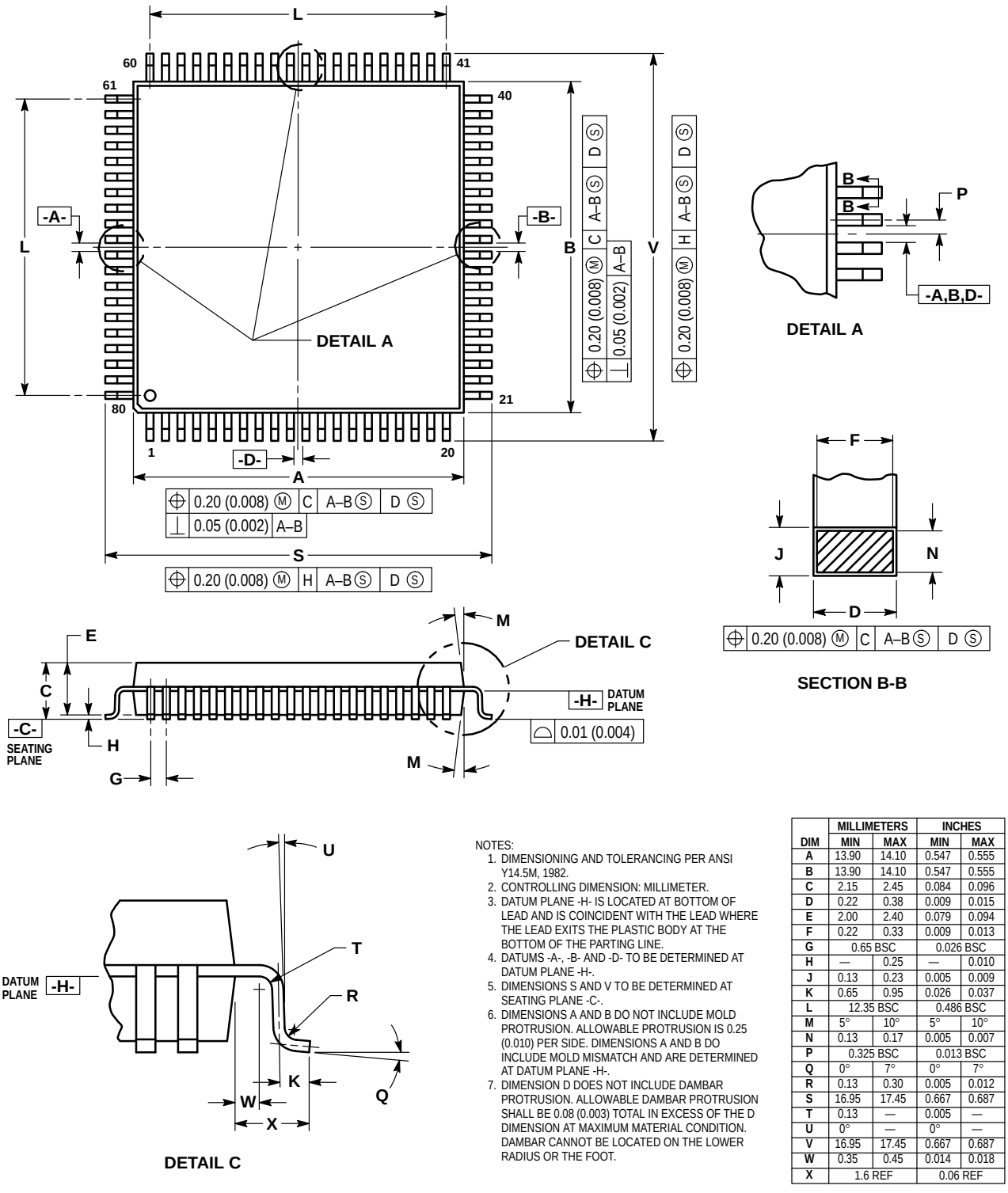
CIAP/CD–DRIVE ARCHITECTURE

In conjunction with a suitable microcontroller, MC68HC05 (IKAT), the MCD221 provides the functionality to connect an MC68xxx host processor to a CD–Drive. The MCD221 decodes both main and subchannel CD data and plays both ADPCM and CDDA audio. External I^2S format audio (e.g., MPEG1) may be input and mixed with the CIAP audio. CIAP audio output can be in either I^2S or Sony formats.



PACKAGE DIMENSIONS

FU SUFFIX
CASE 841B–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	13.90	14.10	0.547	0.555
C	2.15	2.45	0.084	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.40	0.079	0.094
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	12.35 BSC		0.486 BSC	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	16.95	17.45	0.667	0.687
T	0.13	—	0.005	—
U	0°	—	0°	—
V	16.95	17.45	0.667	0.687
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.06 REF	

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.