DMA Controller Pinout

Revision 1.3, 12.3.97 PR

Signal	Direction	Package Pin	Drive [mA]
VDD1		1	
VDD2		2	
VSS1		3	
VSS2		4	
A[23]	bidi	5	6
A[22]	bidi	6	6
A[21]	bidi	7	6
A[20]	bidi	8	6
A[19]	bidi	9	6
A[18]	bidi	10	6
A[17]	bidi	11	6
A[16]	bidi	12	6
A[15]	bidi	13	6
A[14]	bidi	14	6
A[13]	bidi	15	6
A[12]	bidi	16	6
A[11]	bidi	17	6
A[10]	bidi	18	6
A[9]	bidi	19	6
A[8]	bidi	20	6
A[7]	bidi	21	6
A[6]	bidi	22	6
A[5]	bidi	23	6
A[4]	bidi	24	6
VDD3		25	
VDD4		26	
VSS3		27	
VSS4		28	
VDD5		29	
A[3]	bidi	30	6
A[2]	bidi	31	6
A[1]	bidi	32	6
D[15]	bidi	33	6
D[14]	bidi	34	6
D[13]	bidi	35	6
D[12]	bidi	36	6
D[11]	bidi	37	6
D[10]	bidi	38	6
D[9]	bidi	39	6
D[8]	bidi	40	6
VSS5		41	
D[7]	bidi	42	6
D[6]	bidi	43	6
D[5]	bidi	44	6
D[4]	bidi	45	6
D[3]	bidi	46	6
D[2]	bidi	47	6
D[1]	bidi	48	6
D[0]	bidi	49	6
RESET*	in	50	
VDD6		51	
VDD7		52	

VSS6		53	
VSS7		54	
R/W*	bidi	55	6
TS*	bidi	56	6
†TA*	bidi	57	6
BRI*	in	58	
BGO*	out	59	3
BDI*	in	60	
DREQ*	in	61	
DACK*	out	62	3
DONE*	bidi	63	3
OWN*	out	64	3
††ENID	-	65	
SIZE	in	66	
DDIR*	out	67	3
UWE/LWE*	out	68	3
IRQ[7]*	in	69	
IRQ[6]*	in	70	
IRQ[5]*	in	71	
IRQ[4]*	in	72	
IRQ[3]*	in	73	
IRQ[2]*	in	74	
VDD8		75	
VDD9		76	
VSS8		77	
VSS9		78	
VDD10		79	
IRQ[1]*	in	80	
IACK[7]*	out	81	3
IACK[6]*	out	82	3
IACK[5]*	out	83	3
IACK[4]*	out	84	3
IACK[3]*	out	85	3
IACK[2]*	out	86	3
IACK[1]*	out	87	3
IPL[2]*	out	88	3
IPL[1]*	out	89	3
VSS10		90	
IPL[0]*	out	91	3
IACKI*	in	92	
DS*	out	93	6
AS*	out	94	6
DTACK*	in	95	
CS*	in	96	
CLKOUT	out	97	6
TEST*	in	98	
XTALI	in	99	
XTALO	out	100	

† This output has an active release output, driving to logic '1' then releasing to OD.

†† This is a special test pin. For normal operation, this pin must be tied to VSS (GND).