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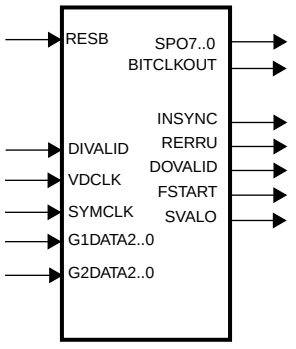
MC92309

Product Preview

Single Chip FEC for OFDM

The MC92309 is the concatenation of the Viterbi Decoder MC92300, the Convolutional Deinterleaver and Reed-Solomon Decoder MC92301. The device is compatible with the OFDM MC92308 and is fully compliant to the ETSI specification for digital terrestrial broadcasting (PR ETS 300744).



Feature Summary

- Max Operating Frequency is 37.0 MHz
- Programmable via I^2C standard serial interface
- implements K=7, (171_8,133_8) Viterbi decoder for rates 1/2, 2/3, 3/4, 5/6 and 7/8 with a survivor depth of 96
- DVB compliant 12x17 Forney Convolutional Deinterleaver
- Reed-Solomon (204,188,8) Decoder as specified by DVB
- VDD = 3.3V
- available in 100 Pin Plastic Quad Flat Package

Ordering Information	
Device	**Package**
MC92309	100QFP

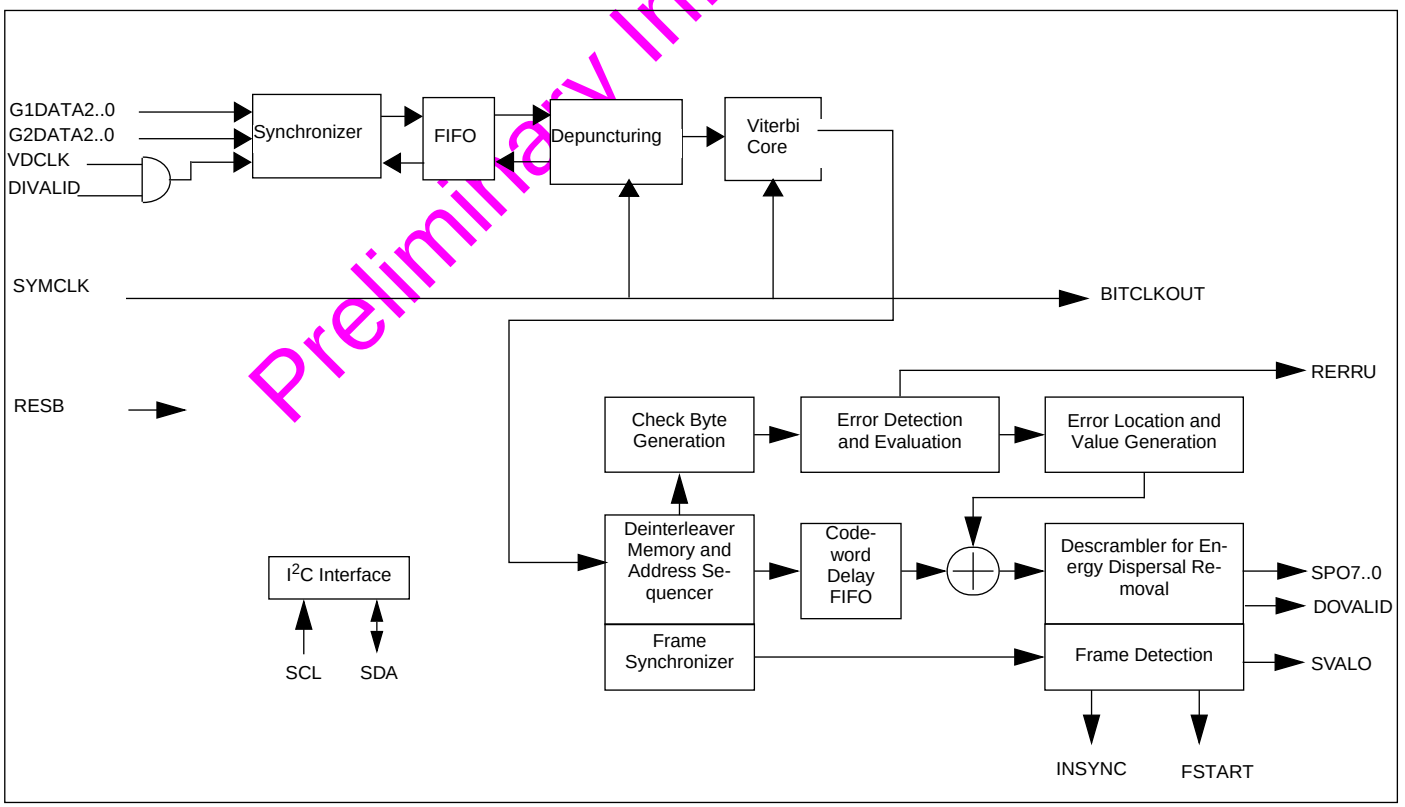


Figure 1. FEC Block Diagram

This document contains information on a product under development.
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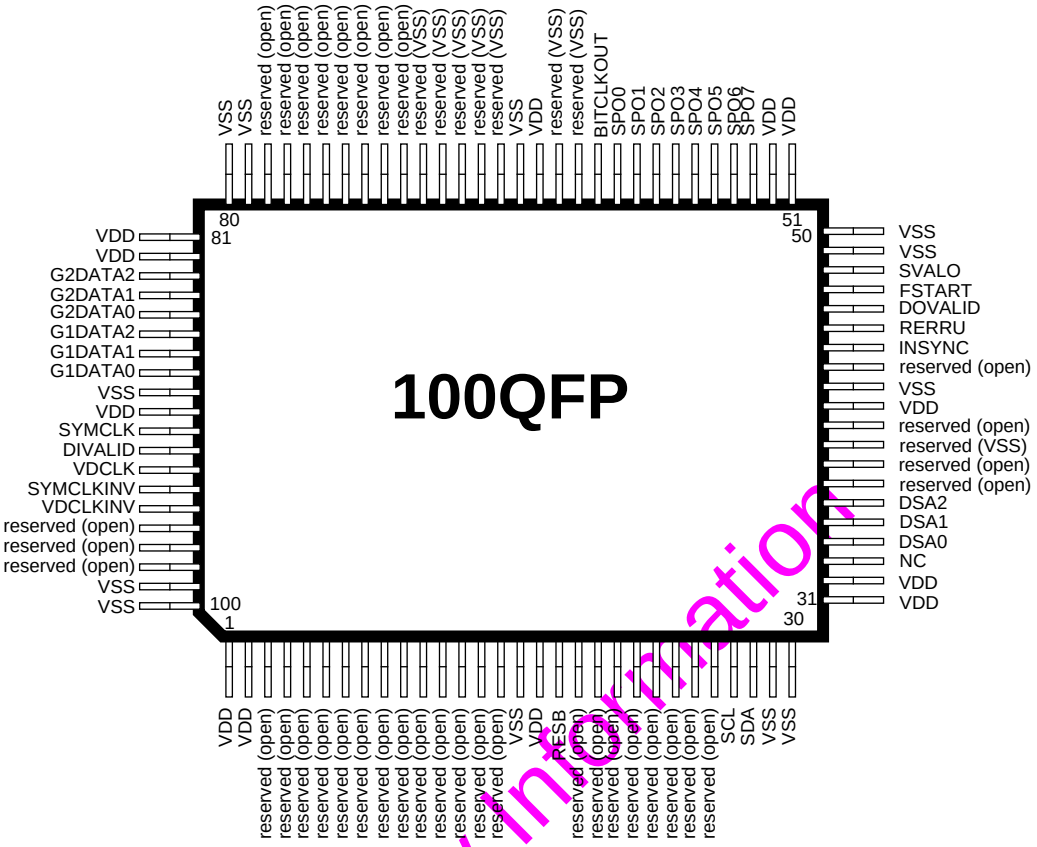

Table 1. MC92309 Pin Description

PIN No	SIGNAL	DESCRIPTION	DIRECTION
27	SCL	I^2C Clock	INPUT
28	SDA	I^2C Data	BIDIRECTIONAL
34..36	DSA0..2	I^2C Address (lower bits)	INPUT
44	INSYNC	Frame Synchronizer in Lock	OUTPUT
45	RERRU	Uncorrectable MPEG2 Frame Indicator	OUTPUT
46	DOVALID	MPEG2 Payload Byte Valid at Output	OUTPUT
47	FSTART	MPEG2 Sync Byte Indicator	OUTPUT
48	SVALO	MPEG2 Byte Clock related to SPO7..0	OUTPUT
53..60	SPO7..0	MPEG2 Transport Stream Byte Data	OUTPUT
61	BITCLKOUT	SYMCLK related to outputs	OUTPUT
83..85	G2DATA2..0	Soft Decision Input 2	INPUT
86..88	G1DATA2..0	Soft Decision Input 1	INPUT
91	SYMCLK	System Clock	INPUT
92	DIVALID	Input Data Valid	INPUT
93	VDCLK	Clock for Depunctured Input Data	INPUT
94	SYMCLKINV	180^o Phase Shift for SYMCLK	INPUT
95	VDCLKINV	180^o Phase Shift for VDCLK	INPUT

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