MC92300

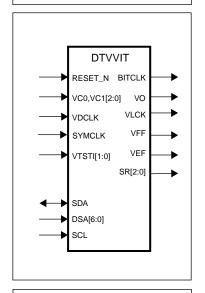
Product Preview

VITERBI Decoder for Digital TV

This product preview describes a high performance device, a Viterbi Decoder, for Digital-TV applications according to the EBU defined DVB transmission standard for satellite and cable Set-Top systems.

Viterbi Decoder - Capability Specification

- Operates at max. 50MBits/s output rate to work with all present DVB channels
- Implements K=7, (171₈,133₈) Viterbi decoder for rates 1/2, 2/3, 3/4, 5/6 and 7/8 with a survivor depth of 96
- Code rate and synchronization control programmable via I²C standard serial bus
- Automatic rate selection and signal quality output (qval)
- Full/empty flag generation of input FIFO for system monitoring of VDCLK/BITCLK ratio
- Simplified system design with internal PLL for the generation of output BITCLK from the incoming VDCLK for all depuncturing modes
- Available in a 128QFP package



| Ordering Information | | | | |
|----------------------|---------|--|--|--|
| Device | Package | | | |
| MC92300CG | 128QFP | | | |

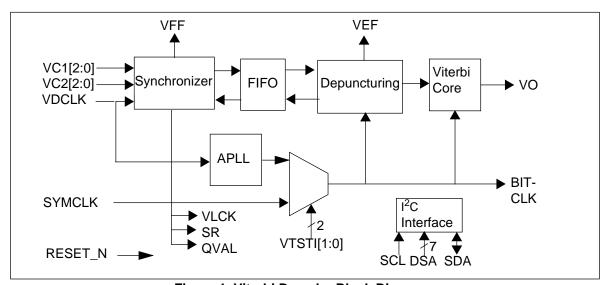


Figure 1. Viterbi Decoder Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Product Description

The Viterbi Decoder contains the Viterbi core logic, which operates the K=7 convolutional code and generates a lock indication after successful acquisition. The core works with the main clock BITCLK, which provides the output data VO (output of the Viterbi). This clock is generated by the integrated bit clock generator circuit and is adjusted according to the programmed depuncturing rate.

The input to the chip are 3 bit soft decision data VC0/1 from the QPSK demodulator together with the associated demodulator clock VDCLK. Rate adjustment in accordance with the several depuncturing rates is achieved with the input FIFO. The data is read into the depuncturing logic with the internally generated BITCLK.

Generator Polynomials

The Viterbi decoder is designed to decode bit streams encoded using the DVB standard generator polynomials (171₈, 133₈).

Punctured Codes

The Viterbi Decoder is able to decode a basic rate 1/2 convolutional code and the "standard" punctured codes for a k=7 constraint length. The punctured codes are shown in the table below. Specific bits of the original rate 1/2 code sequence are periodically deleted prior to transmission according to the entries in the table, where a 0 means that the bit is deleted and a 1 means that the bit is transmitted.

Table 1 Deletion Map For Punctured Rate 1/2 Codes

| Coding Rate | Puncture Map |
|----------------|--------------------|
| 1/2 | 1 1 |
| 2/3 | 11 10 |
| 3/4 | 110 101 |
| 5/6 | 11010 10101 |
| 7/8 | 1111010 1000101 |

Synchronization

Prior to outputting valid data the Viterbi decoder block must synchronize to the input data stream, i.e. remove any phase ambiguity in the received symbols and determine the punctured code rate transmitted The Viterbi block employs a method known as Syndrom Based Node Synchronization to achieve both I & Q symbol and punctured rate synchronization.

The theory of the Syndrom Based Node Synchronization is based on the observation that the product of the incoming data and a syndrom is zero if there are no errors If errors are present in the data, the probability of 0's and 1's in the product increases.

The possible states that the synchronizer has to deal with are a combination of the following factors:

- 1. The phasing of the received symbols.
 - I & Q input streams can either be processed as-is or can be rotated 90° to account for constellation rotation in the receiver.
- Determination of the framing of the I and Q bit streams so as to extract the correct symbol. There are four possible ways to frame the two bit stream and the synchronizer must determine the correct one.

I²C Interface

The internal registers of the VITERBI are accessible via the I²C interface. After reset, default values are preprogrammed, so that no more configuration is necessary.

APLL

In order to allow a simple system design, a Analogue PLL is integrated for generation of the output Bit Clock. The following output frequencies R_o are generated for a given DVB transponder Bandwidth TBW respectively for a given input symbol rate R_s .

| TBW[MHz] | R _s [MHz] | | Hz] fo 2/3 | r rate 3/4 | s 5/6 | 7/8 |
|--------------------------------|----------------------|------|---------------|---------------|----------|------|
| 36 33 30 | 38.3 | 28.3 | 37.7 | 42.4 | 47.2 | 49.5 |
| 27 26 | 20.5 | 20.5 | 27.3 | 30.7 | 34.2 | 35.9 |
| R _s /R _o | | 1 | 4/3 | 3/2 | 5/3 | 7/4 |

Application

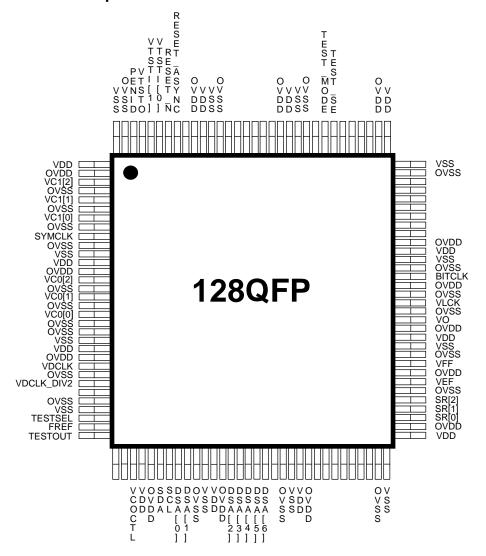
The MC92300 is used in satellite receiver implementation for DVB.

Packaging

The MC92300 is available in a 128-pin Plastic Quad Flat Pack (128QFP) package.

MOTOROLA MC92300

Viterbi Decoder Pin Description



SYMCLK - System Clock (input clock)
BITCLK - System Clock (output clock)

VDCLK - Input Clock VDCLK_DIV2 - VDCLK/2

RESET_N - Asynchronous Reset
VLCK - Viterbi Decoder in Lock

VFF - FIFO Full Flag
VEF - FIFO Empty Flag
SR[2:0] - Selected Rate

VO - Viterbi Decoder Output

VC0,VC1[2:0] - Soft Decision Input

SDA - Data Bus of I²C-interface

DSA[6:0] - Slave Address of I²C-interface

SCL - Clock Line of I²C-interface

TESTSEL, FREF, TESTOUT,

VCOCTL - APLL pins

VTSTI[1:0] - Test pins VTSTO - Test output

RESET_ASYNC - Teset for Scan Test
TEST_SE - Test pin for Scan Mode
TEST_MODE - Test pin for Scan Mode

MOTOROLA Device Test Pins: 51, 56-62, 105, 110-115, 120 (don't connect these pins)

NOT CONNECTED Pins: 27, 33, 34, 88-94, 99-102

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver Colorado 80217. 1-800-441-2447 or 303-675-2140

MFaxTM: RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609 INTERNET:http://mot-sps.com/sps/General/sales.html

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

